# Jitter in Ring Oscillators

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***Abstract*— Jitter in ring oscillators is theoretically described, and predictions are experimentally verified. A design procedure is developed in the context of time domain measures of oscillator jitter in a phase-locked loop (PLL). A major contribution is the identification of a design figure of merit $\kappa$, which is independent of the number of stages in the ring. This figure of merit is used to relate fundamental circuit-level noise sources (such as thermal and shot noise) to system-level jitter performance. The procedure is applied to a ring oscillator composed of bipolar differential pair delay stages. The theoretical predictions are tested on 155 and 622 MHz clock-recovery PLL's which have been fabricated in a dielectrically isolated, complementary bipolar process. The measured closed-loop jitter is within 10% of the design procedure prediction.**

***Index Terms*—Design methodology, jitter, noise measurement, oscillator noise, oscillator stability, phase jitter, phase-locked loops, phase noise, voltage controlled oscillators.**

## I. Introduction

DUE to their speed and ease of integration, ring oscillators are increasingly being used as voltage controlled oscillators (VCO's) in jitter sensitive applications. One example is in clock recovery phase-locked loops (PLL's) for serial data communication [1]–[3]. Other applications that would benefit from the cost and size advantages of a fully integrated low jitter VCO include disk drive clock recovery [4], [5], clock frequency multiplication [6], [7], and oversampling analog-to-digital converters (ADC's) [8], [9].

This paper presents a framework for a theoretical understanding of fundamental limits on jitter performance in ring oscillator VCO's and a design methodology for connecting system-level, closed-loop PLL jitter performance to circuit-level VCO design. Section II begins development of this approach by comparing the ring oscillator to harmonic and relaxation oscillators in the context of noise analysis. Sections III and IV continue development in terms of time domain measures of jitter performance. Section V presents the key equations of the design methodology as applied to a bipolar differential pair delay stage. Section VI gives experimental results.

## II. Comparison of Oscillator Types

### A. Harmonic Oscillator

A harmonic oscillator is characterized by an equivalence to two energy storage elements, operating in resonance, to give a periodic output signal. The actual resonant element might be an *LC* tank or a quartz crystal. Resonant circuit-based VCO's are known to have excellent jitter performance [10], [11]. Unfortunately, the requirement of an off-chip tank or crystal defeats the purpose of integrating the PLL function. Although integrated inductors have been reported in the GHz frequency range [12], these generally have low $Q$ due to resistive losses, and in any case are not practical in the 100 MHz–1 GHz frequency range. Analysis of noise in resonant-based VCO's is well developed in the literature [13]–[15], and design techniques for realizing low jitter performance are relatively well understood. In general, the noise analysis has been approached in the frequency domain, with the high $Q$ of the circuit resonance filtering noise into a narrow band near the fundamental frequency.

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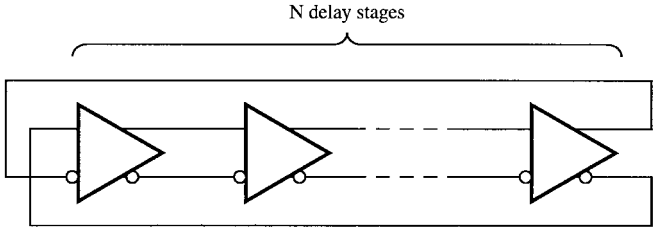


Fig. 1. Typical ring oscillator schematic.

### B. Multivibrator

A relaxation (multivibrator) oscillator is characterized by an equivalence to one energy storage element, with additional circuitry that senses the element state and controls its excitation to give a periodic output signal [16]. Fully integrated clock recovery PLL's have been described using multivibrator VCO's [1], [17]–[19]. In general, jitter analysis for this type of oscillator has been approached in the time domain [16], [20], [21]. The jitter performance of the multivibrator is known to be worse than the harmonic oscillator, although some design techniques for improving jitter are available [16], [22], [23]. The best jitter performance that has been achieved by a multivibrator is larger than typically desired for fully integrated VCO's.

### C. Ring Oscillator

Fig. 1 shows the general ring oscillator investigated in this work: a loop of $N$ delay stages with a wire inversion. The ring will oscillate with a period of $2N$ times the stage delay. Voltage controlled ring oscillators have recently been explored as an alternative to the multivibrator for fully integrated, lower jitter clock recovery PLL's [2], [3], [7], [24]–[31]. Like the multivibrator, a ring oscillator is fully integrable. In addition,

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some of the empirical results show promise of excellent jitter performance [3]. However, investigation into a theoretical analysis of jitter has only recently begun for bipolar [30], [31] and CMOS [32], [33] ring oscillators. Perhaps one reason that analysis of jitter in ring oscillators has lagged is that the ring does not fit well into either of the harmonic or multivibrator oscillator models. The number of energy storage elements is not as explicit; in fact there are many "energy storage elements" since the ring is composed of multiple stages.

## III. Methods of Quantifying Jitter

The design technique developed in this paper follows from different methods of measuring jitter in the time domain. Following is a brief description of three relevant time domain measures of jitter. Note that in the closed-loop cases, it is assumed that the VCO is the dominant jitter source.

### A. Closed-Loop, Transmit Clock Referenced

For a clock recovery PLL, jitter is usually specified as the standard deviation $\sigma_x$ of the phase difference between the transmitted clock and the recovered clock. This measurement can be made as shown in Fig. 2(a), using an instrument such as a communications signal analyzer (CSA) [34]. The transmit clock $TCLK$ is used to trigger the CSA; the recovered clock $RCLK$ is observed as the CSA input. In the presence of jitter, a distribution of threshold crossing times is observed as shown in Fig. 2(b). The CSA records a histogram of this distribution; the standard deviation of the distribution is $\sigma_x$.

Although this test is a simple indicator of PLL performance, the test provides little information on improving jitter from circuit-level noise sources if $\sigma_x$ is not satisfactory. This test also requires the PLL to be operating closed-loop. VCO design and simulation would be simplified if we could consider the VCO by itself (open loop), while being able to predict the closed-loop $\sigma_x$.

### B. Open Loop, Self Referenced

We can also measure the jitter of the VCO on a stand-alone basis as shown in Fig. 2(c). With the VCO free-running at its center frequency, $RCLK$ is used as both the trigger and the input to the CSA. The CSA compares the phase difference between transitions in the clock waveform, separated by an interval $\Delta T$ derived from the CSA's internal time base. As in the previous case, the CSA measures the standard deviation of the threshold crossing times $\sigma_{\Delta T(\mathrm{OL})}$.

In this measurement, however, the standard deviation is observed to depend on the measurement interval $\Delta T$. Fig. 2(d) shows a typical plot of $\sigma_{\Delta T(\mathrm{OL})}$ versus $\Delta T$ on log–log axes. It can be shown that, for a large class of noise processes [30]–[32], the jitter increases as the square root of the measurement interval

$$\sigma_{\Delta T(\mathrm{OL})}(\Delta T) \approx \kappa\sqrt{\Delta T}. \tag{1}$$

The proportionality constant $\kappa$ is an important time domain figure of merit which will be used in design to connect open-loop and closed-loop performance, as well as circuit-level and system-level design.

Intuitively, (1) can be understood by considering the jitter over the measurement interval $\Delta T$ to be the sum of jitter contributions from many individual stage delays. If these jitter errors are independent, then the standard deviation of the sum increases as the square root of the number of delays being summed.

### C. Closed Loop, Self Referenced

The open-loop and closed-loop jitter performance can be related by measuring the "stand-alone" jitter performance of the clock recovered under closed-loop conditions, as shown in Fig. 2(e). When lead-lag compensation is used, the closed-loop transfer function $H(s)$ is that of a second-order system [35]. In clock recovery PLL's, however, it is common to overdamp the loop to avoid peaking in the jitter transfer function [30], and the loop transfer function can be approximated as

$$H(s) = \frac{2\pi f_L}{s + 2\pi f_L} \tag{2}$$

which is a first-order system, where $f_L$ is the loop bandwidth. In this case, the plot of $\sigma_{\Delta T(\mathrm{CL})}$ versus $\Delta T$ is of the form shown in Fig. 2(f) [30], [32]. The plot shows two asymptotes which can be understood qualitatively as follows: At short delays, the jitter increases in proportion to the square root of delay, just as in the open-loop case. This is because at time scales shorter than the loop bandwidth time constant, the VCO control voltage cannot change appreciably, and the VCO is essentially running open loop. At longer delays, the phase detector and loop filter are able to sense accumulated phase error due to VCO jitter and adjust the VCO input to bring the VCO phase "back in line" with the transmit clock. At very long delays, the jitter over the measurement interval $\Delta T$ is due to the $\sigma_x$ jitter at the beginning and end of the $\Delta T$ time period. Since the jitter errors of clock edges separated by a long delay are uncorrelated, the total jitter is $\sqrt{2}\sigma_x$.

Analysis [30] shows that the two asymptotes intersect at the loop bandwidth time constant $\tau_L = 1/2\pi f_L$. We can use this to solve for the closed-loop $\sigma_x$ in terms of the open-loop figure of merit $\kappa$

$$\sigma_x = \kappa\sqrt{\frac{1}{4\pi f_L}}. \tag{3}$$

If $f_L$ is a free parameter, the closed-loop jitter can be reduced simply by increasing $f_L$. However, if $f_L$ is fixed (for example, by specification as in SONET [36]), then the only way to reduce closed-loop jitter is to improve the oscillator by reducing the open-loop time domain figure of merit $\kappa$.

## IV. Jitter Independence of Ring Length

The parameter $\kappa$ is a link between the open-loop VCO and the closed-loop system-level jitter performance. We will see in Section V that, at the circuit level, it is possible to determine $\kappa$ for a single delay stage. To complete the design path from circuit level to system level, it is necessary to determine how the circuit-level $\kappa$ is affected when a number of stages are combined to form a ring oscillator.

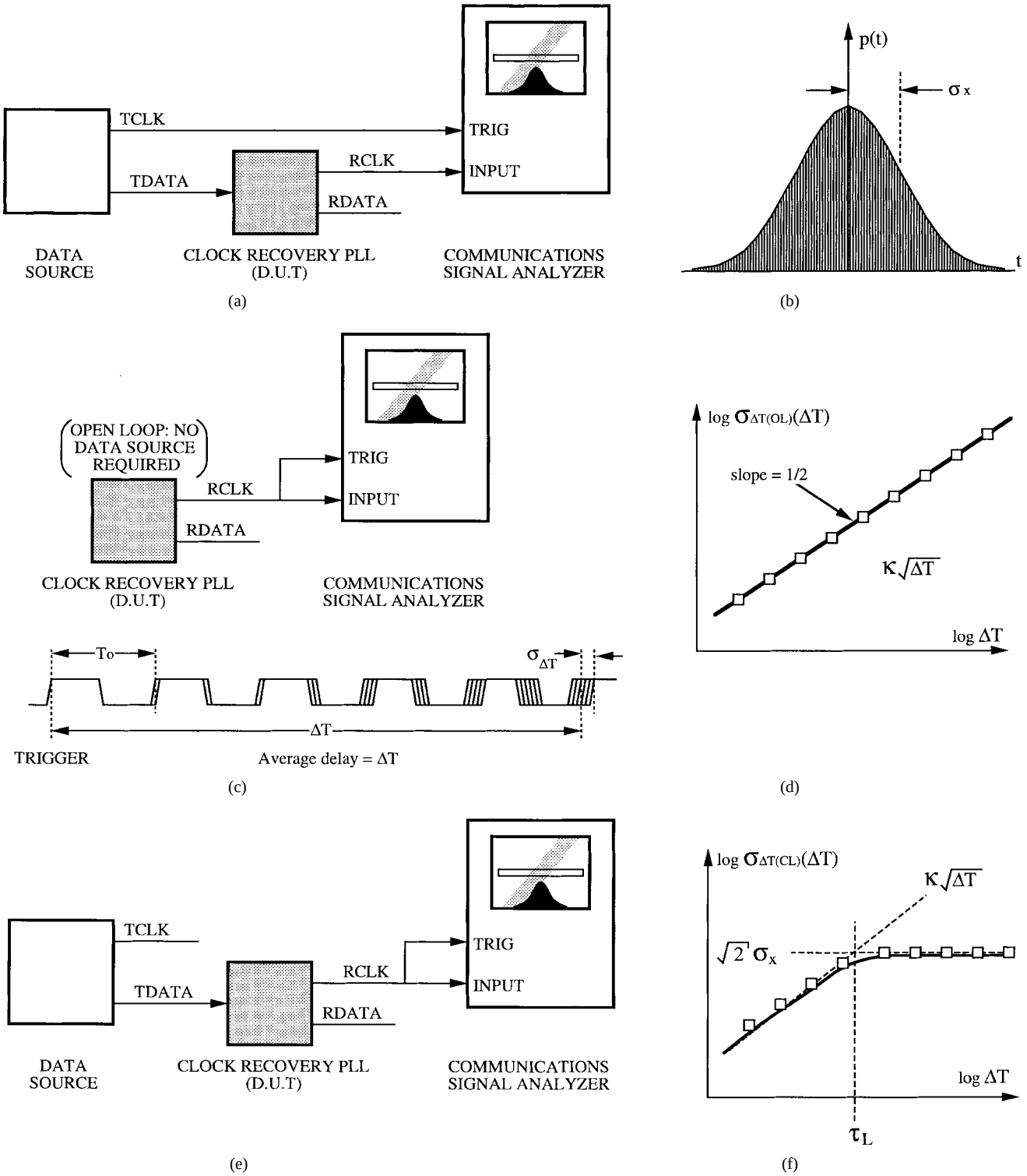


Fig. 2. (a) Measurement technique: time domain, closed loop, and transmit clock referenced. (b) Measurement result: standard deviation of $TCLK/RCLK$ phase. (c) Measurement technique: time domain and open loop. (d) Measurement result: standard deviation versus delay time $\Delta T$. (e) Measurement technique: time domain and closed loop. (f) Measurement result: standard deviation versus delay time $\Delta T$.

An experiment was performed in which ring oscillators of lengths three, four, five, seven, and nine stages were fabricated in a 3-GHz $f_T$ junction-isolated Si bipolar process [31]. The delay element was the gate shown in Fig. 3. The jitter performance for each ring was measured using the open-loop technique described in Section III-B; the results are plotted in Fig. 4. The experimental results in Table I show the least-squares-fit values for $\kappa$, as well as the free-running VCO center frequencies.

Fig. 4 shows that the jitter increases roughly as the square root of delay time, consistent with the model of (1). More importantly, the jitter over a given measurement interval is the same regardless of how many stages there are in the ring. Table I shows that the $\kappa$ values are approximately the same

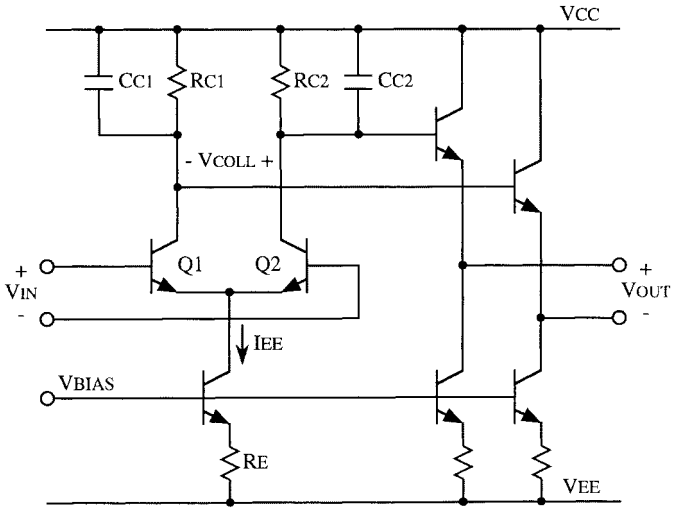


Fig. 3. Differential pair delay gate.

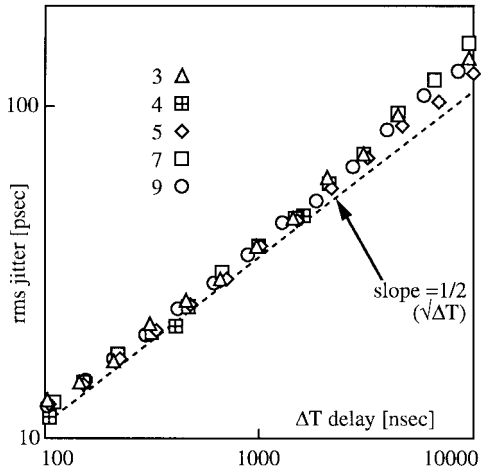


Fig. 4. Jitter versus delay for three-, four-, five-, seven-, and nine-stage rings.

TABLE I
RING EXPERIMENT RESULTS

| RING STAGES | κ [E-08√sec] | fo [MHz] |
|---|---|---|
| 3 | 4.17 | 170.1 |
| 4 | 3.56 | 164.1 |
| 5 | 3.78 | 102.7 |
| 7 | 3.77 | 71.9 |
| 9 | 3.94 | 56.8 |

regardless of the length of the ring: even as center frequency varies by a 3 : 1 ratio over a range of 56–170 MHz, the value of $\kappa$ changes by only $\pm 8\%$. We conclude that the ability of a ring to accurately measure an interval of time depends primarily on the accuracy of its basic delay element as characterized by $\kappa$ and is essentially independent of the number of stages in the ring. When we have characterized the accuracy of the delay stage in terms of $\kappa$, we can predict the jitter for a ring of any length using that stage.

This may seem counterintuitive at first: when more delay stages (and, seemingly, more noise sources) are added, why is the jitter unchanged? The reason can be seen by considering the jitter accumulation process from the "point of view" of the signal transition or "edge" that propagates around the ring. The only delay stage that affects jitter accumulation at a given instant is the stage that is processing the transition. All other gates in the ring are inactive and do not contribute to jitter. Thus, from the standpoint of jitter accumulation, the key measure is the number of gate transitions, not the number of oscillator periods. This is why measures that normalize to the oscillator period are not independent of the number of stages [32].

## V. Determining $\kappa$ Expressions for Jitter Sources

To determine $\kappa$ at the gate level requires a detailed analysis of each circuit-level noise source and depends on the particular gate used as the delay element in the ring. For design illustration, the simple delay stage shown in Fig. 3 will be analyzed. The input voltage $v_{\rm IN}$ causes differential pair $Q_1/Q_2$ to steer the tail current $I_{EE}$ to one of the collector loads, $R_{C1}$ or $R_{C2}$. Capacitors $C_{C1}$ and $C_{C2}$ represent wiring stray, junction, and any explicit capacitances that may be present at the collector node. We begin the analysis by noting that the delay through the gate has two components: the delay through the differential pair (from $v_{\rm IN}$ to $v_{\rm COLL}$), and the delay through the emitter follower buffers (from $v_{\rm COLL}$ to $v_{\rm OUT}$). To simplify the analysis and make the results easier to interpret, we will now make some assumptions regarding the gate delay.

i) The gate delay is dominated by the differential pair delay.
ii) The differential pair delay is dominated by the RC time constant of the load.
iii) The differential signal amplitude is much greater than $V_T = kT/q_e$.
iv) The amplitude of the noise is much smaller than the differential signal.
v) All noise sources are white and uncorrelated.

As has been shown in the literature [37], the switching time of a differential pair depends on many factors, so some tradeoff of accuracy is necessary to obtain a simple analytical expression. Generally, as long as assumption iii) holds, the differential pair switches the tail current much faster than the RC time constant of the collector load, and assumption ii) introduces an error less than 20% of delay time. The error due to assumption i) is usually less than 10%. Although the error in delay time due to these assumptions is not insignificant, the assumptions are nevertheless justified since the resulting theory predicts jitter quite well and provides insights for guiding design. The following subsections derive the effective $\kappa$ for the most significant noise sources in the differential pair delay.

### A. Thermal Noise of Collector Load Resistors

For noise analysis, the circuit can be modeled as shown in Fig. 5(a). Thermal noise in the collector load is represented by

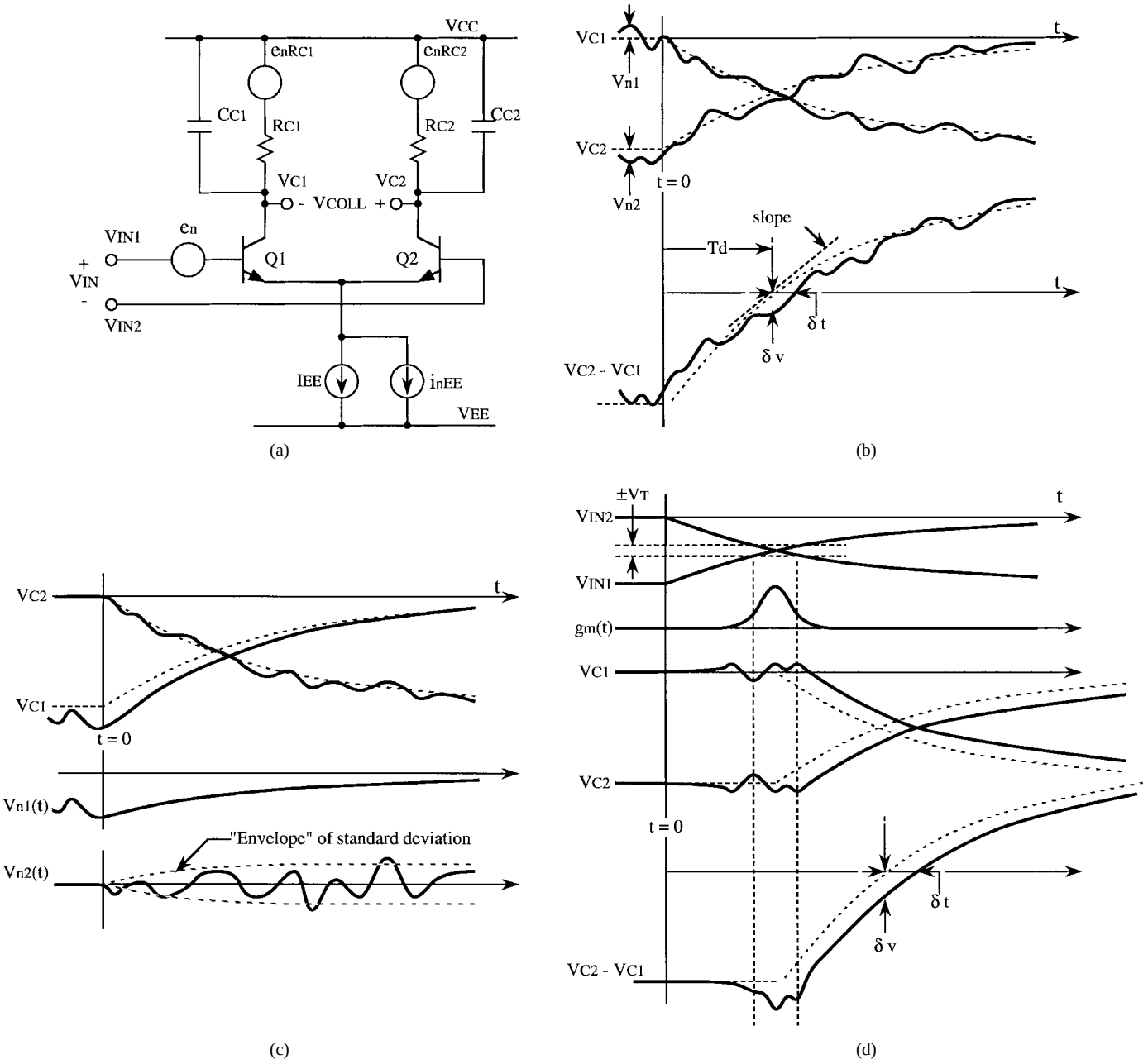


Fig. 5. (a) Noise model, (b) voltage waveforms, $R_{C1}/R_{C2}$ thermal noise (noise effect exaggerated), (c) tail current source noise waveforms, and (d) differential input switching noise waveforms.

$e_{nR_{C1}}$ and $e_{nR_{C2}}$. These sources appear directly at $v_{C1}$ and $v_{C2}$, but are bandlimited by the $R_{C1}C_{C1}$ and $R_{C2}C_{C2}$ poles. If the differential pair is represented by an ideal switch that is switched at time $t = 0$, the noise-free differential signal is given by

$$\begin{aligned} v_{\mathrm{COLL}}(t) &= v_{C2}(t) - v_{C1}(t) \\ &= I_{EE}R_C\left[1 - 2\exp\left(\frac{-t}{R_CC_C}\right)\right] \end{aligned} \tag{4}$$

with $R_{C1} = R_{C2} = R_C$ and $C_{C1} = C_{C2} = C_C$. The noise-free exponential waveforms are shown as dashed lines in Fig. 5(b). The gate delay $T_d$ is defined as the time when the differential voltage $v_{\mathrm{COLL}}$ crosses zero. For the noise-free waveform, solving (4) for $T_d$ gives

$$T_d = \ln(2)R_CC_C. \tag{5}$$

The slope of the differential signal is given by taking the derivative of (4) with respect to time and evaluating at $T_d$, giving

$$\left.\frac{dv_{\mathrm{OUT}}}{dt}\right|_{T_d} = \frac{I_{EE}}{C_C}. \tag{6}$$

The solid lines in the figure represent the actual collector waveforms, including the exaggerated effect of typical thermal noise waveforms $v_{n1}(t)$ and $v_{n2}(t)$. By superposition, the noise waveforms simply "ride" on the ideal exponential. The result is that, at the time of the ideal differential waveform

zero crossing, there is a voltage error $\delta v$. This causes a time error in the threshold crossing $\delta t$. Since [by assumption iv)] the noise is much less than the exponential signal, then (6) can be used to relate the errors $\delta v$ and $\delta t$, as well as the standard deviations of errors $\sigma_v$ and $\sigma_t$

$$\frac{\sigma_v}{\sigma_t} = \frac{I_{EE}}{C_C}. \tag{7}$$

The standard deviation of the differential voltage error is simply the square root of the sum of the squared (RSS) individual standard deviations $\sigma_{v1}$ and $\sigma_{v2}$. Applying the Johnson noise equation gives the well-known result $\sigma_{v1} = \sigma_{v2} = \sqrt{kT/C_C}$, so the standard deviation of the differential voltage is

$$\sigma_v = \sqrt{\frac{2kT}{C_C}}. \tag{8}$$

Using (7) and (8) gives for the standard deviation of the time error (the jitter)

$$\sigma_t = \sqrt{\frac{2kTC_C}{I_{EE}^2}}. \tag{9}$$

$\kappa$ for the individual gate is determined by dividing the standard deviation of delay $\sigma_t$ by the square root of the average delay in (5)

$$\begin{aligned}\kappa_{R_C} &= \frac{\sigma_t}{\sqrt{T_d}} \\ &= \sqrt{\frac{2}{\ln(2)}}\sqrt{\frac{kT}{I_{EE}^2 R_C}}.\end{aligned} \tag{10}$$

$\kappa$ has dimensions of $\sqrt{\text{sec}}$, and from (10) we see that this comes about by taking the square root of an energy ($kT$) divided by a power ($I_{EE}^2 R_C$). The rms thermal energy $kT$ represents an uncertainty in the energy of the collector load. $I_{EE}^2 R_C$ represents the dc power dissipation (energy flow) in the collector load. The intuitive meaning of (10) is that $\kappa$ characterizes the gate's ability to resolve time (jitter) by an energy uncertainty ($kT$) as a fraction of the energy flow over time ($I_{EE}^2 R_C$).

Since lower $\kappa$ corresponds to improved jitter, (10) indicates that jitter improves when bias current $I_{EE}$ is increased. This is similar to results that have been reported for differential delay stages in CMOS ring oscillators [32], [33]. Equation (10) also indicates that jitter is improved when the dc power dissipation $I_{EE}^2 R_C$ is increased. This is similar to the results of the noise analyses for harmonic and relaxation oscillators [14], [16].

### *B. Tail Current Noise*

Noise is also present in the tail current of the differential pair. This is represented by noise source $i_{nEE}$. In this case, the source is switched so the analysis is somewhat more complicated. When $v_{\text{IN}}$ is large enough to fully switch the differential pair, the current noise is passed to the output, but is bandlimited by the either the $R_{C1}C_{C1}$ or $R_{C2}C_{C2}$ pole. When $v_{\text{IN}}$ is small, the differential pair is approximately balanced, the tail current noise is a common-mode error, and its effect on the differential $v_{\text{COLL}}$ is reduced.

The analysis can be simplified by using assumption iii) to idealize the differential pair as switching instantaneously. Fig. 5(c) shows the resulting $v_{C1}$ and $v_{C2}$ waveforms, as well as the superimposed noise waveforms $v_{n1}$ and $v_{n2}$. Prior to switching, the noise current through $R_{C1}$ causes a noise voltage $v_{n1}$ with standard deviation given by

$$\begin{aligned}\sigma_{V_{n1}}(t \le 0) &= i_{nEE} R_C \sqrt{\frac{1}{4R_C C_C}} \\ &= \frac{i_{nEE}}{2}\sqrt{\frac{R_C}{C_C}}.\end{aligned} \tag{11}$$

When switching occurs at $t = 0$, this voltage is sampled on $C_{C1}$. For $t > 0$, $v_{n1}$ decays exponentially with a time constant of $R_C C_C$, so that

$$\sigma_{V_{n1}}(t > 0) = \frac{i_{nEE}}{2}\sqrt{\frac{R_C}{C_C}}\, e^{-t/R_C C_C}. \tag{12}$$

For $v_{n2}$, analysis shows [30] that the standard deviation "builds up" as

$$\sigma_{V_{n2}}(t > 0) = \frac{i_{nEE}}{2}\sqrt{\frac{R_C}{C_C}}\sqrt{1 - e^{-2t/R_C C_C}}. \tag{13}$$

Taking the root sum of (12) and (13) and evaluating at $T_d$ gives the standard deviation of the differential voltage at the zero crossing time as

$$\sigma_v = \frac{i_{nEE}}{2}\sqrt{\frac{R_C}{C_C}}. \tag{14}$$

Using (7) and (14) gives the standard deviation of the time uncertainty as

$$\sigma_t = \frac{1}{2}\sqrt{R_C C_C}\,\frac{i_{nEE}}{I_{EE}}. \tag{15}$$

Dividing $\sigma_t$ by the square root of the delay in (5) gives $\kappa$

$$\kappa = \frac{1}{2\sqrt{\ln 2}}\,\frac{i_{nEE}}{I_{EE}}. \tag{16}$$

It is interesting to consider (16) when expressions for $i_{nEE}$ are substituted for shot and thermal noise.

*Shot Noise:* Substituting the shot noise density $i_{nEE} = \sqrt{2q_e I_{EE}}$ into (16) gives

$$\kappa = \frac{1}{\sqrt{2\ln 2}}\sqrt{\frac{q_e}{I_{EE}}}. \tag{17}$$

In this case, the gate's ability to resolve time is characterized by the smallest resolvable unit of charge ($q_e$) as a fraction of the charge flow over time ($I_{EE}$).

*Thermal Noise:* If the tail current source is degenerated, the output noise will be dominated by the thermal noise of the degeneration resistor [38]. Using the thermal noise density $i_{nEE} = \sqrt{4kT/R_E}$ in (16) gives

$$\kappa_{R_E} = \frac{1}{\sqrt{\ln 2}}\sqrt{\frac{kT}{I_{EE}^2 R_E}}. \tag{18}$$

This is similar to (10) in that the gate's ability to resolve time is characterized by the energy uncertainty ($kT$) as a

fraction of the energy flow over time ($I_{EE}^2 R_E$) in the element that determines the current.

Again, in both cases an increase in bias current $I_{EE}$ results in lower $\kappa$, which corresponds to improved jitter.

### C. Sampling of Input Noise by Switching of Differential Pair

There are also noise sources in series with the inputs of the differential pair, represented by an equivalent $e_n$ in Fig. 5(a). This is due to thermal noise of the $Q_1/Q_2$ transistor base resistances [39] as well as other wideband noise sources (such as emitter followers in the signal path) going back to $v_{\mathrm{COLL}}$ of the preceding stage of the ring. Calculating the jitter effects of these sources is complicated by the fact that the gain from input to output depends on the signal amplitude. Fig. 5(d) shows the input waveforms, the time-dependent transconductance, and the collector voltages $v_{C1}$ and $v_{C2}$.

The input–output characteristic of a bipolar differential pair is

$$i_{\mathrm{OUT}} = I_{EE} \tanh\left(\frac{v_{\mathrm{IN}}}{2V_T}\right) \tag{19}$$

where tanh is the hyperbolic tangent function [39]. The incremental gain is

$$\begin{aligned} g_m &= \frac{di_{\mathrm{OUT}}}{dv_{\mathrm{IN}}} \\ &= \frac{I_{EE}}{2V_T} \operatorname{sech}^2\left(\frac{v_{\mathrm{IN}}}{2V_T}\right) \end{aligned} \tag{20}$$

where sech is the hyperbolic secant.

For input signals that are large compared to $V_T$, the gain to the output current is small. Thus, the input voltage noise has little effect when the input signal is large. As the input signals cross over during switching, however, the gain rises. During this time, the input voltage noise causes a noise current which is integrated on the collector capacitors. Although the integration is "leaky" due to the discharge path through $R_{C1}$ and $R_{C2}$, some of the integrated noise still remains when the collector voltages cross approximately $T_d$ later. Assuming all noise sources to be white, and lumped into a single source with density $e_n$, analysis [30] shows the standard deviation of the differential voltage at the zero crossing is

$$\sigma_v(T_d) = \frac{e_n}{2}\sqrt{\frac{I_{EE}}{3C_C V_T}}. \tag{21}$$

The time uncertainty obtained by dividing by the slope is

$$\sigma_t = \frac{e_n}{2}\sqrt{\frac{C_C}{3I_{EE}V_T}}. \tag{22}$$

Dividing by the square root of $T_d$ gives $\kappa$

$$\kappa = \frac{1}{2\sqrt{3\ln 2}}\, e_n \sqrt{\frac{1}{I_{EE}R_C V_T}}. \tag{23}$$

Substituting the noise density expression $e_n = \sqrt{4kTr_{bT}}$ (for an equivalent total base resistance $r_{bT}$) into (23) gives

$$\kappa_{r_{bT}} = \frac{1}{\sqrt{3\ln 2}}\sqrt{\frac{q_e}{I_{EE}}\frac{r_{bT}}{R_C}}. \tag{24}$$

This is similar to (17) in that the gate's ability to resolve time is characterized by charge ($q_e$) divided by current ($I_{EE}$). In this case, the relative magnitude of the total equivalent base resistance $r_{bT}$ and the collector resistance $R_C$ impose an additional scale factor.

### D. Noise at VCO Input

For any VCO, white noise at the VCO input will modulate the VCO frequency and add jitter. It can be shown [30] that white noise at the VCO input will give jitter following the $\kappa$ model. For a white noise density of $e_{n(\mathrm{VCO})}$, $\kappa$ is given by

$$\kappa_{\mathrm{VCO}} = \frac{1}{\sqrt{2}}\frac{K_o}{\omega_o}\, e_{n(\mathrm{VCO})} \tag{25}$$

where $K_o$ is the VCO scale factor [rad/V $\cdot$ sec] and $\omega_o$ is the VCO center frequency [rad/sec].

### E. Other Noise Influences

All of the above-mentioned sources of jitter are an inherent part of the components in the ring. In practice, external influences (such as power supply sensitivity) are often a dominant source of jitter [7], [11], [30]. The "noise floor" set by the sources described above will not be realized unless externally caused jitter can be reduced to a sufficiently low level.

### F. Combining $\kappa$ from Different Sources

Since each $\kappa$ represents a contribution from an independent noise voltage [by assumption v)], then the $\kappa$ of all sources together is just the RSS combination of the individual $\kappa$ terms from (10), (16), (24), and (25).

## VI. Implications for Design

To design for a desired closed-loop jitter $\sigma_x$, the first step is to use (3) to determine the value of $\kappa$. Then (10), (16), (24), and (25) can be used in a noise budgeting process to assign contributions of each source to the total $\kappa$. For each source, the design equations provide an explicit linkage between system level jitter (as described by $\kappa$) and circuit-level design considerations.

For example, in the case of low power design, (10) and (18) set a limit on the best possible jitter that can be achieved for a given dc power dissipation. As another example, (24) shows that for a given equivalent base resistance $r_{bT}$, there is a link between waveform amplitude $I_{EE}R_C$ and jitter. Thus, in the case of low supply voltage design (with little headroom for large signal swings), we can immediately determine the best possible jitter that could be achieved at a given signal amplitude.

The expressions for different sources of jitter allow the designer to determine which source is the major contributor in a given design. The equations also show the temperature dependence of jitter, which is important since it is possible to compensate by making circuit parameters (such as the tail current $I_{EE}$) temperature dependent as well.

TABLE II
SUMMARY OF DESIGN PARAMETERS, PREDICTED PERFORMANCE, AND MEASURED RESULTS

| | Open Loop VCO | 155 MHz PLL | 622 MHz PLL |
|---|---|---|---|
| Process | Si Bipolar Junction Isolated $f_T$ = 3 GHz | Si Bipolar Dielectrically Isolated $f_T$ = 5 GHz | Si Bipolar Dielectrically Isolated $f_T$ = 9 GHz |
| $R_C$ | 500 Ω | 1.9 kΩ | 500 Ω |
| $R_E$ | 4.0 kΩ | 9.5 kΩ | 2.5 kΩ |
| $r_{bT}$ | 1.65 kΩ | 4.80 kΩ | 1.29 kΩ |
| $I_{EE}$ | 280 μA | 122 μA | 400 μA |
| $e_{n(VCO)}$ | 11 nV/√Hz | 95 nV/√Hz | 34 nV/√Hz |
| $f_o$ | 164.1 MHz | 155.4 MHz | 622 MHz |
| $K_o$ | 44.1 MHz/V | 70.2 MHz/V | 240 MHz/V |
| $f_L$ | --- | 228 kHz | 330 kHz |
| κ (predicted) | 3.51E-08 √s | 5.46E-08 √s | 2.73E-08 √s |
| $\sigma_x$ (predicted) | --- | 32.3 ps rms | 13.4 ps rms |
| κ (measured) | 3.56E-08 √s | 6.05E-08 √s | 2.41E-08 √s |
| $\sigma_x$ (measured) | --- | 35.0 ps rms | 13.07 ps rms |
| κ error | -1.3% | -9.7% | +13% |
| $\sigma_x$ error | --- | -7.8% | +2.7% |

The relationship between open-loop ($\kappa$) and closed-loop ($\sigma_x$) performance expressed in (3) is also useful in evaluation of actual devices. From an open-loop VCO measurement of $\kappa$, we can predict what the closed-loop performance should be if limited only by the VCO jitter. Then we can compare this prediction with actual closed-loop measurements to determine if performance is being degraded by jitter coupled from other on-chip circuitry.

## VII. EXPERIMENTAL RESULTS

### A. Simulation

To test the results of the mathematical techniques developed in Section V, the effects of the individual noise sources in the circuit of Fig. 5(a) were simulated using transient noise sources and a differential pair behavioral model following (19). The simulation environment allowed control over the circuit conditions so that it was possible to isolate the effects of individual noise sources, something that would be difficult if not impossible in a physical circuit.

For each of the noise sources, circuit parameters were varied over an order of magnitude range around design center values. The simulated results [30] showed agreement to within 10% of the predicted $\kappa$ values, except when one of the assumptions i)–v) of Section V was not met. The only region of significant disagreement was for signals of amplitude $\approx V_T$. This limitation is not encountered in practice since larger signal amplitudes are used to realize lower jitter.

### B. Open-Loop Hardware Test

The measured jitter of the three-, four-, five-, seven-, and nine-stage ring oscillators of Section IV can be compared to the prediction of Section V. The design parameters for the ring delay stage circuit are given in the "Open Loop VCO" column of Table II. The predicted value of $\kappa$ is given by substituting the circuit parameter values into (10), (16), (24), and (25). Combining these in RSS fashion gives $\kappa = 3.51\text{E-}08$ $\sqrt{\text{s}}$. The dashed line in Fig. 4 shows the predicted $\sigma_{\Delta T(\text{OL})}$ corresponding to this value of $\kappa$. Good agreement is seen between this plot and the measured results.

For the four-stage ring, the circuit implementation allowed variation in the $I_{EE}$ tail current. Table III gives the measured results and the predicted $\kappa$ values. The results in Fig. 6 show good agreement, to within 5%.

### C. Closed-Loop Clock Recovery PLL Design

Using the technique of Section V, voltage controlled ring oscillators were designed and fabricated in 155 and 622 MHz clock recovery PLL's [40]. Voltage control of frequency was achieved by taking a linear interpolation of signals at different stages in the ring [41]. Table II gives process information, circuit design values, predicted performance, and measured results for each case. Substituting these into (10), (16), (24), and (25), and combining in RSS fashion gives the predicted value of $\kappa$. Using this $\kappa$ and the loop bandwidth $f_L$ in (3) gives the predicted value of $\sigma_x$. As can be seen from Table II, the agreement between the predicted and measured results for $\kappa$ and $\sigma_x$ is quite good. Fig. 7 shows the measured closed-loop

TABLE III
MEASURED RESULTS AND PREDICTED $\kappa$ VERSUS IEE

| | $\kappa$ components [E-08$\sqrt{\text{sec}}$] | | | | $\kappa$ [E-08$\sqrt{\text{sec}}$] | | |
|---|---|---|---|---|---|---|---|
| $I_{EE}$ [$\mu$A] | $\kappa_{rbT}$ | $\kappa_{RC}$ | $\kappa_{RE}$ | $\kappa_{VCO}$ | PREDICTED | MEASURED | ERROR [%] |
| 280 | 3.01 | 1.75 | 0.44 | 0.22 | 3.51 | 3.56 | - 1.3 |
| 470 | 2.33 | 1.04 | 0.26 | 0.22 | 2.56 | 2.57 | - 0.3 |
| 505 | 2.24 | 0.97 | 0.24 | 0.22 | 2.46 | 2.50 | - 1.7 |
| 540 | 2.17 | 0.91 | 0.23 | 0.22 | 2.36 | 2.41 | - 1.9 |
| 570 | 2.11 | 0.86 | 0.22 | 0.22 | 2.29 | 2.37 | - 3.3 |
| 600 | 2.06 | 0.82 | 0.20 | 0.22 | 2.22 | 2.33 | - 4.5 |

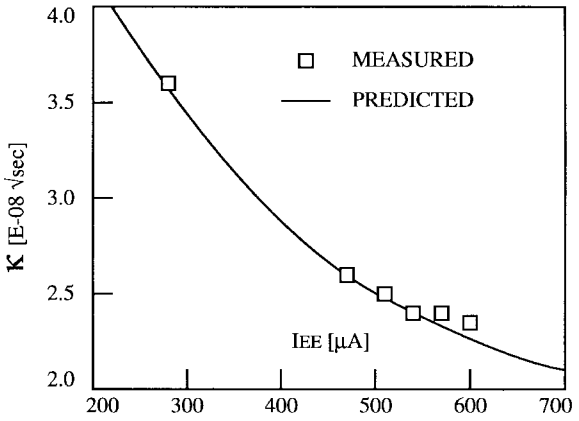


Fig. 6. $\kappa$ versus tail current IEE.

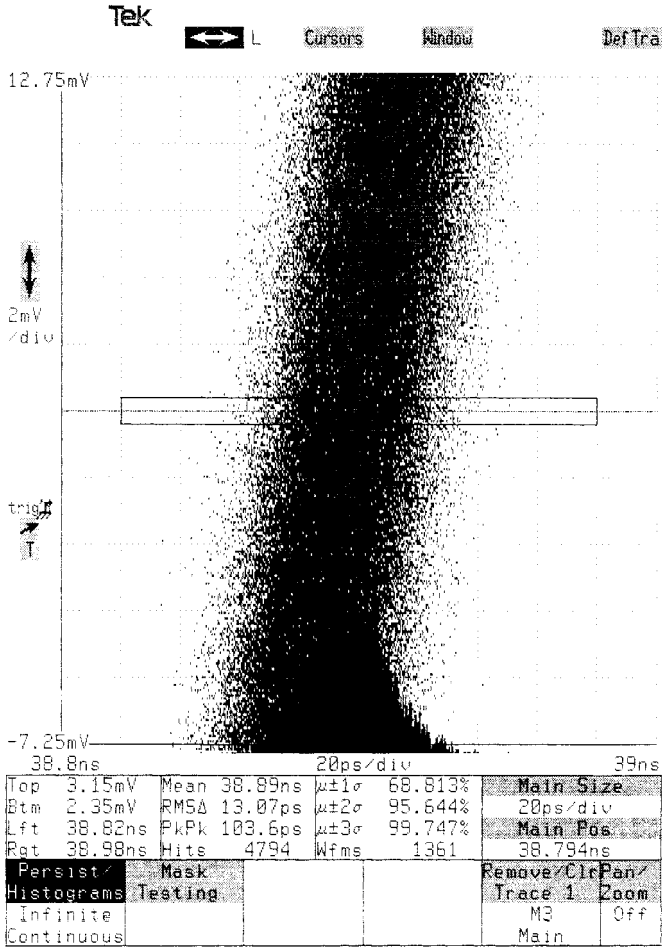


Fig. 7. Measured closed-loop jitter of 622 MHz PLL.

$\sigma_x$ of 13.07 ps rms for the 622 MHz clock recovery PLL with a pseudorandom data input.

## VIII. CONCLUSION

This paper has developed a methodology to guide design of low-jitter, voltage controlled ring oscillators. The key design parameter is the time domain figure-of-merit $\kappa$, which provides the link between circuit-level design and system-level jitter $\sigma_x$. (The design technique can also be related to frequency domain measures [30], which is beyond the scope of this paper.) A key insight of this approach is that jitter performance of a ring, as characterized by $\kappa$, depends primarily on the individual gate and not on the number of gates in the ring or the ring operating frequency. Explicit expressions were developed to provide a simple, direct means of relating jitter performance to fundamental design parameters. Experimental results at 155 and 622 MHz show that system-level jitter can be predicted to an accuracy of order 10%.

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