A Low-Phase-Noise 5-GHz CMOS Quadrature VCO Using Superharmonic Coupling

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***Abstract*—A new concept for quadrature coupling of *LC* oscillators is introduced and demonstrated on a 5-GHz CMOS voltage-controlled oscillator (VCO). It uses the second harmonic of the outputs to couple the oscillators. The technique provides quadrature over a wide tuning range without introducing any increase in phase noise or power consumption. The VCO is tunable between 4.57 and 5.21 GHz and has a phase noise lower than −124 dBc/Hz at 1-MHz offset over the entire tuning range. The worst-case measured image rejection is 33 dB. The circuit draws 8.75 mA from a 2.5-V supply.**

***Index Terms*—CMOS analog integrated circuit, image rejection, injection locking, jitter, oscillators, phase noise, quadrature, voltage-controlled oscillator (VCO), wireless LAN.**

I. Introduction

THE DEVELOPMENT of single-chip CMOS solutions for the 5-GHz 802.11a wireless local area network (LAN) standard is desirable to enable implementations at low cost. The full integration of transceivers implies the use of low intermediate frequency (IF) or zero-IF architectures that require quadrature local oscillator (LO) signals for image rejection and demodulation. Several techniques exist to generate quadrature.

1) A divide-by-two frequency divider following a voltage controlled oscillator (VCO) running at the double frequency. This approach generally shows poor quadrature accuracy, as it requires an accurate 50% duty cycle VCO.
2) A VCO followed by a passive *RC* complex filter. The main drawback of this solution is that a power-hungry buffer is needed between the VCO and the filter [1].
3) Two VCOs forced to run in quadrature by using coupling transistors [2]. This technique suffers from a tradeoff between quadrature accuracy and phase noise. Moreover, the coupling transistors increase the power consumption. The phase-noise penalty can be circumvented by driving the coupling transistors with additional 90° phase shifters [3]–[5]. However, an increase in power consumption remains. It can be avoided by connecting the coupling transistors in series with the transistors that provide the negative resistance, as proposed in [6]. It has been found that the coupling transistors have to be about five times larger than the negative resistance transistors [6], thus loading the oscillator with large parasitic capacitors that reduce the tuning range. This drawback makes this solution unsuitable for wide-band applications.

The solutions proposed so far suffer from an increase in phase noise and/or an increase in power consumption or they result in a limited tuning range, when used at high frequencies of oscillation. This paper presents a fully integrated 5-GHz quadrature CMOS VCO that generates quadrature over a wide tuning range without suffering from an increase in power consumption or phase noise. This technique uses second-order harmonic coupling to enforce the quadrature relation between two oscillators.

The paper is organized as follows. Section II describes the principles of superhamonic-coupled quadrature oscillators. Section III discusses the design issues involved with improving the quadrature accuracy in the presence of mismatches. In Section IV, a comparison is made between the proposed technique and the conventional ring-based quadrature coupling. Section V describes the actual implementation of the 5-GHz CMOS quadrature VCO, and Section VI presents the experimental results. Finally, conclusions are drawn in Section VII.

II. Quadrature Through Superharmonic Coupling

In principle, two differential oscillators can oscillate in quadrature at frequency ω_0 by letting a coupling network enforce an anti-phase relationship between the second-order harmonics. This quadrature oscillator concept has been recently published in [7]–[9]. The following provides a more detailed analysis by first looking at a single differential oscillator.

In the oscillator shown in Fig. 1(a), the common-source signal V_S clamps the output amplitude at high bias currents and the oscillator enters the voltage-limited regime. This clamping occurs since the transistors' drain voltage cannot be lower than the source voltage, as this would reverse the current flow. As is evident from the simulated waveforms shown in Fig. 2(a), the common source voltage of the transistors (V_S) oscillates at $2\omega_0$. This oscillation, which originates from the rectifying action of the two MOS switches, is not aligned optimally with the output waveform. The misalignment is caused by the time delay given by the resistance of the transistor in triode and the tail capacitance. It results in an even stronger clamping of the output waveforms.

Instead, if the tail network is designed to resonate at $2\omega_0$ as shown in Fig. 1(b), the tail impedance is real, so that the minima of V_S align with the minima of the output waveforms V_1 and V_2 [see the plot in Fig. 2(b)]. Since the sinusoids V_1 and V_2 are no longer clamped by V_S, they can reach higher amplitudes. In fact,

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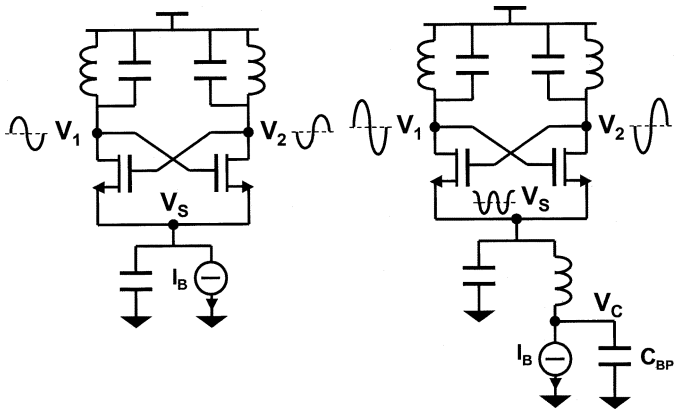


Fig. 1. Differential oscillator. (a) With tail capacitor. (b) With tail resonator.

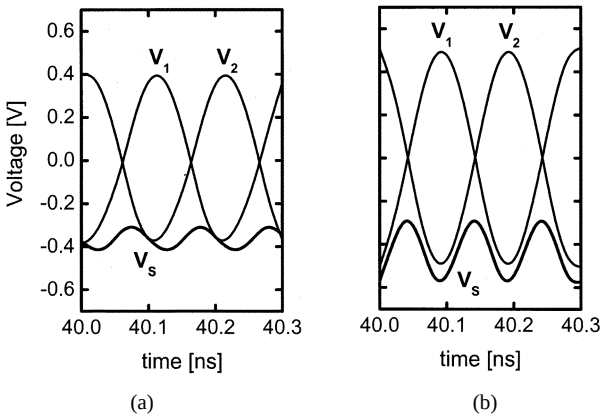


Fig. 2. Simulated waveforms of the output voltages and of the common source voltages of the circuit in (a) Fig. 1(a) and (b) Fig. 1(b).

the oscillator will now operate in the current limited regime. The tail resonator has also beneficial effects on phase noise, as highlighted in [10].

Two oscillators like the one of Fig. 1(b) can be coupled by removing the bypass capacitor $C_{\rm BP}$ and connecting the respective nodes (C) as depicted in the circuit in Fig. 3. It can be shown that this circuit has two oscillation modes: the outputs may run either in quadrature or in phase.

The impedance of the tail network between the nodes (S_1)–(S_2) and ground depends on the relative phase between V_{S1} and V_{S2}. If these voltages run in anti-phase, (C) is a balanced node and each of the two oscillators behaves like the oscillator of Fig. 1(b). With the second-order harmonics being in anti-phase, the output waveforms of the two oscillators must be in quadrature. We will refer to this mode as the *odd mode*. Instead, if V_{S1} and V_{S2} are in-phase, no ac-current flows in the tail inductors, and each of the two oscillators behaves like the one in Fig. 1(a). This implies that the outputs V_1 and V_3 oscillate in-phase as well. We will refer to this mode as the *even mode*.

Since we are interested in generating oscillations in quadrature, we need to select the odd mode. This automatically happens if the coupled oscillators are driven at high bias currents. In this condition, the even-mode equivalent circuit in Fig. 1(a) works in the voltage limited regime, while the odd-mode equivalent circuit in Fig. 1(b) works in current limited regime. Therefore, the even-mode amplitude is lower than the odd-mode one. The loop nonlinearity selects the mode with higher oscillation amplitude. In fact, simulations show that only the odd mode prevails. Fig. 4 depicts the initial transient of the coupled oscillators when they are forced to start in phase. The plots show the differential amplitude, the oscillation frequency, and the phase difference between the two oscillator outputs as a function of time. As expected, at the beginning of the transient, the oscillation amplitude is identical to that of the circuit in Fig. 1(a) and the outputs run in phase. The oscillation frequency is lower than the tank resonance frequency (about 5 GHz), since in the even mode, the tail capacitance is seen in parallel to the tank [11]. After the simulator's numerical inaccuracy creates a slight asymmetry, the phase difference between the outputs changes. At steady state, the amplitude of both oscillators reaches that of the circuit in Fig. 1(b) and the outputs run in quadrature. The final oscillation frequency is set only by the tank resonance and it is not altered by the coupling.

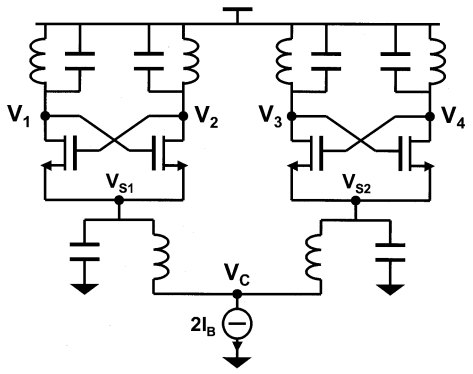


Fig. 3. Superhamonic-coupled quadrature oscillator.

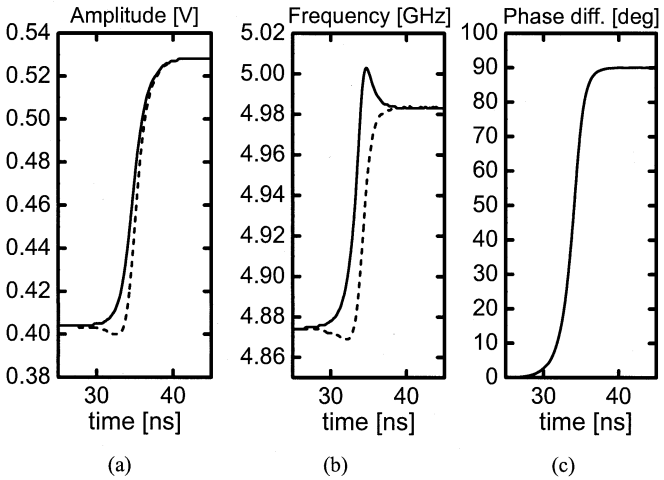


Fig. 4. Start-up transients of the superharmonic-coupled oscillator in Fig. 3. (a) Output amplitudes of the two oscillators. (b) Oscillation frequencies. (c) Relative phase between the two oscillators.

III. Effect of Mismatches on Quadrature Accuracy

Oscillators are known to be able to lock their frequency of oscillation to the frequency of an injected harmonic. In the differential oscillator of Fig. 1(b), the frequency of oscillation can depart from its natural value if a tone at a frequency close to

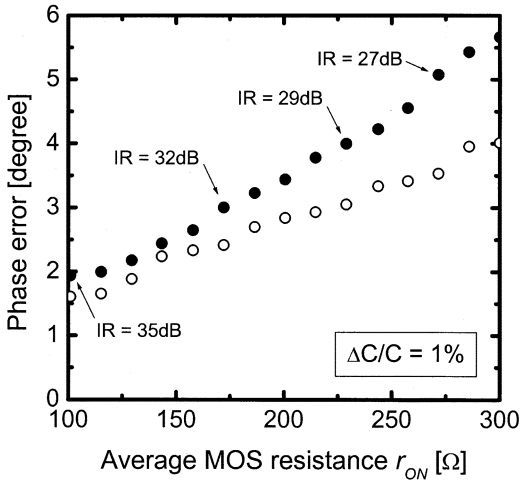


Fig. 5. Simulated phase error of the quadrature oscillation as a function of the MOS on-resistance $r_{\rm ON}$ for $R_{\rm tail} = 500\ \Omega$ (filled circles) and for $R_{\rm tail} = 500$ kΩ (hollow circles), given 1% tank capacitor mismatch.

twice the natural frequency is injected into the tail of the circuit [12].

A similar process takes place in the two quadrature-coupled oscillators in the case of mismatches. Due to mismatches, the two coupled oscillators have slightly different resonant frequencies ω_{r1} and ω_{r2}. When coupled, they will eventually oscillate at a common frequency ω_0 through a process called injection locking [13], [14], if the frequency difference $(\omega_{r1}-\omega_{r2})$ is relatively small. This process can be qualitatively described as follows: the second harmonic $2\omega_{r2}$ injected into the tail of the first oscillator, running at ω_{r1}, beats with ω_{r1} and results in a sinusoid at $(2\omega_{r2}-\omega_{r1})$, which is slightly higher than ω_{r1}. This will cause the first oscillator to increase its frequency of oscillation toward ω_{r2}, a sub-harmonic of the injected signal. At the same time, an analogous injection-locking phenomenon takes place in the other oscillator, which tends to decrease its frequency toward ω_{r1}. Finally, the frequency locks to a common value. Since both oscillators operate slightly off-resonance, they need to accommodate for a small phase delay between the output voltage and the current signal injected into the tank. As a result, some phase error occurs between the quadrature outputs and a small even-mode oscillation at $2\omega_0$ appears.

A mismatch between the tank capacitors of the two coupled oscillators has been applied and the circuit has been simulated. The tank resonance frequency is about 5 GHz and its quality factor is 10, giving a parallel resistance of 1 kΩ. The tail resonator is centered at 10 GHz and has a quality factor of 10, featuring a parallel resistance $R_{\rm tail}$ of 500 Ω. Since the transconductors' transistors work in the triode region for most of the time, we can calculate an average on-resistance $r_{\rm ON}$, which is about 100 Ω. The resulting oscillation frequency is about the average of the two tank resonance frequencies. The quadrature error is about 2° for a tank capacitor mismatch of 1%.

We also varied $r_{\rm ON}$ from 50 to 300 Ω by changing the transistors' width. The phase error for 1% tank mismatch is plotted in Fig. 5, for two values of the tail resonator's parallel resistance $R_{\rm tail}$ (500 Ω and 500 kΩ). That figure shows that, over a wide range, the phase error decreases linearly with $r_{\rm ON}$. It also shows that the phase error decreases with higher tail resonator impedance, but this dependency is not as pronounced as the dependency on $r_{\rm ON}$. For values of $r_{\rm ON}$ higher than 300 Ω, the oscillators loose lock. This behavior can be understood intuitively. With increasing values of $r_{\rm ON}$, the dc level of V_{S1} and V_{S2} lowers with respect to the dc level of the output nodes. Consequently, the amplitude of the even-mode oscillations at V_{S1} and V_{S2} (that results from the mismatch) can grow larger, before experiencing the clamping effect. This will give rise to a higher quadrature phase error until ultimately, the oscillators loose lock.

IV. Ring-Based Quadrature Coupling Versus Superharmonic Coupling

In quadrature LC oscillators based on a ring structure, the frequency of oscillation can differ from the resonance frequency of the individual tanks. Since the tank is no longer operating at the frequency where the impedance is the highest and the phase characteristic is the steepest, the oscillation amplitude and the phase stability are reduced and the phase noise increases [4]. In addition to that, the oscillator becomes more sensitive to the flicker noise of the coupling transistors [15].

In the presented superharmonic-coupled VCO, the quadrature coupling does not require the oscillation frequency to deviate from the tank resonance. Consequently, the coupling does not reduce the phase stability of each individual oscillator and no phase noise increase is seen. Moreover, since the quadrature coupling is established by means of coupled inductors rather than by transistors, the coupling elements introduce no significant extra sources of noise.

In order to prove that no phase noise penalty exists, simulations have been performed on both a single oscillator with tail resonator [circuit in Fig. 1(b)] and a quadrature oscillator as in Fig. 3. The simulated phase noise of the single oscillator is -124 dBc/Hz at 1-MHz offset, which is compatible with the limited quality factor $Q = 10$ of the inductors. The quadrature-coupled oscillator has a phase noise 3 dB lower than that of the single oscillator. This improvement is obtained at the expense of double the current consumption. The 3-dB improvement in phase noise is a result that is commonly encountered in the case of two bilaterally coupled oscillators [14]. Theoretically, one could of course double the current in a single oscillator, achieving a 3-dB improvement in phase noise, as long as the circuit can accommodate the increase in amplitude. When normalized to power consumption, the phase noise simulation effectively shows that no degradation in phase noise occurs when two oscillators are coupled in quadrature by means of a $2\omega_0$ odd-mode resonant network.

V. Circuit Implementation

Fig. 6 shows the circuit schematic of the realized quadrature oscillator. The circuit consists of two separate differential oscillators whose common-mode second-order harmonics are coupled by the inductor pair $L_{5,6}$. They are dimensioned such that they resonate with the parasitic capacitance at a frequency $2\omega_0$ when driven in the odd mode. This gives rise to high odd-mode impedance at frequency $2\omega_0$. The even-mode

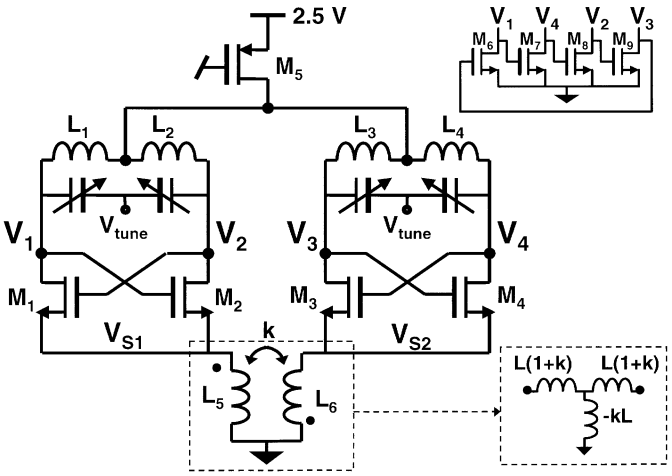


Fig. 6. Actual circuit implementation of the superharmonic-coupled quadrature VCO.

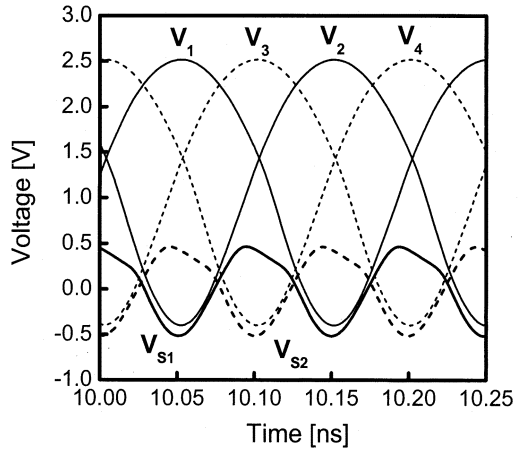


Fig. 7. Simulated waveforms of the output voltages and of the common source voltages of the circuit in Fig. 6.

resonance occurs at a frequency higher than $2\omega_0$, and thus the even-mode impedance at frequency $2\omega_0$ is much lower. This ensures that the circuit exhibits a strong "preference" for quadrature oscillation, as explained in Section II. The difference between the even- and odd-mode resonance frequencies of the tail-network follows from the T-equivalent network of the coupled inductors shown in the inset in Fig. 6. It shows that the differential inductance of the two coupled inductors is larger than the common-mode inductance.

Transistor M_5 supplies the bias current from the top-side of the circuit (different from the simplified model of Fig. 3), such that a rail-to-rail oscillation waveform is possible without exceeding the breakdown limits of transistors $M_{1\text{-}4}$. It also allows for plenty of voltage headroom for M_5, such that its current noise can be made low.

Fig. 7 shows the four simulated quadrature output waveforms, along with the source voltages V_{S1} and V_{S2}. It shows that the gate-source and drain-source voltages of transistors $M_{1\text{-}4}$ periodically reach a value close to zero. As a result, the $1/f$ noise of transistors $M_{1\text{-}4}$ is reduced [16].

Transistors $M_{6\text{-}9}$ in Fig. 6 are minimum size devices (2.2/2.2) that are added to give directivity to the quadrature phases.

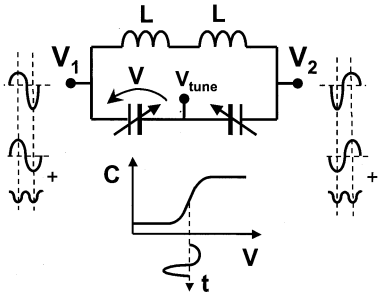


Fig. 8. MOS varactor in a resonator gives rise to an oscillation waveform containing a strong second-order harmonic component.

Without them, the oscillator would have no distinct preference for oscillation at either $+90^\circ$ or -90° phase difference. The current flowing through $M_{6\text{-}9}$ is negligible compared to the current in the transistors $M_{1\text{-}4}$, as their (W/L)'s are less than 1% of that of $M_{1\text{-}4}$ (whose W/L equals 32/0.24).

Apart from the transistors $M_{1\text{-}4}$, also the varactors contribute to the second-order harmonic oscillation at the common nodes (S_1) and (S_2). The varactors are accumulation/depletion pMOS devices: they exhibit a step-like $C(V)$ curve with maximum capacitance at high gate-to-well voltages. Fig. 8 shows the $C(V)$ curve of the varactor, along with a single-ended waveform, that is distorted by the varactor. When the single-ended waveform that drives the gate of the varactor is high, the associated varactor capacitance is high and the oscillation waveform "slows down" and flattens. When the voltage is low, the capacitance is low and the waveform "speeds up" and sharpens. This gives rise to a second-order harmonic that shows up as a common-mode signal [17]. Like the second-order harmonic due to $M_{1\text{-}4}$, the maxima of this second-order harmonic align in-phase with the zero crossings of the fundamental, as shown in Fig. 8. Thus, the distortion introduced by the varactors effectively adds to the quadrature coupling.

The inductors L_1 and L_2 in Fig. 6 are deliberately not combined into a single symmetrical inductor (the same holds for L_3 and L_4) but rather each inductor is implemented separately. A symmetrical inductor exhibits a larger quality factor when driven differentially [18]. This would result in a larger suppression of the common-mode second-harmonic, which is instead beneficial for maximizing the quadrature coupling in this topology.

The proposed quadrature VCO is realized in Agere Systems' 0.25-μm CMOS process. The inductors are laid out in the top three Al-metal layers of this five metal-layer process. Although the process has the option to use a thick metal-5 layer, only regular-thickness metal layers were used. An in-house electromagnetic simulator (IES^3) is used to model all inductors.

Fig. 9 shows a photograph of the chip. The four inductors $L_{1\text{-}4}$ of the oscillator core are in the center of the figure. They have a simulated inductance of 1.8 nH and a quality factor of 9 at 5 GHz. The coupled inductors $L_{5,6}$ are laid out as a center-tapped symmetrical inductor (see the left-hand side of Fig. 9). This inductor is intentionally placed relatively further from the core, so as to minimize parasitic coupling to the other inductors. Its relatively long connecting leads are also included in the electromagnetic simulation. The two coupled inductors have a

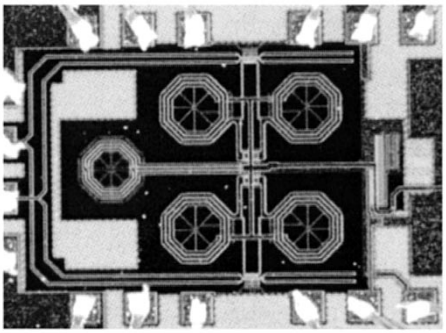


Fig. 9. Chip photograph.

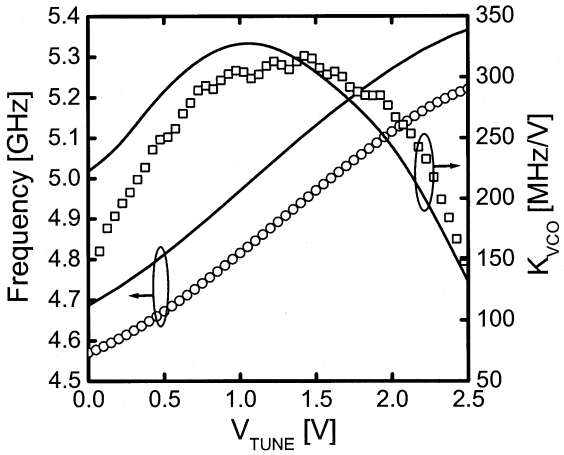


Fig. 10. Simulated (solid lines) and measured (dots) tuning curve and tuning sensitivity.

simulated inductance of 0.62 nH each and a coupling coefficient k of 0.55 at 10 GHz. The circuit also includes a set of in-phase and quadrature (I/Q) mixers, used for quadrature accuracy measurements to be discussed in the next section. The layout is highly symmetrical. All ground currents combine in one point in the center of the oscillator layout and go from there through a single path to the ground bondpads. The supply is decoupled by means of on-chip capacitors.

VI. Experimental Results

Fig. 10 shows both the simulated and measured tuning curves. The shapes of the two curves are nearly identical. The measured tuning curve is offset only by about 100 MHz with respect to the simulated one. This is most likely due to inaccuracies in the estimated stray capacitances. The oscillator is tunable between 4.57 and 5.21 GHz (13% tuning range). The maximum and minimum values of $K_{\rm VCO}$ are within a $\pm 35\%$ range of the average value of 233 MHz/V. The relatively constant $K_{\rm VCO}$ is due to the large signal amplitude, which effectively averages the steep $C(V)$ curve of the varactor [19], [17]. A constant $K_{\rm VCO}$ is beneficial for PLL design, since it gives a constant loop gain and thus does not require dynamic adjustment of the charge pump current.

Fig. 11 shows a plot of the phase noise at oscillation frequency of 4.88 GHz. It measures -125 dBc/Hz at 1-MHz offset from the carrier. At offset frequencies larger than about 2 MHz,

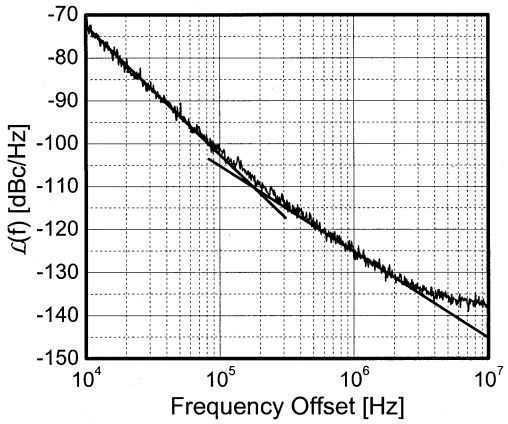


Fig. 11. Measured phase noise spectrum.

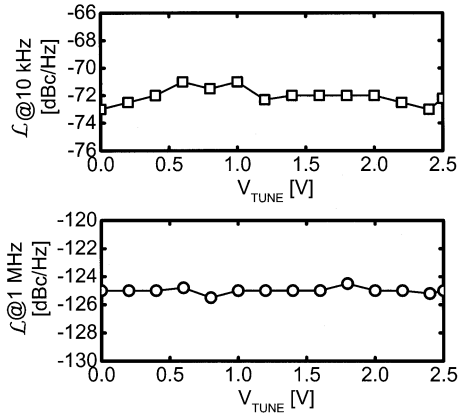


Fig. 12. Measured phase noise at 10-kHz and at 1-MHz offset from the carrier over the oscillator tuning range.

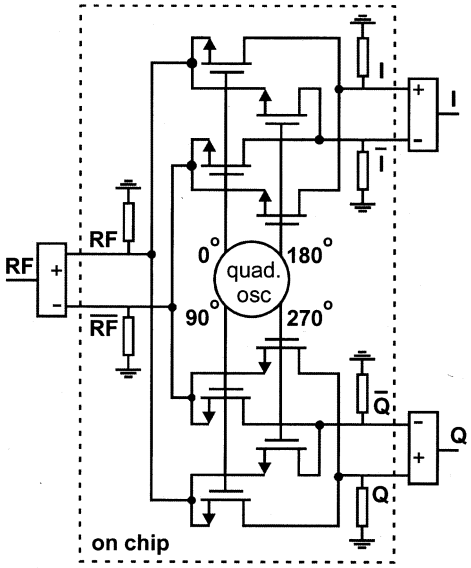
TABLE I
Comparison of the Quadrature Oscillator Performance Against Prior Art

Ref.	f_{osc} [GHz]	P [mW]	FOM
[3]	1.88-1.98	27	178
[4]	4.91-5.23	21	168
[5]	1.36-1.66	30	181
[19]	1.77-1.99	20	185
[6]	1.64-1.97	50	178
This work	**4.60-5.20**	**22**	**185**

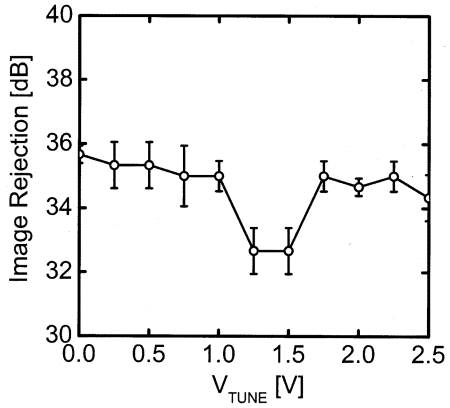
the measured phase noise is limited to -140 dBc/Hz by the noise floor of the measurement setup.

Fig. 12 shows the measured phase noise along the entire tuning range, for offset frequencies of both 10 kHz (flicker noise dominated) and 1 MHz (white noise dominated). Both the $1/f^3$ and $1/f^2$ phase noise are remarkably constant over the tuning range. The worst-case noise levels are -71 dBc/Hz at 10 kHz and -124.5 dBc/Hz at 1 MHz. Table I shows a comparison of the achieved figure of merit (FOM) [20] to that of other published quadrature oscillators. All FOMs are calculated from the worst-case phase noise.

In order to measure the quadrature accuracy, the integrated circuit includes a set of in-phase/quadrature (I/Q) mixers, driven by the quadrature VCO. Accurate incoming baseband I and Q 2.5-MHz tones are single-sideband upconverted by



(a)



(b)

Fig. 13. Setup for (a) image rejection measurement and (b) measured image rejection of the quadrature mixer-VCO over the tuning range.

the I/Q mixers to one sideband of the oscillator. Due to inaccuracies in amplitude and quadrature caused by mismatches in oscillator and mixers, some energy will leak into the other sideband. The ratio between the two sidebands is measured with a spectrum analyzer at the radio frequency (RF) port; this ratio represents the image rejection (in decibels). Fig. 13(a) shows the image-reject mixer circuit. The circuit uses external power splitters and combiners to convert from single-ended to differential and vice versa. The differential I and Q baseband signals entering the chip have an image rejection better than 45 dB, measured with a vector analyzer. The image rejection of the chip has been measured over several samples. Fig. 13(b) shows the mean value of the image rejection along with the standard deviation; the mean is better than 33 dB over the tuning range.

This image rejection can be limited by both amplitude and phase errors. In order to measure the amplitude imbalance between the two paths, we applied alternatively only the I or the Q input and measured the output signal at the RF port. The amplitude imbalance is smaller than 0.1 dB over all chips and it would limit the image rejection to about 38 dB. Thus, we can assume that solely the phase inaccuracy between the two paths is responsible for the image rejection performance. The estimated quadrature phase error is smaller than 2.6°.

It should be noted that the matching between the on-chip I and Q mixers is not optimal in the current layout of the chip, as can be seen in the die photograph (see Fig. 9): the I mixers (above the VCO) are placed far from the Q mixers (below the VCO).

VII. Conclusion

A new quadrature-coupling concept has been analyzed and implemented. In the proposed scheme, two oscillators are injection locked in quadrature by coupling their second-order harmonics in anti-phase, using a coupling network that exhibits high odd-mode and low even-mode impedance. The advantages over conventional ring-based quadrature oscillators have been discussed. A 0.25-μm CMOS 5-GHz quadrature VCO demonstrates the proposed concept, using common-mode inductive coupling. The coupling network introduces no increase in phase noise or power consumption. The circuit features a measured phase noise lower than -124 dBc/Hz at 1-MHz offset over the 4.57–5.21-GHz tuning range at 22-mW power consumption. The worst-case image rejection is 33 dB.

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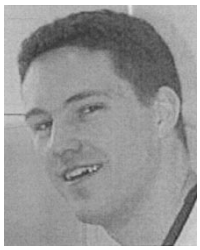

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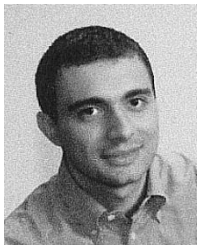

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