RF Transceiver Electronics

Course # 5/10

LNA circuit topologies and design

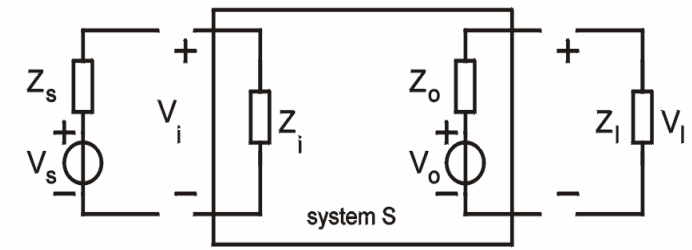
5TT40

Johan van der Tang,
28 February 2005

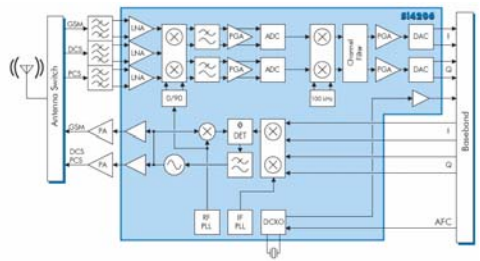
j.d.v.d.tang@tue.nl

Mixed-signal
Microelectronics
Group

Previous and next lecture

- **Last course:** Spec. and system design (II)
- 

- **Next course:** Invited Lecturer Arjan Leeuwenburgh (National Semiconductor: DECT transceiver design in the real world



- **This course:** Low noise amplifiers

Content lecture #5/10

- Introduction
- Specifications
- Matching issues in a LNA
- LNA circuit topologies
  - Common-source LNA
  - Common-gate LNA
  - Common-emitter LNA
  - Common-base LNA
- Example of LNA dimensioning
- Other LNA topologies
- Typical LNA performance
- Appendix
  - ADS simulation example of a common-source cascode LNA
  - Component quality factor

Course slides are downloadable at

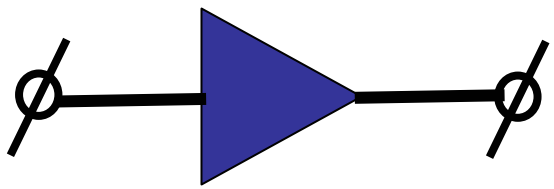
http://www.msm.ele.tue.nl/~jvdtang/homepage

Introduction

Main function of a LNA

- Normally the first active building block in a receiver

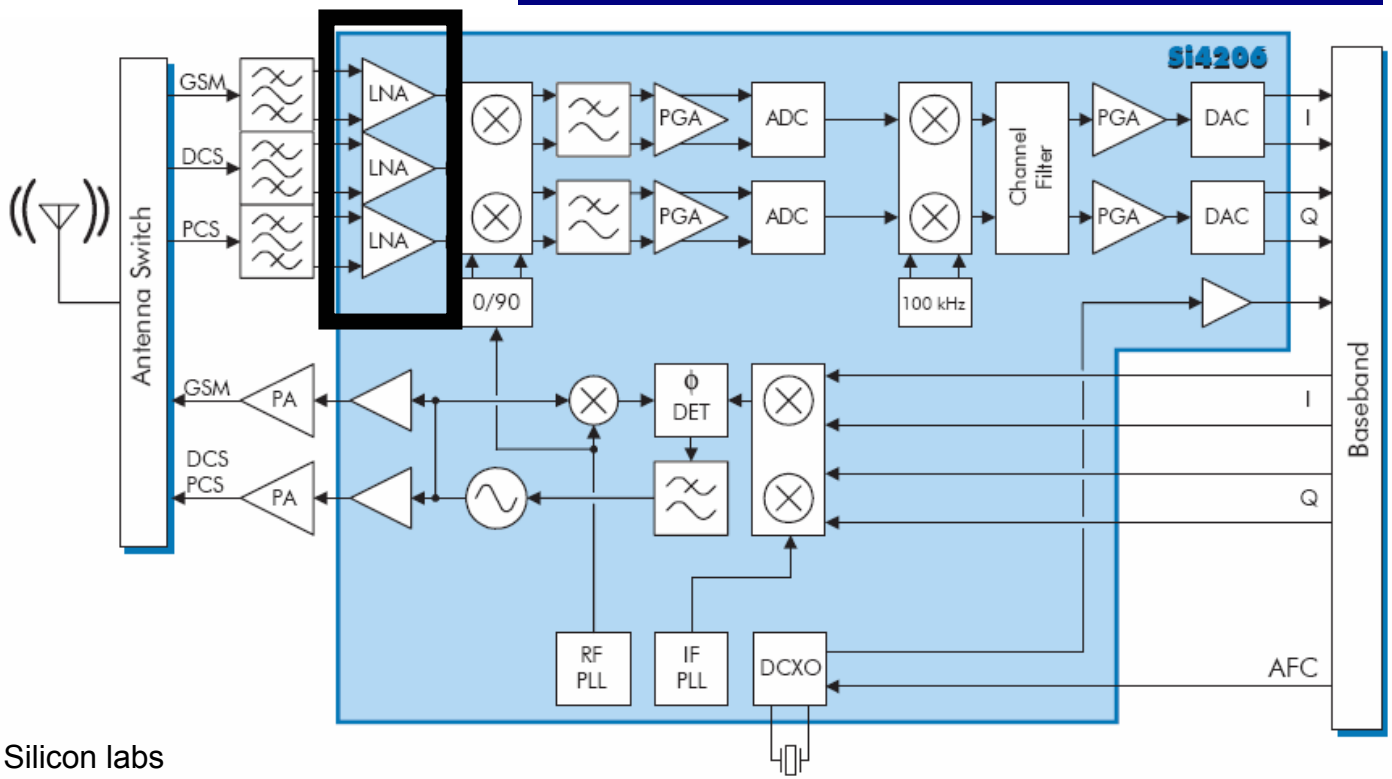
Low noise amplifier



The LNA must increase the often weak antenna signal, while hardly deteriorating the signal-to-noise ratio. Because of large unwanted signals, or because of a strong (amplitude-modulated) desired signal, it also must have a good linearity (IIP3).

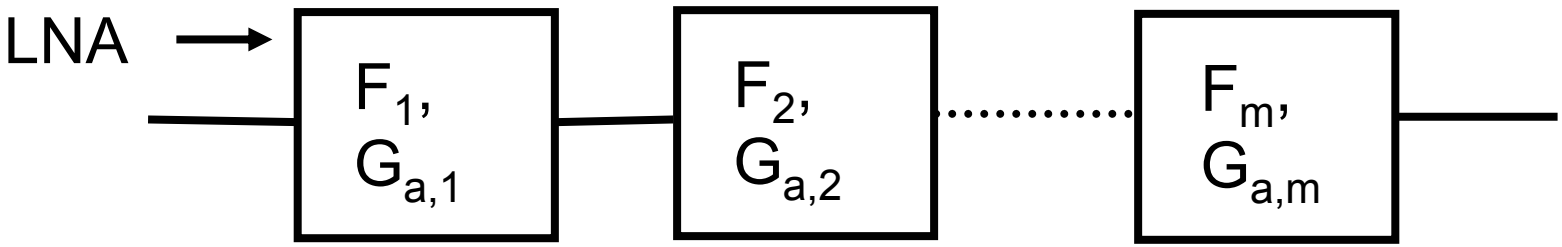
The LNA in a transceiver

As much gain as possible with the lowest possible noise figure



Source: Silicon labs

Friss formula shows the importance of the LNA

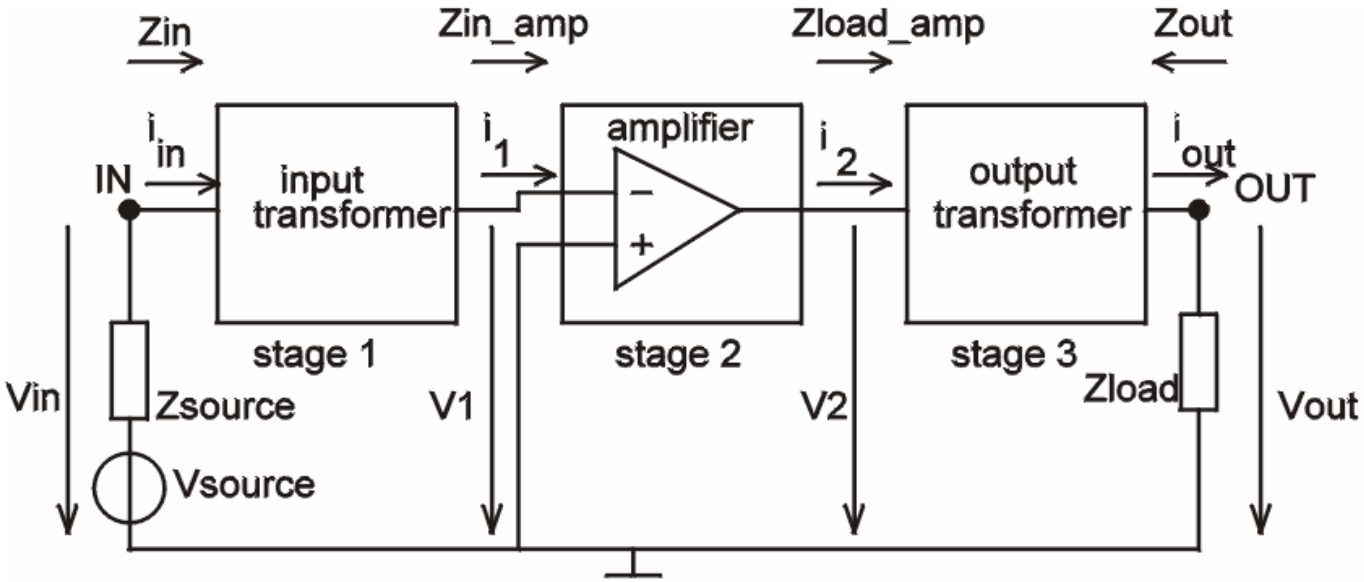


System with cascaded sub-systems with noise figure F_m and available gain $G_{a,m}$

$$F_{total} = 1 + (F_1 - 1) + \frac{F_2 - 1}{G_{a,1}} + \ldots + \frac{F_m - 1}{G_{a,1} G_{a,2} \ldots G_{a,(m-1)}}$$

The noise figure F of the first stage (the LNA) is dominant when the gain of each stage is reasonable.

Break-down of LNA into a cascade of three stages

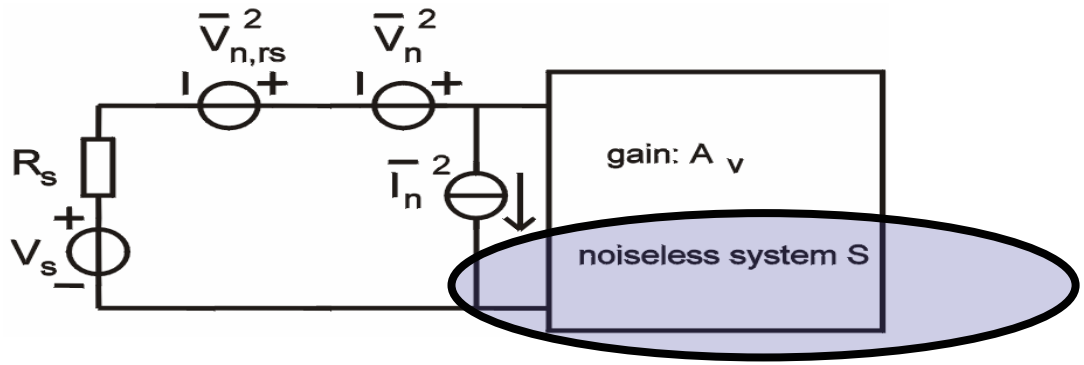


1st stage: Input matching stage for optimum gain and/or NF.
2nd stage: Actual LNA (one transistor or several stages).
3rd stage: Impedance matching stage to output impedance.

Specifications

Important specifications for LNAs (I)

- NF

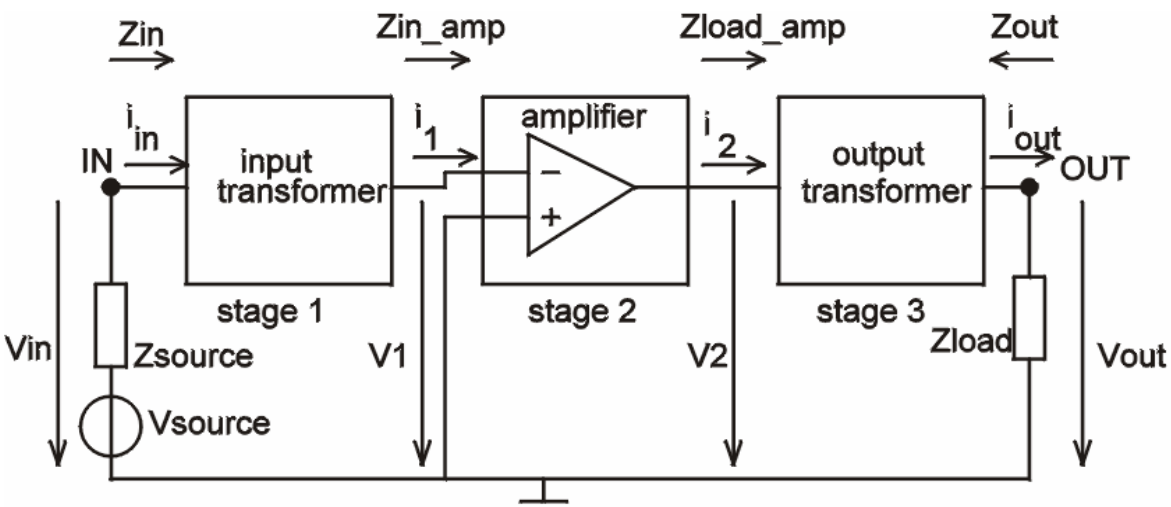


$$F = 1 + \frac{\overline{(V_n + R_s I_n)^2}}{\overline{V_{n,rs}^2}}$$

When F is taken in 1 Hz:
spot noise figure

Important specifications for LNAs (II)

- Gain



$$A_v = \frac{V_2}{V_1}$$

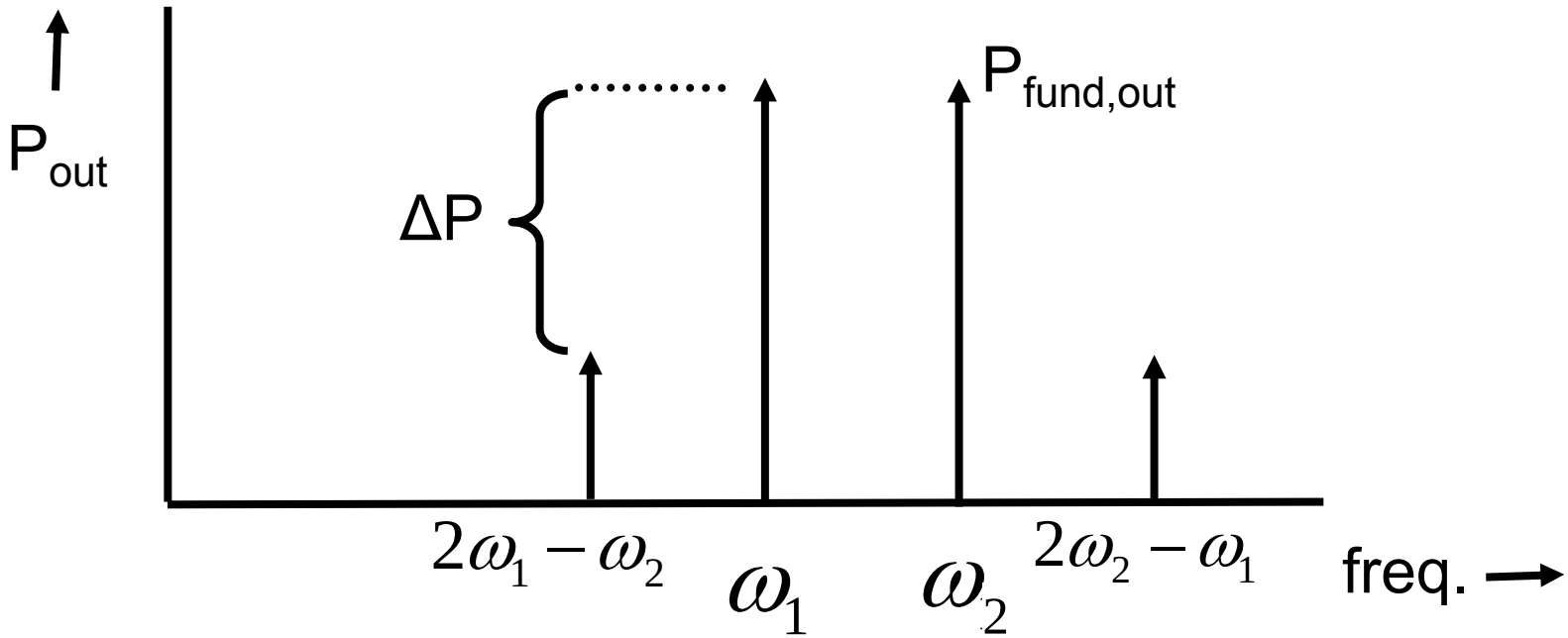
Voltage gain, no losses due to input transformer take into account

$$G_p = \frac{P_{l,del}}{P_{i,del}} = \frac{P_{load}(real)}{P_{in}(real)} = \frac{real(v_{out} \cdot i_{out}^*)/2}{real(v_{in} \cdot i_{in}^*)/2}$$

Power gain

Important specifications for LNAs (III)

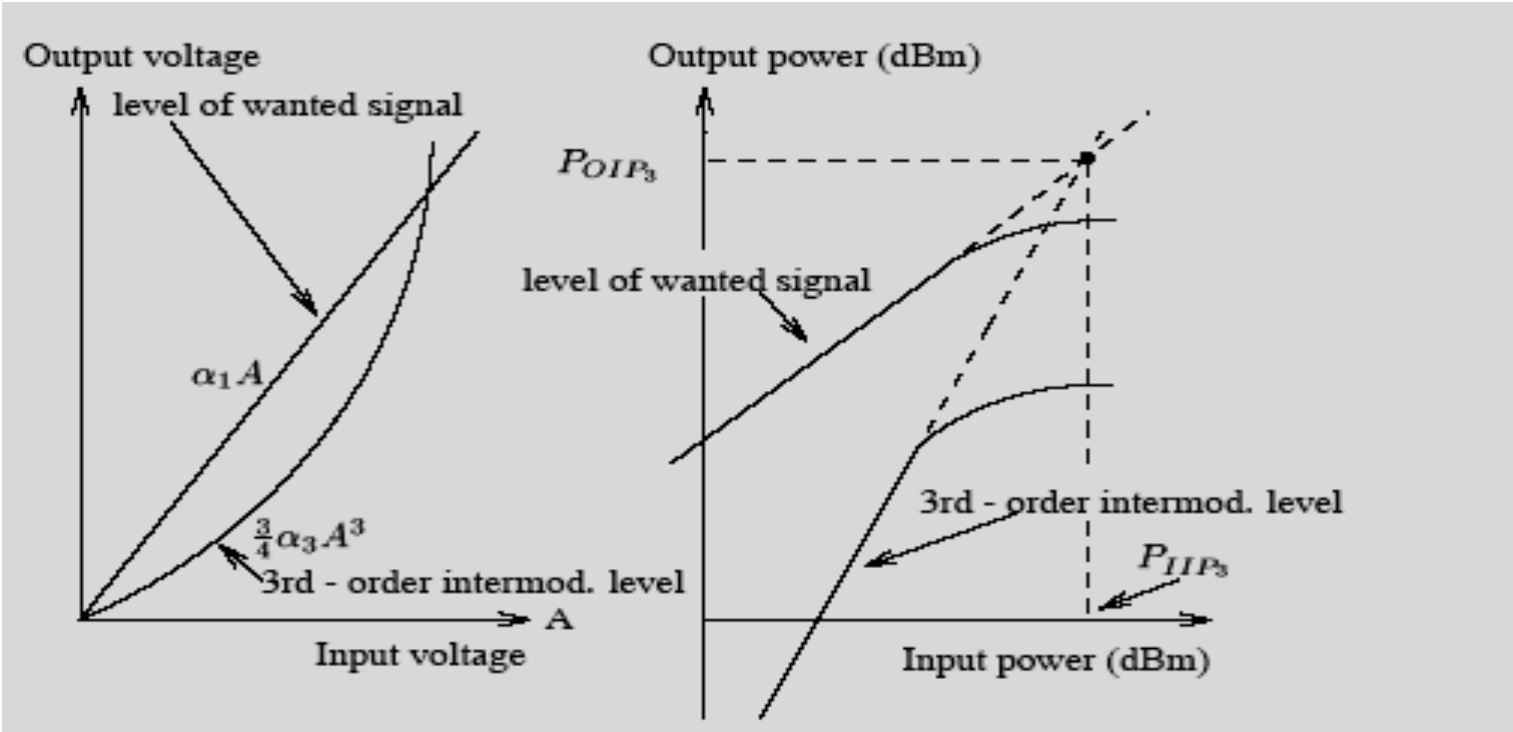
- IP3



$$OIP_3 = P_{fund,out} + \frac{\Delta P}{2} \quad \text{(dBm)}$$

Important specifications for LNAs (IIII)

- IP3 measurement (and 1 dB compression point)



Important specifications for LNAs (V)

- Return loss $20 \cdot \log(\Gamma_s)$

with $$\Gamma_s = \frac{Z_s - Z_o}{Z_s + Z_o}$$

Z_o is the characteristic impedance (often the source impedance is equal to Z_o)

For a perfect output match: $\Gamma_s = S_{11}$

A related measure is the standing wave ratio (VSWR): $$\frac{1+|\Gamma_s|}{1-|\Gamma_s|}$$

Return loss example

$$\Gamma_s = \frac{Z_s - Z_o}{Z_s + Z_o}$$

Assume Z=R + ΔR in a 50 Ω system (i.e. Z_o=50Ω)

A ΔR of 20% results in a return loss (20log(Γ)) of -20.8 dB. In other words about 1% of the power is reflected back. The VSWR is in this case 1.2

There will be no reflection for a perfect match. In that case the VSWR will have its minimum value of one.

Stability

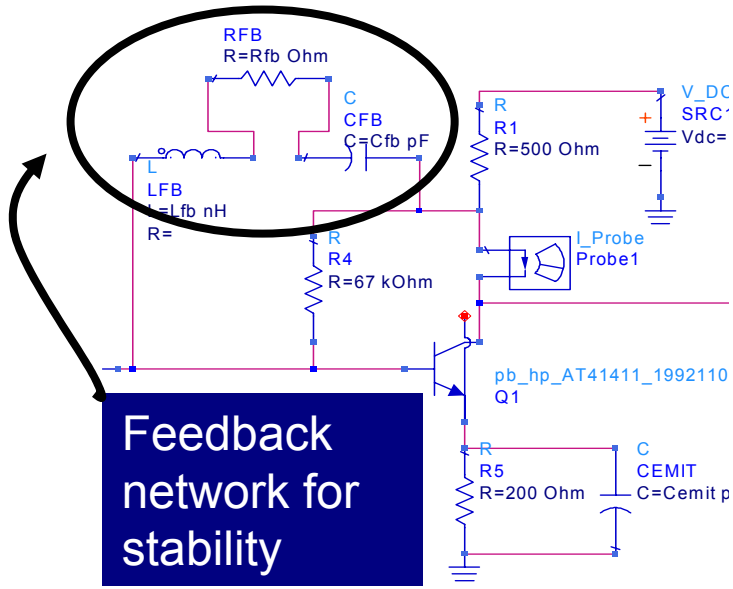
- Stern stability factor (worst case, a real output impedance is often sufficient: stability for any combination of source and load impedances):

$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|}$$

With $\Delta = S_{11}S_{22} - S_{12}S_{21}$

The LNA is unconditionally stable if K>1 and |Δ|<1

Stability increases if S_{12} (the reverse isolation) is improved, e.g. by tuning out the feedback capacitance or cascoding

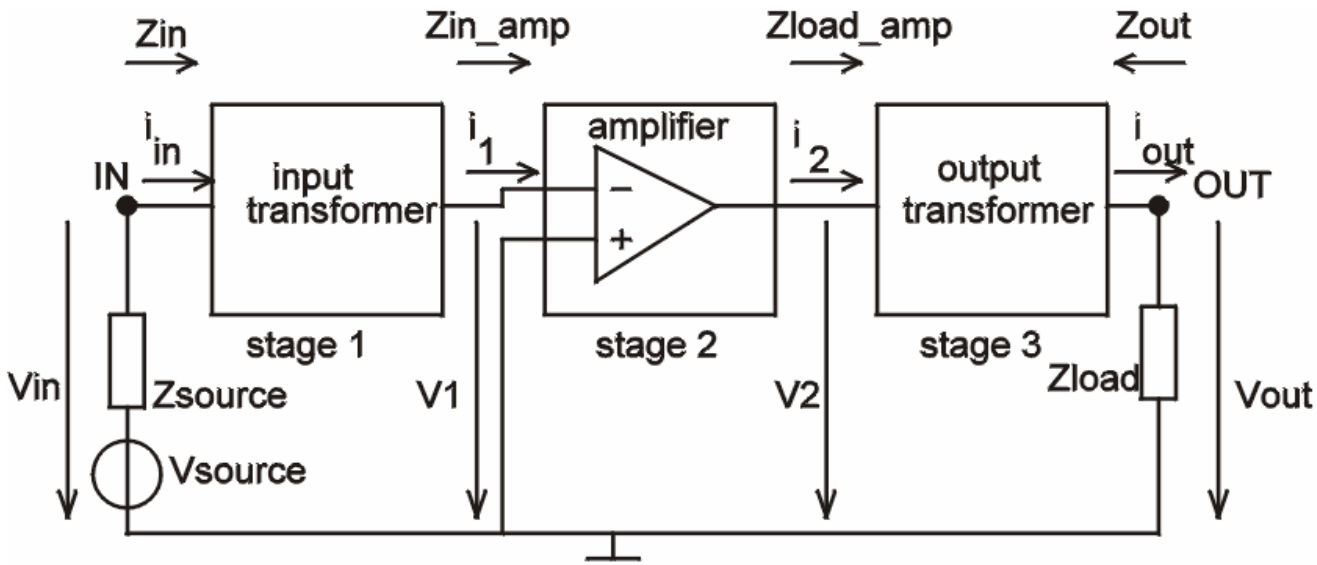


Other important specifications / and issues

- Power dissipation (mW)
- Chip area (um^2) (number of coils)
- Influence of IC package
- Influence of bondpads with ESD
- Robustness against process spread
- Robustness against temperature variations

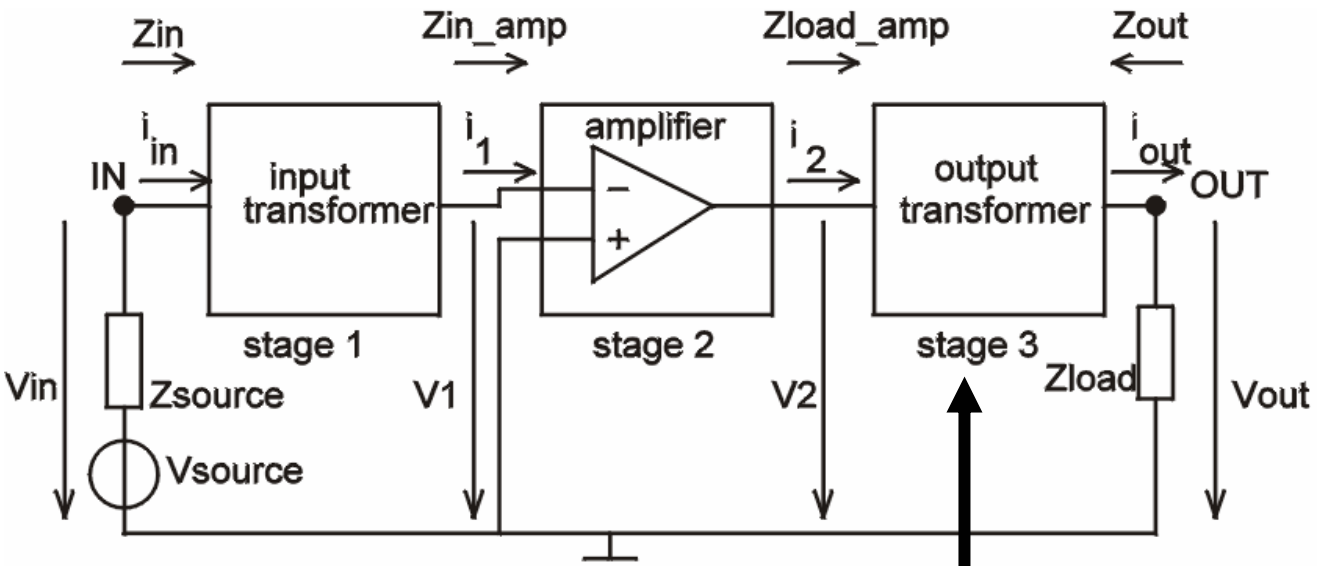
Matching issues in a LNA

Input match important for gain and noise



The goal of matching is to achieve a minimum noise figure, maximum gain and acceptable return loss. Often conflicting specs and not achieved for the same input matching network.

Output match normally on chip not required



When distances are small enough on the IC, no output match is required

When the LNA must drive a 50Ω off-chip filter (e.g. super-heterodyne architecture), then an output match is desired.

Tools for assessing noise and power match

- Constant gain circles
- Constant NF circles

Beyond the scope of this (broader transceiver design) course to explain working with constant gain circles, constant NF circles and stability circles in the smith chart.

Good reference for this: “Microwave Transistor Amplifiers”, Guillermo Gonzalez, Prentice Hall, ISBN 0-13-254335-4

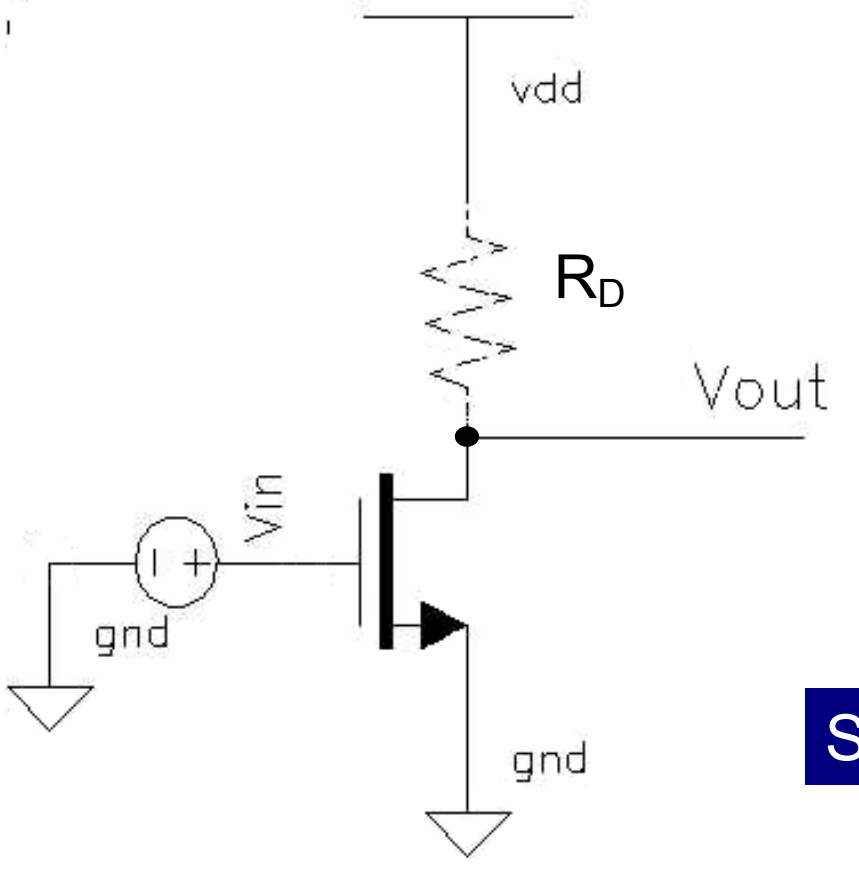
LNA circuit topologies

KISS-principle

- KISS-principle”
  - “keep it simple,…….stupid”
- In general true for all RF circuits: more components: more parasitics….
- Especially true for LNAs: more components : more parasitics and…. more noise (when they are in the signal path)

Common source topology

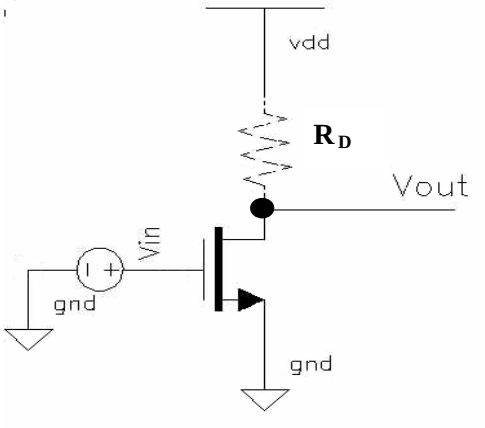
Common source topology



This is the basic topology: no input matching, or emitter degeneration

Source is grounded

Calculation of the small-signal gain



If the NMOS operates in saturation, the drain current can be described by:

$$I_D = \frac{\mu_n C_{ox} W}{2L}\left(V_{GS} - V_{TH}\right)^2$$

if $V_{DS} \geq \underbrace{V_{GS} - V_{TH}}_{V_{gt}}$

Device must be in saturation

Large signal analysis:

$$V_{out} = V_{DD} - I_D R_D$$

Combining above equations, the gain of the common source LNA can be calculated:

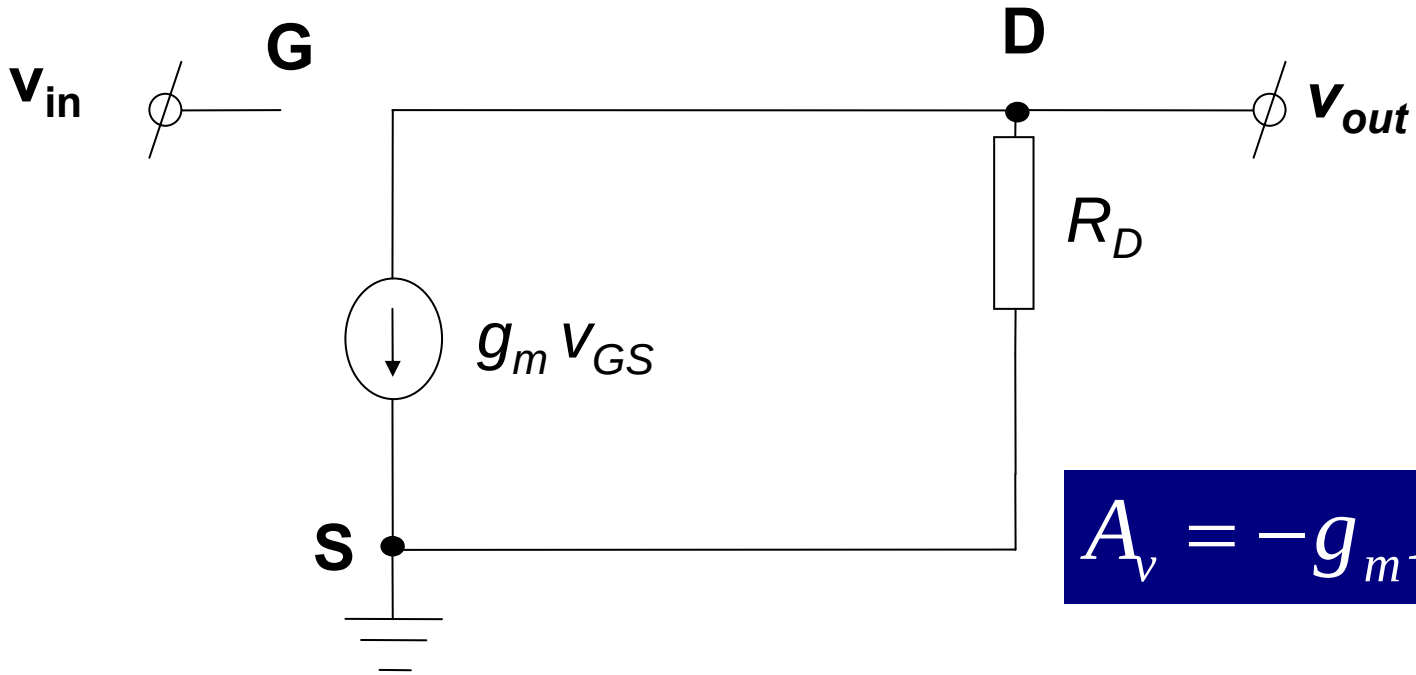
$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = -\mu_n C_{ox} \frac{W}{L} R_d \left(V_{in} - V_{TH}\right)$$

With

$$g_m = \mu_n C_{ox} \frac{W}{L}\left(V_{in} - V_{TH}\right)$$

$$A_v = -g_m R_d$$

Gain calculation with small-signal model



$$A_v = -g_m R_d$$

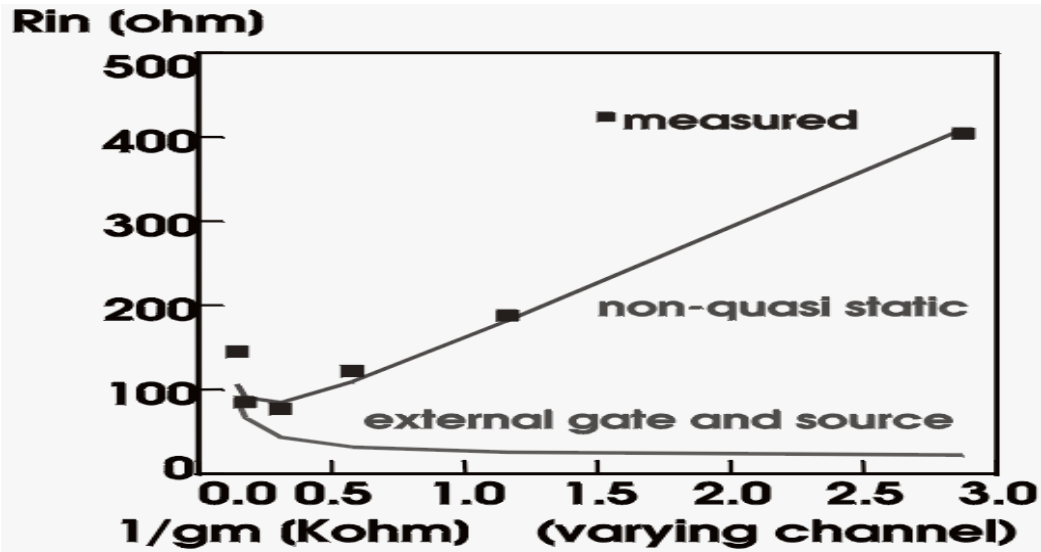
Channel length modulation, body effect, substrate node and parasitic capacitance are (among other things) neglected.

Input impedance

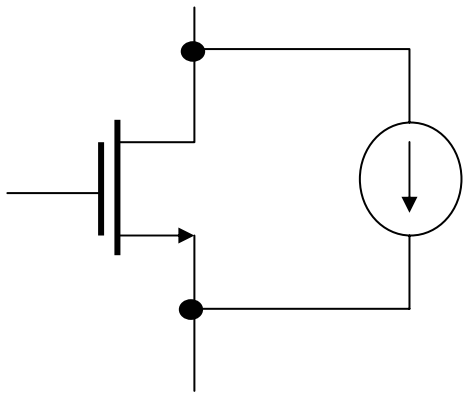
- Consists mainly of the gate source capacitance

$$Z_{in} = \frac{1}{j\omega C_{gs}}$$

However, for sub-micron technologies also resistive part (~ to 1/gm) for RF:



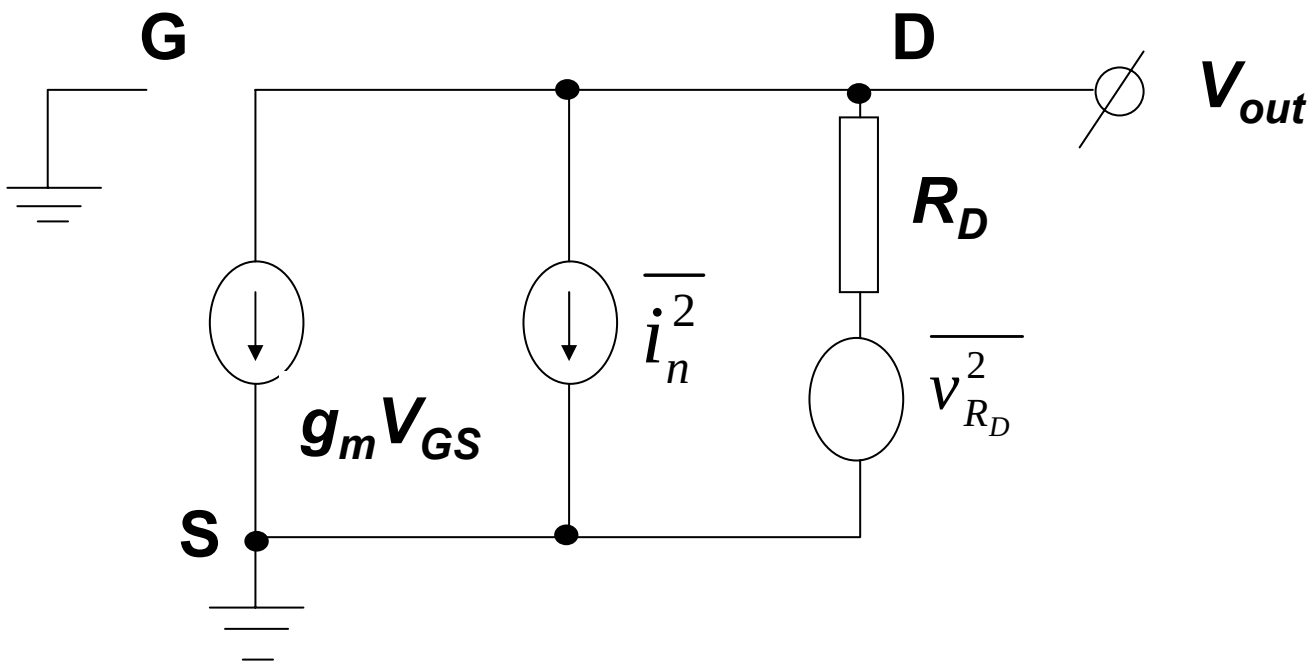
Main noise contributor in LNA



$$\overline{i_n^2} = 4kT\gamma g_m$$

The most significant noise source is the thermal noise in the channel of the MOS transistor. For long channel transistors γ is usually 2/3, but for sub-micron technologies this value is larger.

Model for NF calculation



Note that in this calculation we omit (the resistance of) matching components: they will increase the NF.

Calculation of the NF of a common source LNA

By calculating the noise contributions of each of the sources separately and afterwards applying superposition, the total mean square value of the output noise can be expressed by:

$$\overline{v_{n,out}^2} = 4kT\gamma g_m R_D^2 + 4kTR_D$$

To find the power spectral density of the input referred noise, the spectral density of the noise at the output is divided by the square of the gain (Av):

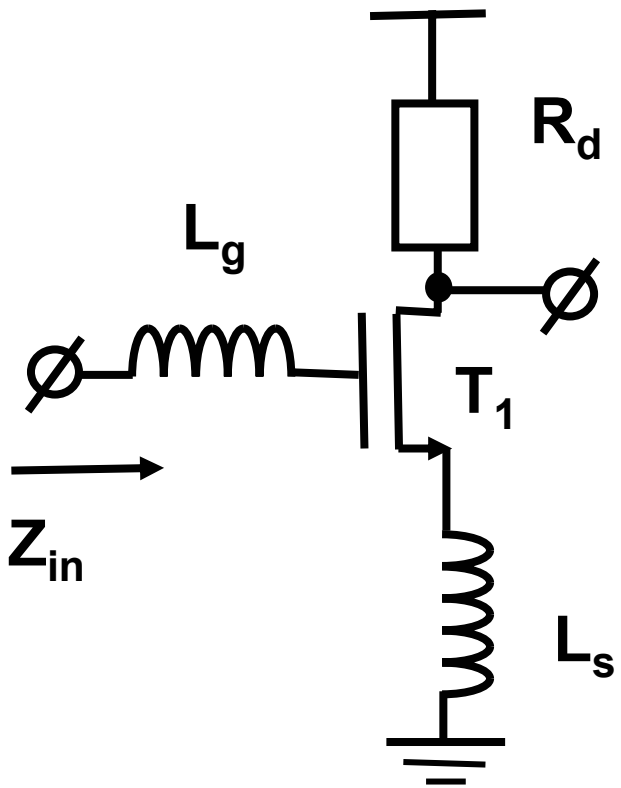
$$\overline{v_{n,in}^2} = 4kT\left(\frac{2}{3g_m} + \frac{1}{g_m^2 R_d}\right)$$

Application of the NF formula (slide 11) yields:

$$NF = 1 + \frac{2}{3g_m R_s} + \frac{1}{g_m^2 R_d R_s}$$

The NF can be decreased by increasing g_m and Rd

Source matching by inductive degeneration



$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs}} + (\frac{g_{m1}}{C_{gs}})L_s$$

$$Z_{in,resonance} = (\frac{g_{m1}}{C_{gs}})L_s \approx \omega_T L_s \quad (at\ resonance)$$

Can be made 50 Ω (real part)

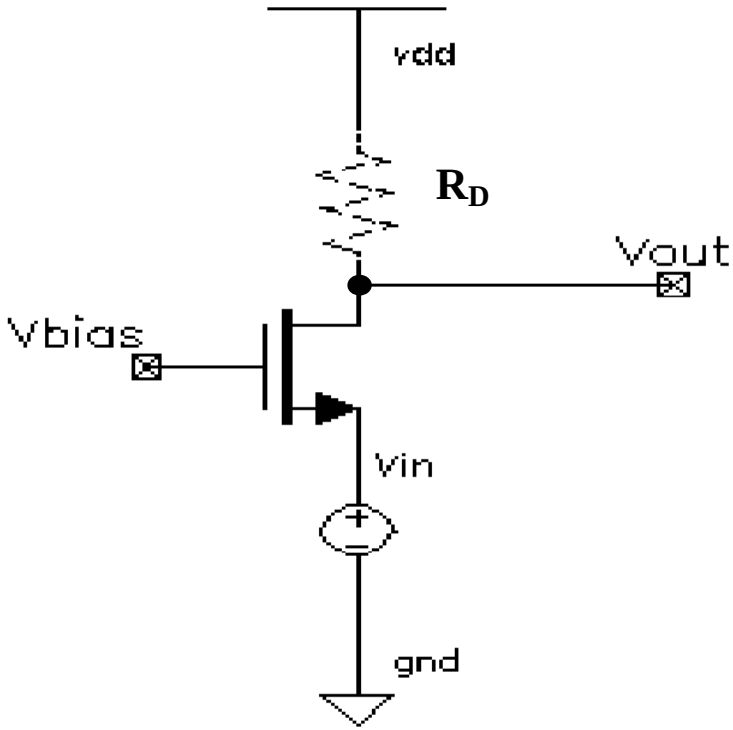
$$\omega_o = \frac{1}{\sqrt{(L_s + L_g)C_{gs}}}$$

Degeneration reduces the gain:

$$g_m = g_{m1}Q_{in} = \frac{\omega_T}{2\omega_0 R_s} = \frac{1}{2\omega_0 L_s}$$

Common gate topology

Common gate topology



This is the basic topology

Gate is grounded for AC signals

Small-signal gain calculation (I)

From the large signal behavior of the common gate LNA (working in saturation) it can be derived that:

$$I_D = \frac{\mu_n C_{ox} W}{2L}\left(V_{bias} - V_{in} - V_{TH}\right)^2 \qquad \text{IF} \qquad V_{DS} \geq V_{GS} - V_{TH}$$

$$V_{out} = V_{DD} - I_D R_D$$

Substitution of the first in the second equation yields the output voltage. Taking the derivative from the output voltage the gain can be calculated:

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{ox} \frac{W}{L} R_d \left(V_b - V_{in} - V_{TH}\right)\left(1 + \frac{\partial V_{TH}}{\partial V_{in}}\right) R_d$$

Small-signal calculation (II)

$$A_v = \frac{\partial V_{out}}{\partial V_{in}} = \mu_n C_{ox} \frac{W}{L} R_d \left(V_b - V_{in} - V_{TH}\right)\left(1 + \frac{\partial V_{TH}}{\partial V_{in}}\right) R_d$$

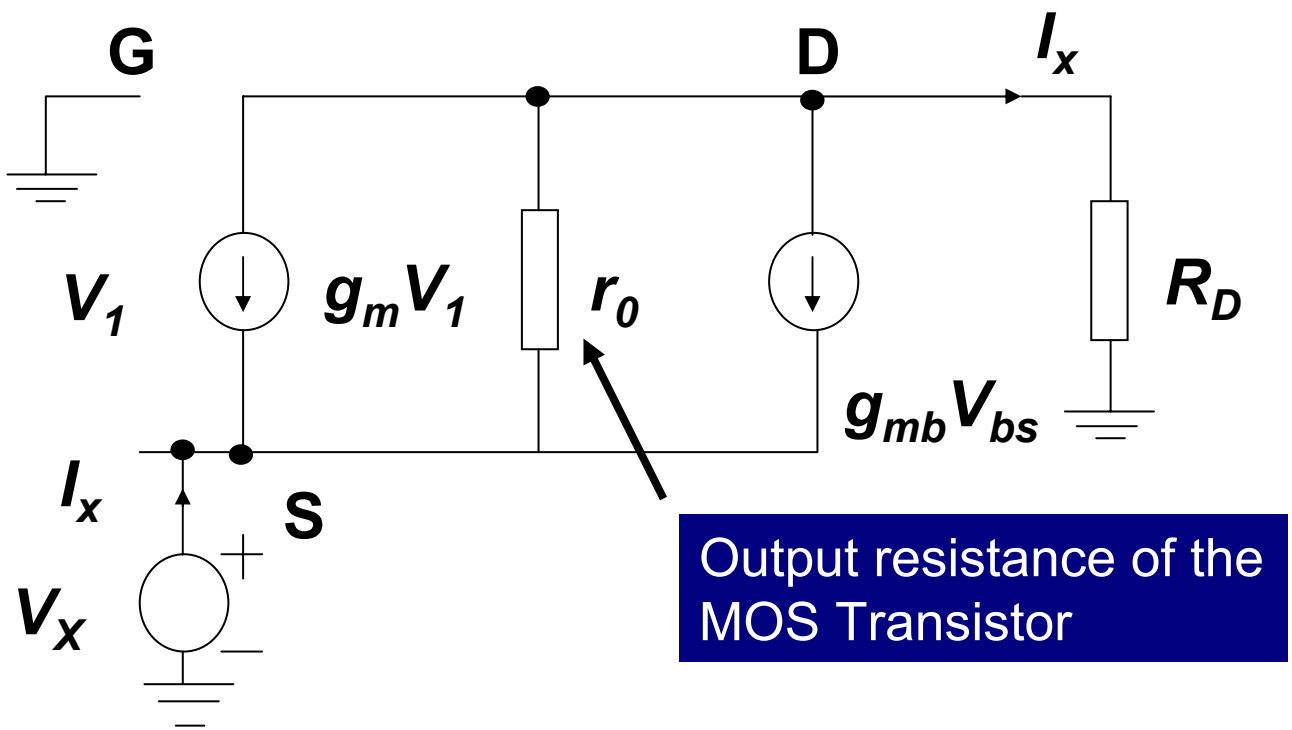
Where $\eta = \frac{\partial V_{TH}}{\partial V_{in}}$

denotes the influence of the input voltage on the threshold voltage, and can be expressed as: $\eta = \frac{g_{mb}}{g_m}$

where g_{mb} is the transconductance from the bulk, hence the voltage gain is:

$A_v = g_m(1+\eta)R_d$ which is equal to $\boxed{A_v = (g_m + g_{mb})R_d}$

Input impedance of common gate LNA (I)



Calculation model for input impedance

Input impedance of common gate LNA (II)

- From the small signal model in figure is can be concluded that *V1= -Vx*, and thus:

$$V_X = R_D I_X + r_0 \left[I_X - (g_m + g_{mb}) V_X \right]$$

Hence, the input impedance is:

$$Z_{in} = \frac{V_X}{I_X} = \frac{R_D + r_0}{1 + (g_m + g_{mb}) r_0} \approx \frac{R_D}{(g_m + g_{mb}) r_0} + \frac{1}{g_m + g_{mb}}$$

If gm+gmb>>1

The advantage of this frequency independent input impedance is that broadband matching can be applied, assuming a fixed value for g_m+g_{mb}

NF of common gate LNA

The input referred noise voltage of the common gate LNA can be calculated in a similar way as for the common source:

$$\overline{V_{n,in}^2} = \frac{4kT\left(\gamma g_m + 1/R_d\right)}{\left(g_m + g_{mb}\right)^2}$$

Where g_{mb} is the bulk-transconductance and γ= 2/3 for long channel transistors (larger value for sub-micron technologies)

Application of the NF formula (slide 11) yields:

$$NF = 1 + \frac{\dfrac{4kT\left(\gamma g_m + 1/R_D\right)}{\left(g_m + g_{mb}\right)^2}}{4kTR_s}$$

Comparison between NF of both LNAs

Common source LNA:

$$NF = 1 + \frac{2}{3 g_m R_s} + \frac{1}{g_m^2 R_d R_s}$$

This LNA can have an ***arbitrary small*** NF at the cost of power dissipation.

Common gate LNA:

$$NF = 1 + \frac{4kT\gamma}{4kT g_m R_s}$$

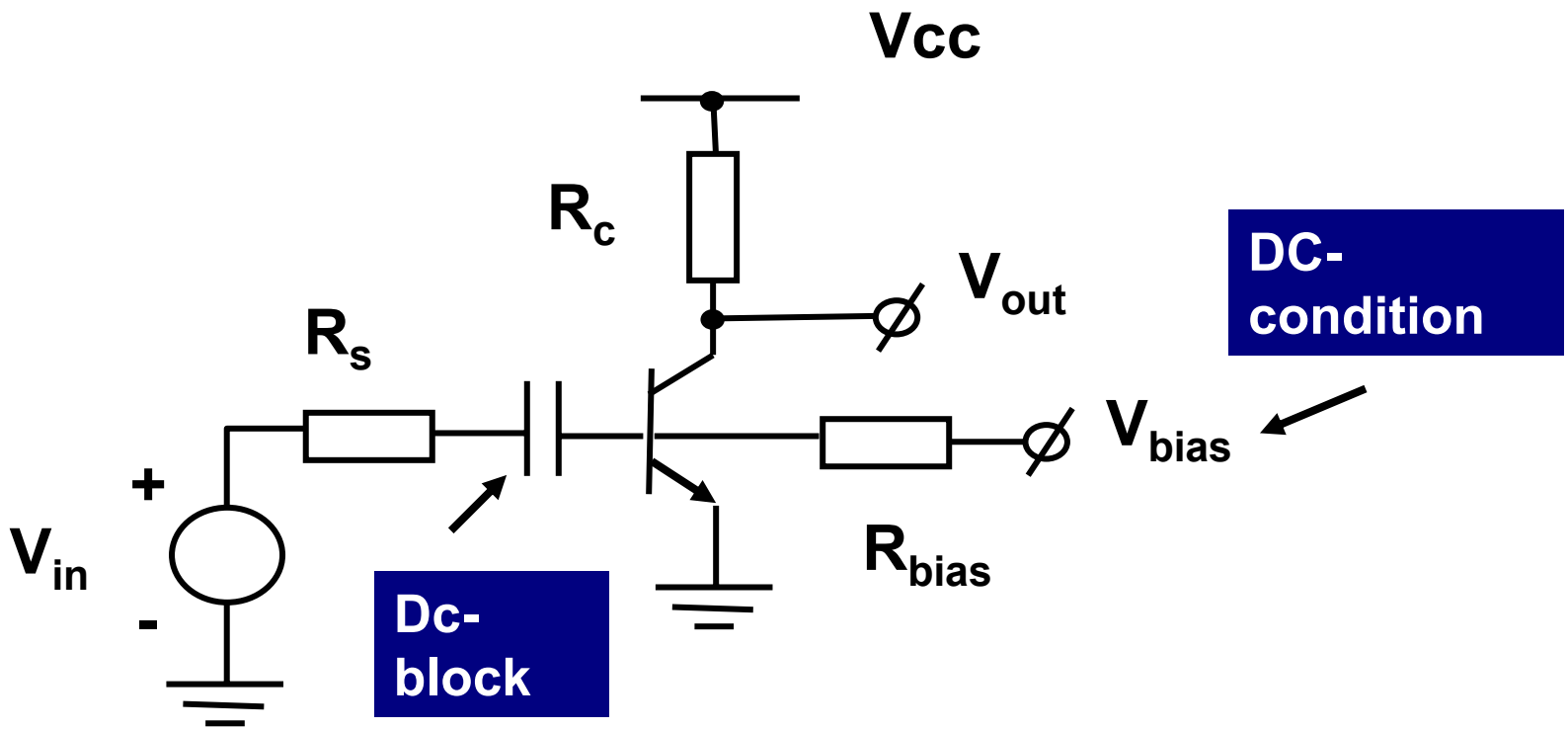
Assuming that $g_{mb} \ll g_m$ and $g_m \ll 1/R_d$ the noise figure can be calculated as:

Under matching constraints $g_m R_s = 1/50 * 50 = 1$, and if γ is chosen to be 2/3 the minimum possible noise figure in dB will be:

$$NF = 10\log(1+\gamma) = 10\log(1+2/3) = 2.2 \text{ dB}$$

Common emitter LNA

Common emitter LNA



NF of common emitter LNA

- The total input-referred noise voltage (including the source resistance) calculates to:

$$\overline{v_{tot}^2} = 4kT\left(\frac{1}{2g_m} + \frac{g_m R_s^2}{2\beta} + R_s + r_b\right)$$

collector shot noise — $\frac{1}{2g_m}$

Base shot noise — $\frac{g_m R_s^2}{2\beta}$

source resistance — R_s

base resistor — r_b

$$NF = \frac{\overline{v_{tot}^2}}{4kTR_s} = 1 + \frac{1}{2g_m} + \frac{g_m R_s^2}{2\beta} + r_b$$

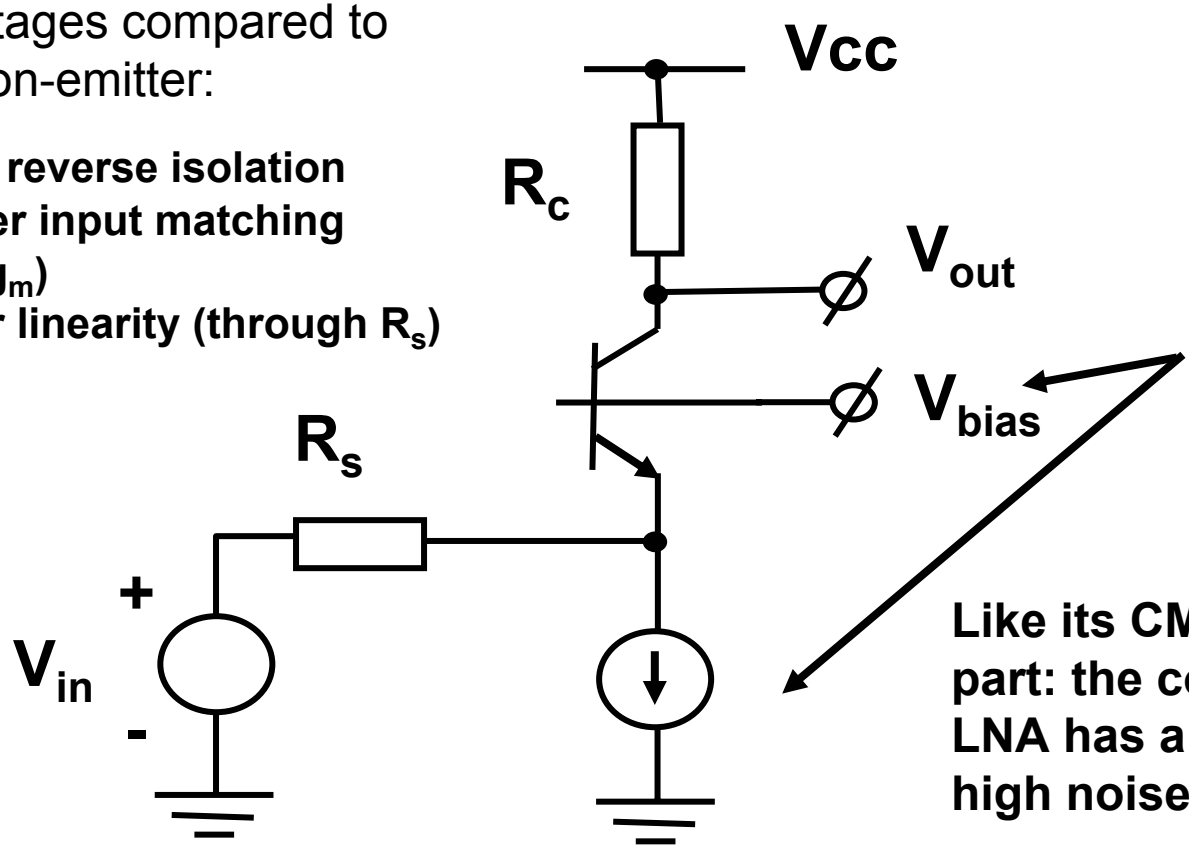
$$NF_{\min} = 1 + \sqrt{\frac{(1+2g_m R_b)}{\beta}} \quad \textbf{for} \quad R_{s,opt} = \frac{\sqrt{\beta(1+2g_m R_b)}}{g_m}$$

Common base LNA

Common base LNA

Advantages compared to common-emitter:

-Better reverse isolation
-Simpler input matching (Z_{in}~$1/g_m$)
-Higher linearity (through R_s)



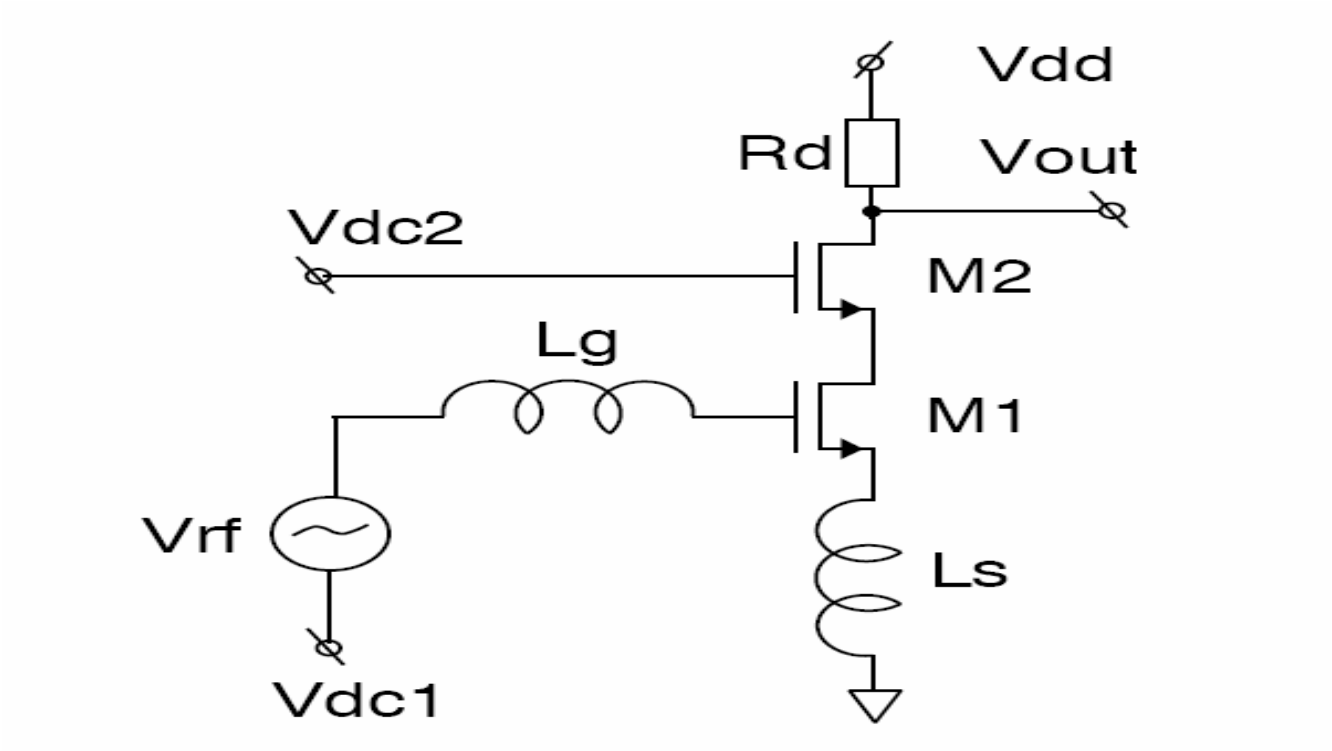
DC-conditions

Like its CMOS counter-part: the common-gate LNA has a relatively high noise figure

Example of LNA Dimensioning

(see also hand-out)

Start-point: analysis of an LNA topology



Common-source inductively degenerated LNA topology

Analysis of the circuit topology (I)

SEE HAND-OUT: FULLY-INTEGRATED DECT/BLUETOOTH MULTI-BAND LNA IN 0.18 CMOS, V.vidojkovic, et. al.)

- Input impedance

transconductance M1

$$Z_{in} = s(L_s + L_g) + \frac{1}{sC_{gs_t}} + \frac{g_m}{C_{gs_t}}L_s$$

gate and source inductances

to match: make IMAG-part Zin zero (see slide 32)

Analysis of the circuit topology (II)

- Noise factor

$$F = 1 + \frac{1}{Rs}\left(\frac{\omega Lg}{Q_{Lg}} + \frac{\omega Ls}{Q_{Ls}}\right) + \gamma g_{d0} Rs\left(\frac{\omega C_{gs_t}}{g_m}\right)^2 + \frac{(\omega Ls)^2}{R_s R_d}$$

$$Q_{Lg} = \omega Lg/Rg$$
$$Q_{Ls} = \omega Ls/Rs$$

finite quality factor of coils that are used

Channel thermal noise, noise of load R_d and the finite quality factors of the inductors is taken into account.

Analysis of the circuit topology (III)

- We can simplify the noise factor expression by introducing a new parameter: n, the ratio between the two inductances:

$$n = \frac{Lg}{Ls}$$

The noise factor

$$F = 1 + \frac{\omega Ls}{R_s}\left(\frac{n}{Q_{Lg}} + \frac{1}{Q_{Ls}}\right) + \gamma\frac{g_{d0}}{g_m}\frac{1}{n+1} + \frac{(\omega Ls)^2}{R_s R_d}$$

Analysis of the circuit topology (IIII)

- Linearity is, in the first order, determined by the overdrive voltage:

$$IIP3 \approx V_{gs} - V_t$$

When choosing an overdrive voltage: the transconductance M1 can be determined based on the available power budget

$$g_m = \frac{2P_d}{V_{dd}(V_{gs} - V_t)}$$

$\mu_n C_{ox} \frac{W}{L}(V_{gs} - V_{TH})$

$\sqrt{2\mu_n C_{ox} \frac{W}{L} I_d}$

} **long channel**

$\frac{\mu_n C_{ox}}{2} W E_{crit}$ ← **short-channel**

After many equations (to boring for slides: see hand-out): some conclusions

- A lower *F* can be obtained by increasing *gm*, which in turn can be obtained by a higher power consumption

- Better quality factor of the inductors *Lg* and *Ls* improves *Fmin*.

- The chip area can be reduced by reducing the values of the inductances *Lg* and *Ls*. This can be done by increasing *gm*,

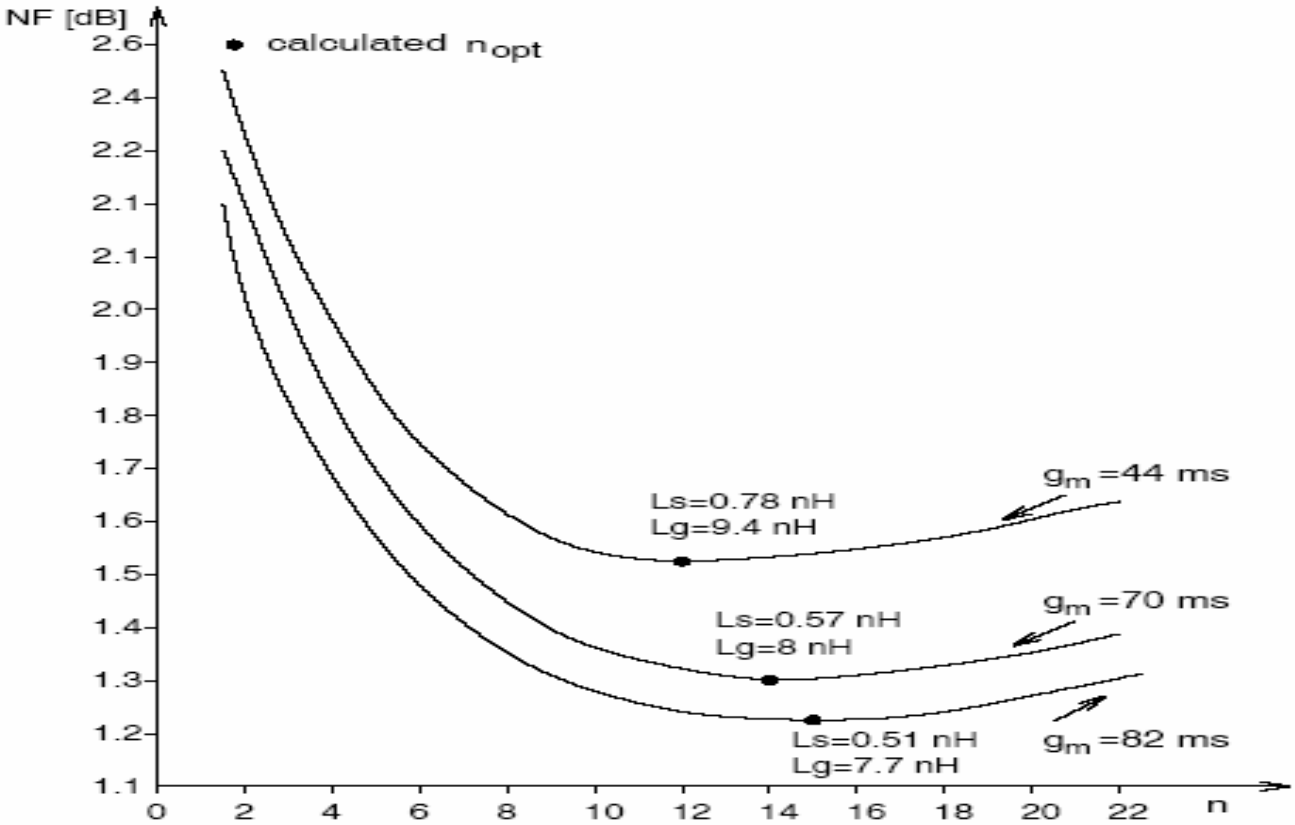
- A higher voltage gain can be obtained by increasing *gm*, which means by increasing the power consumption and by increasing the value of the load resistor (*Rd*).

After all LNA analysis: structured design flow can be defined

- **Step1:** Choose overdrive voltage V_{gs}-V_{th} based on IIP3 requirements
- **Step2:** Based on a given power budget (*Pd*), determine the aspect ratio *W*/*L* of and the transconductance (*gm*) of the transistor *M*1
- **Step3:**Calculate n_{opt} *(coil ratio)* that gives minimum noise factor
- …
- …
- … (see hand-out)

- **Step10**: Check if all specification is met in simulation and check DC conditions

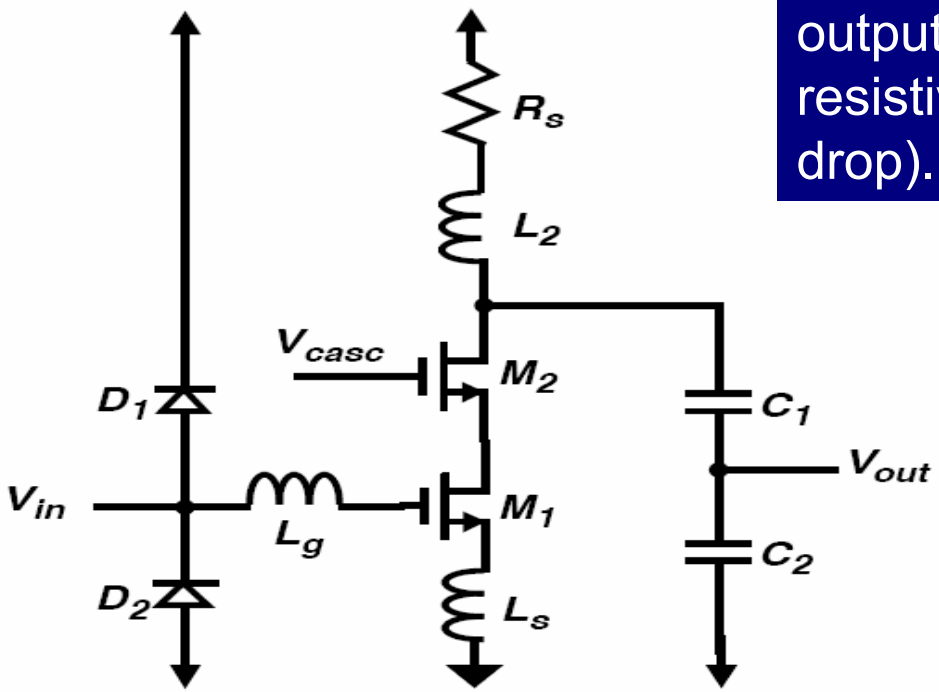
Result of analysis: good prediction of LNA spec, such as NF & structured design flow



Simulated noise figure as a function of n

Other LNA topology examples/ derivatives

Common source cascode LNA



Picture: cascode LNA with tuned output (more gain than only resistive output and less voltage drop). LNA includes ESD protection

Cascode advantages:

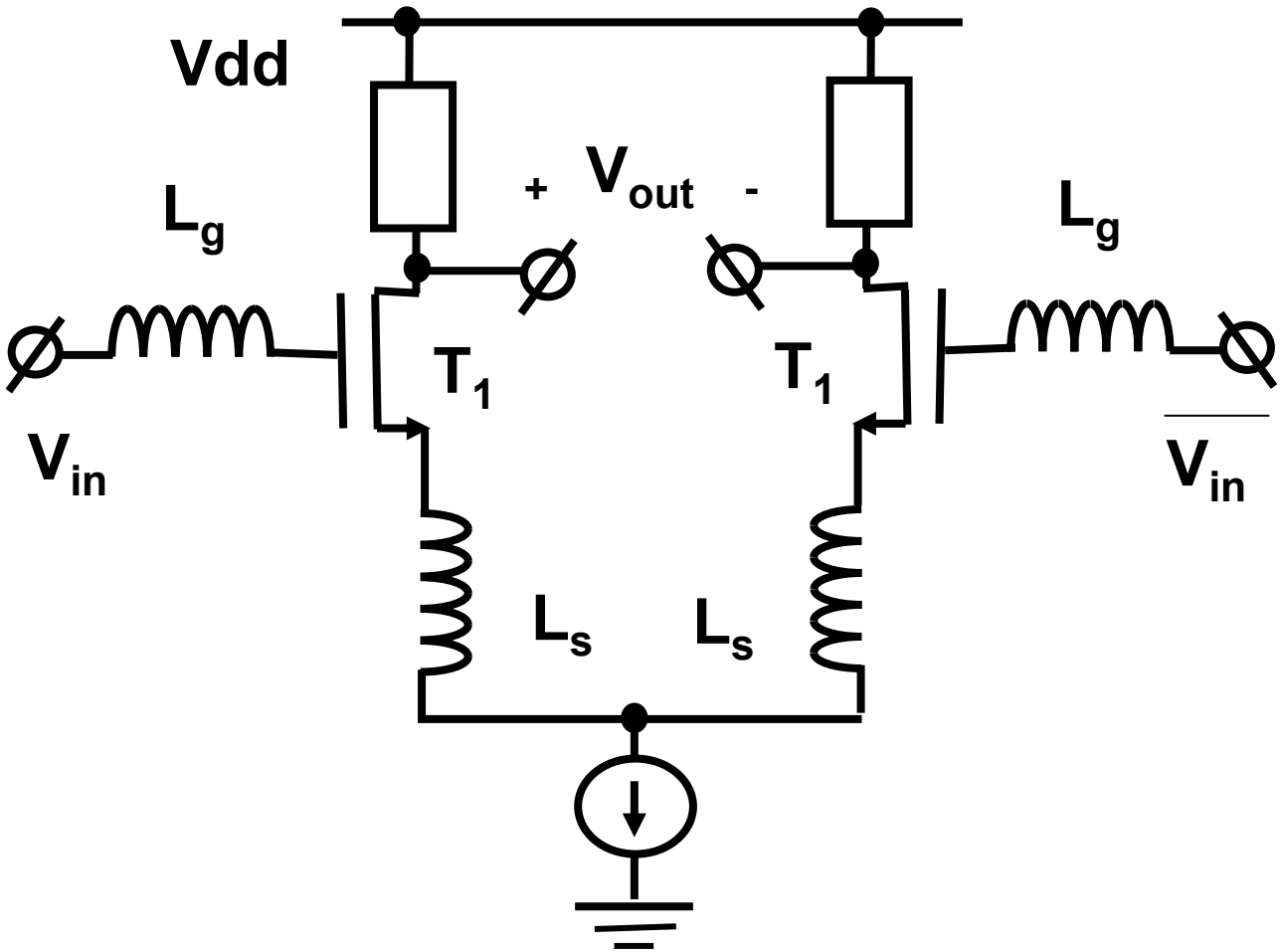
- **Higher reverse isolation (S12)**
- **Improved gain (miller-effect due to C_{gd1} is reduced)**

Cost: somewhat higher noise figure

Ref [1] on slide: "NF/power trade-off"

Source: P. Westergaard

Differential LNAs

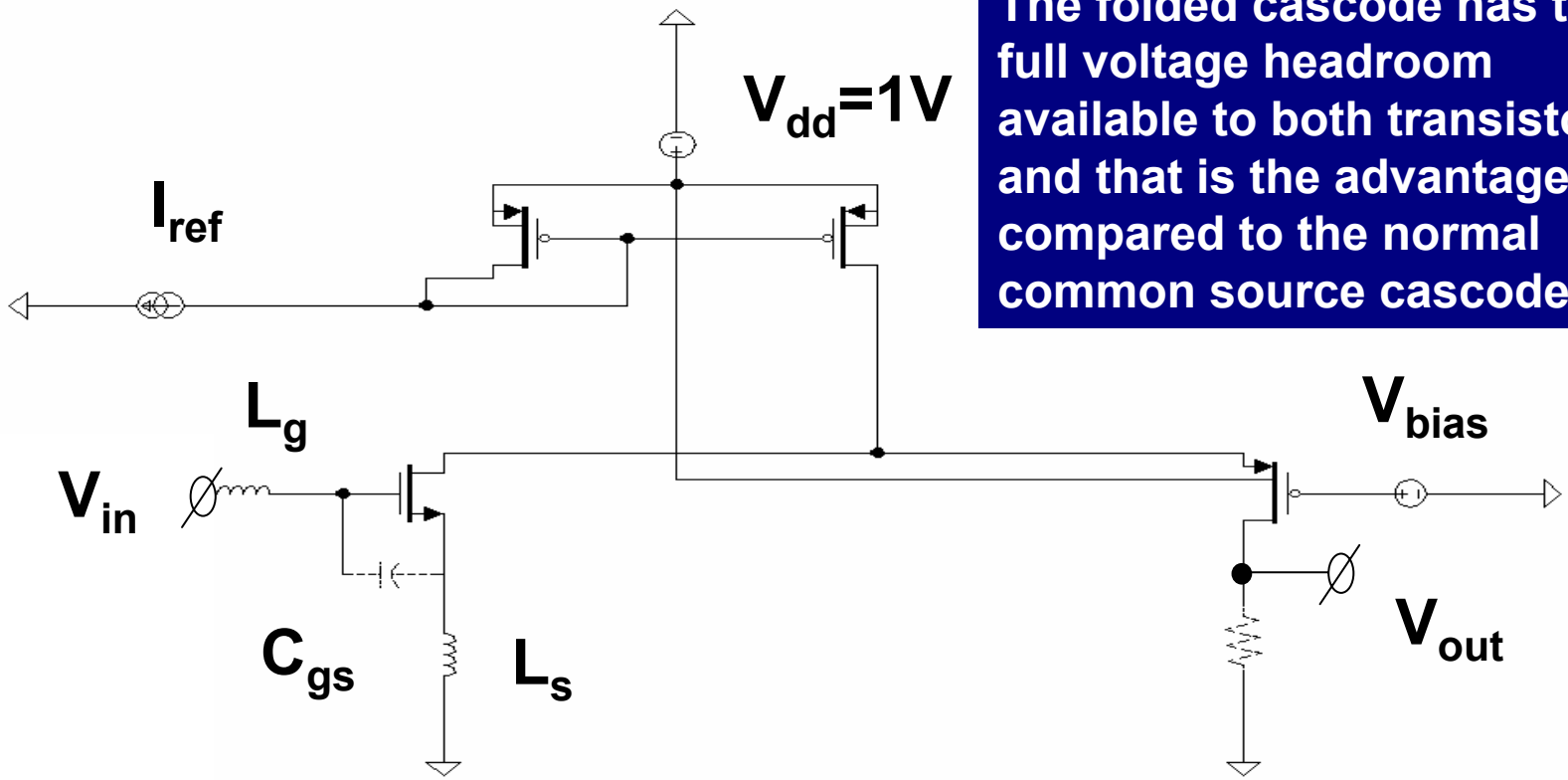


Pros & Cons differential LNAs

A differential architecture gives a better rejection of on-chip interference. Also, the differential architecture alleviates the problem of parasitic source degeneration (e.g. bondwires). Obviously, circuit techniques like cascoding, etcetera, can be implemented differentially.

The penalty is that twice the power must be consumed to achieve the same noise figure as a single-ended version.

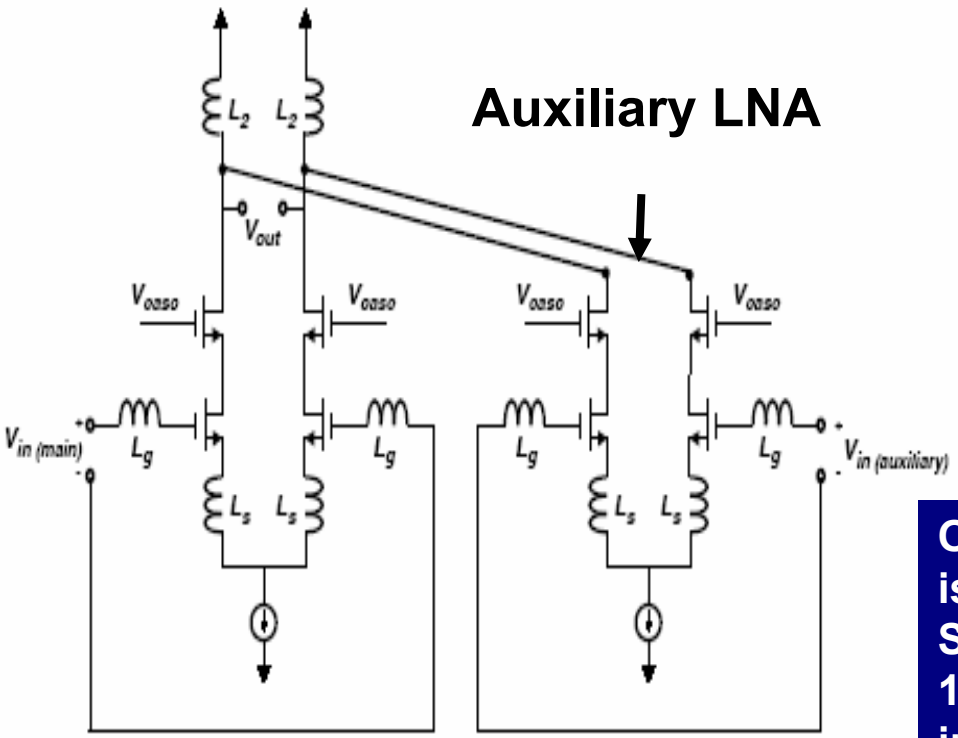
Low voltage folded-cascode LNA



The folded cascode has the full voltage headroom available to both transistors, and that is the advantage compared to the normal common source cascode

Image: E. Hanssen

LNA with third-order term cancellation

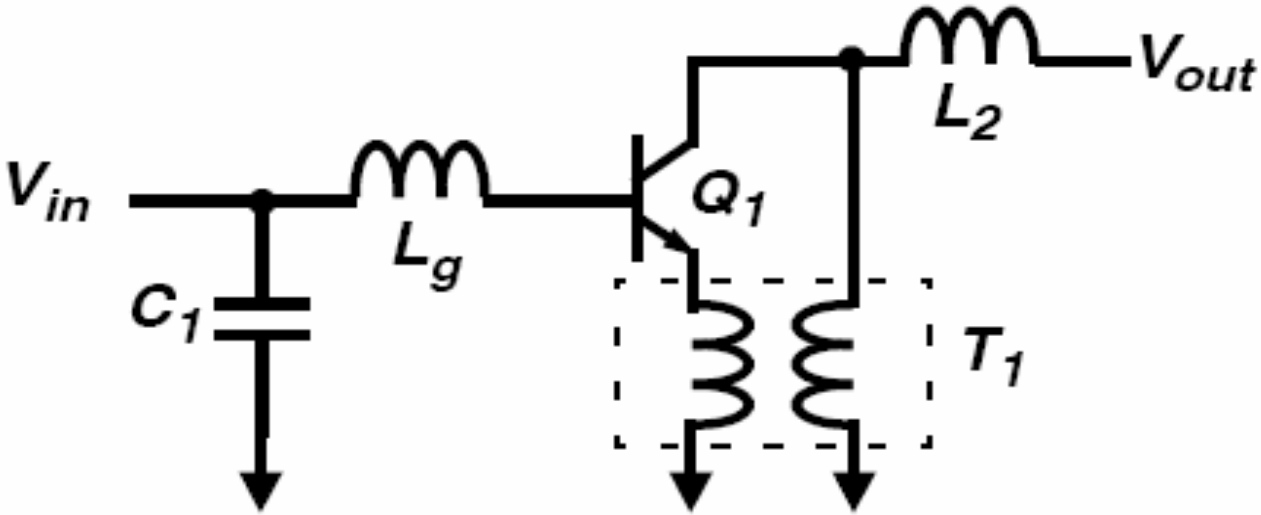


The placement of two LNAs in parallel allows the third-order IM products to be effectively cancelled. The drawback of this design is a doubling of power consumption due to the dual-LNA architecture.

Only 1/8th of the auxiliary output current is subtracted from the main LNA output. Since the auxiliary LNA contributes only 1/8th more output noise, its addition increases the overall noise figure of the circuit by less than 0.2dB.

Ref [3] on slide: IIP3/power trade-off

Low voltage (1V) LNA with transformer



The integrated transformer *T1* has two purposes. The negative feedback it employs improves the linearity of the circuit. More importantly, the transformer feedback tunes out the Miller capacitor Cbc: better stability, more gain.

Source: P. Westergaard

Circuit: John Long

Typical LNA performance

Overview of CMOS LNA performance

Ref.	NF (dB)	Gain (dB)	f_0 (GHz)	IIP3 (dBm)	I (mA)	V (V)	P (mW)	Techn. (um)	Arch.	Year
[1]	3.6	26	1.3	-3	5	2.8	14	0.35	Diff.	2001
[2]	4.5	7.5	2.4	-	8	1.8	14.4	0.18	Single	2001
[3]	2.5	19.9	2.4	2	7.4	2	14.7	0.35	Diff.	2001
[4]	5.7	18	2.4	-10	8.5	1	8.5	0.35	Diff.	2001
[5]	0.8	20	1.3	-11	6	1.5	9	-	Single	2001
[6]	4.8	18	5	-	3.6	2	7.2	0.24	Diff.	2000
[7]	1.24	21	2.4	-	2.5	2	5	0.35	Single	2000
[8]	-	-	1	-	0.2	1.5	0.3	0.35	Diff.	2001
[9]	2.5	22	2.5	-	8	1.5	12	0.35	Single	1999
[10]	3.5	22	1.5	-	5	1.5	7.5	0.6	Single	1997
[11]	3.8	17	1.5	-6	8	1.5	12[1]	0.35	Diff.	1997

Source: M. de Jongh

References of previous table (I)

[1] Svelto, F. and S. Deantoni, G. Montagna, R. Castella
IMPLEMENTATION OF A CMOS LNA PLUS MIXER FOR GPS APPLICATIONS WITH NO EXTERNAL COMPONENTS
IEEE transactions on very large scale integration (VLSI) systems, vol. 9, no. 1, Feb. 2001

[2] Yamamoto, K. and T. Heima, A. Furukawa, M. Ono, Y. Hashizume, H. Komurasaki, S. Maeda, H. Sato, N. Kato
A 2.4 –GHz-BAND 1.8-V OPERATION SINGLE-CHIP Si-CMOS T/R-MMIC FRONT-END WITH A LOW INSERTION LOSS SWITCH
IEEE journal of solid-state circuits, vol. 36, no. 8, p. 1186 – 1197, Aug. 2001

[3] Huang, J.C. and R.M. Weng, C.C. Chang, K. Hsu, K.Y. Lin
A 2V 2.4Ghz FULLY INTEGRATED CMOS LNA
Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on, vol. 4, p. 466 – 469, 2001

[4] Chan, A.N.L. and J.M.C.Wong, H.C. Luong
A 1-V 2.4-GHz CMOS RF receiver front-end for Bluetooth application
Circuits and Systems, 2001. ISCAS 2001. The 2001 IEEE International Symposium on, vol. 4, p. 454 –457, 2001

[5] Leroux, P. and J. Janssens, M. Steyaert,
A 0.8 dB NF ESD-protected 9 mW CMOS LNA
Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC. 2001 IEEE International, p. 410 -411, 471, 2001

Source: M. de Jongh

References of previous table (II)

[6] Samavati, H. and H.R. Rategh, T.H. Lee

A 5-GHz CMOS wireless LAN receiver front end
Solid-State Circuits, IEEE Journal of, vol. 35, issue 5, p. 765 –772, May 2000

[7] Choong-Yul, C. and S.G. Lee

A low power, high gain LNA topology
Microwave and Millimeter Wave Technology, 2000, 2nd International Conference on. ICMMT 2000, p. 420 –423, 2000

[8] Vouilloz, A. and C. Dehollain, M. Declercq

A low-power CMOS super-regenerative receiver at 1 GHz
Custom Integrated Circuits Conference, 2000. CICC. Proceedings of the IEEE 2000,

p. 167 –170

[9] Rafla, R.A. and M.N. El-Gamal,

Design of a 1.5 V CMOS integrated 3 GHz LNA
Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on, vol. 2, p. 440 -443 vol.2, 1999

[10] Shaeffer, D.K. and T.H. Lee

A 1.5-V, 1.5-GHz CMOS LOW NOISE AMPLIFIER

IEEE Journal of solid-state circuits, vol. 32, no. 5, p. 745 – 751, May 1997

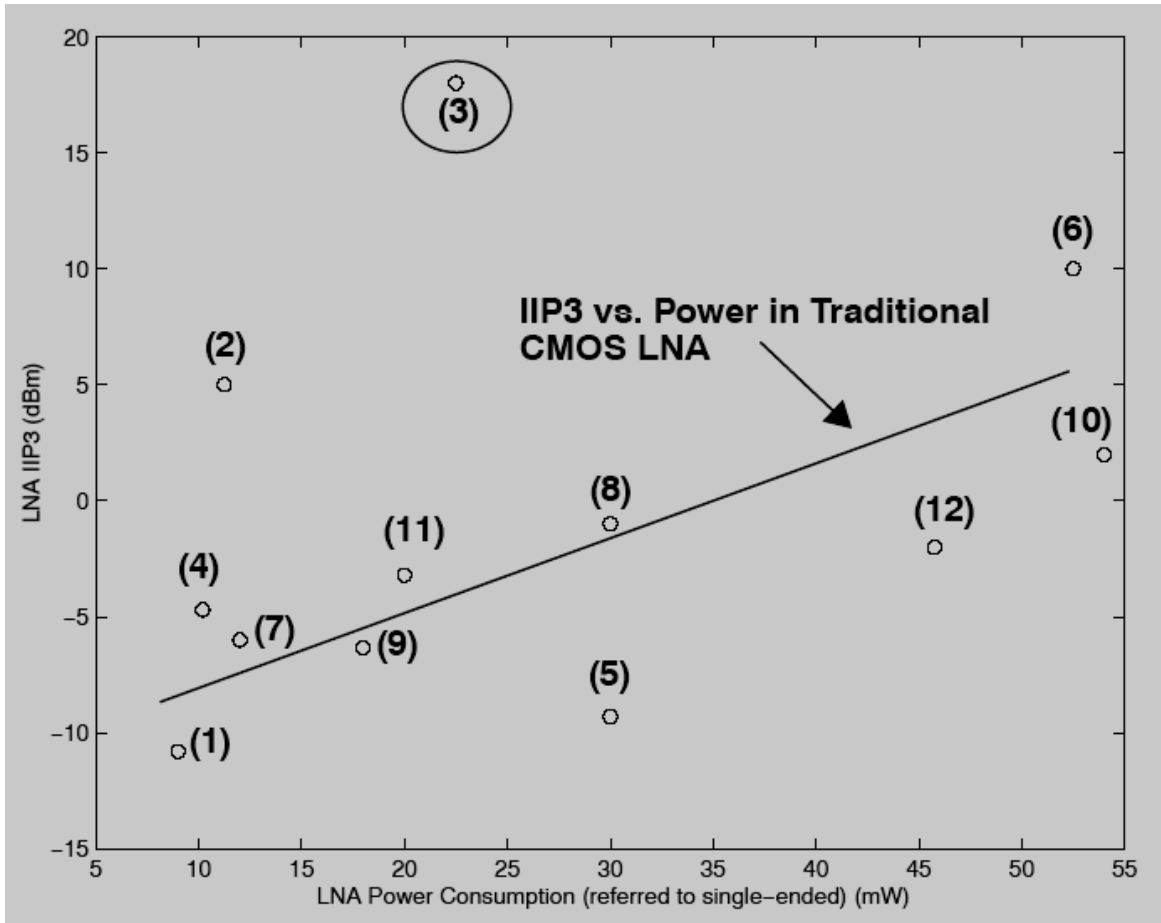
[11] Shahani, A.R. and D.K. Shaeffer, T.H. Lee

A 12-Mw WIDE DYNAMIC RANGE CMOS FRONT-END FOR A PORTABLE GPS RECEIVER

IEEE journal of solid-state circuits, vol. 32, no. 12, p. 2061- 2070, Dec 1997

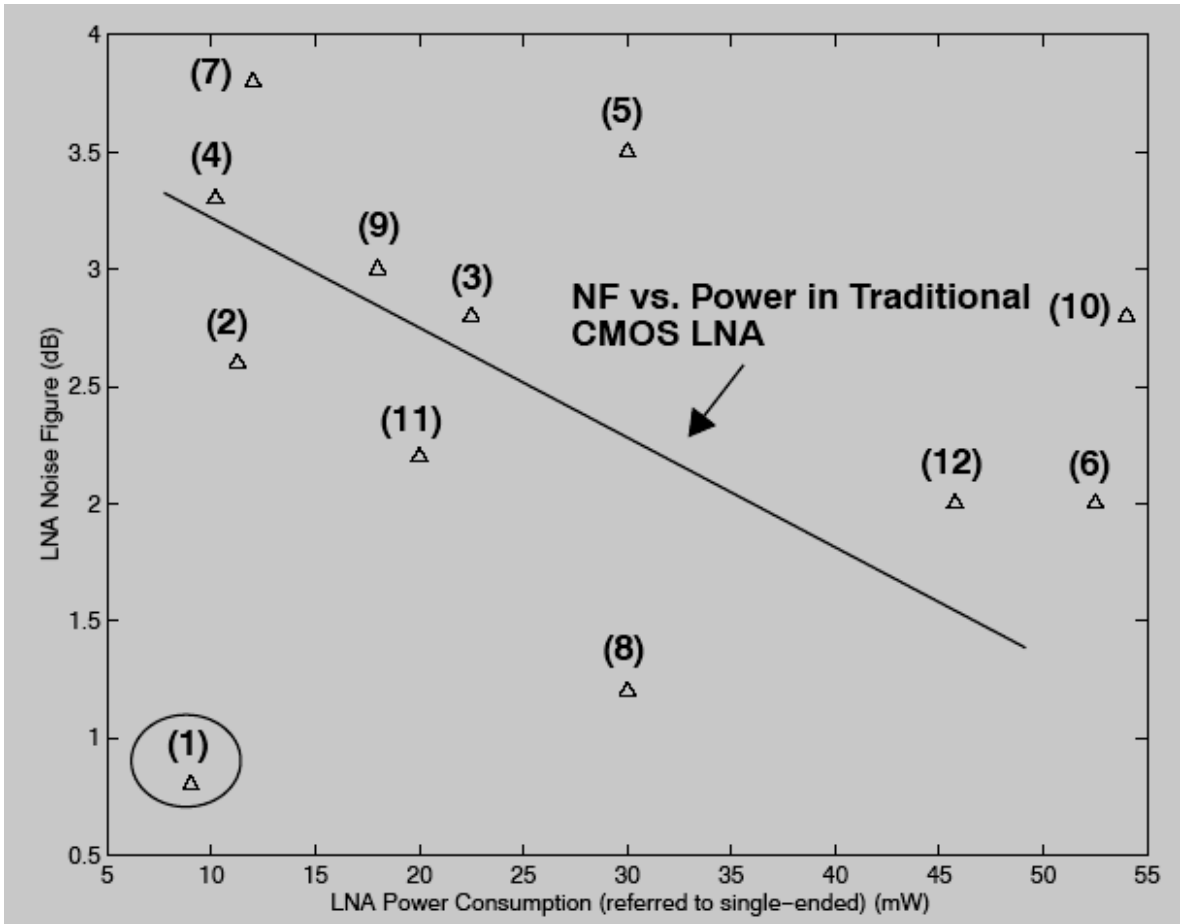
Source: M. de Jongh

IIP3 / Power Trade-off



Source: P. Westergaard

NF / Power trade-off



Source: P. Westergaard

References of two previous slides

(1) Leroux 2001, CMOS @ 1.23GHz [1]
(2) Ding 2001, 0.35um CMOS @ 900MHz [2]
(3) Ding 2001, 0.35um CMOS @ 900MHz [2]
(4) Janssens 1998, 0.5um CMOS @ 900MHz [3]
(5) Shaeffer 1997, 0.6um CMOS @ 1.5GHz [4]
(6) Rodgers 1999, UTSi CMOS @ 2.0GHz [5]
(7) Shahani 1997, 0.35um CMOS @ 1.6GHz [6]
(8) Floyd 1999, 0.8um CMOS @ 900MHz [7]
(9) Zhou 1998, 0.6um CMOS @ 900MHz [8]
(10) Kim 1998, 0.8um CMOS @ 1.9GHz [9]
(11) Karanicolas 1996, 0.5um CMOS @ 900MHz [10]
(12) Huang 1999, 0.25um CMOS @ 900MHz [11]

Appendix

ADS LNA simulation example

ADS documentation

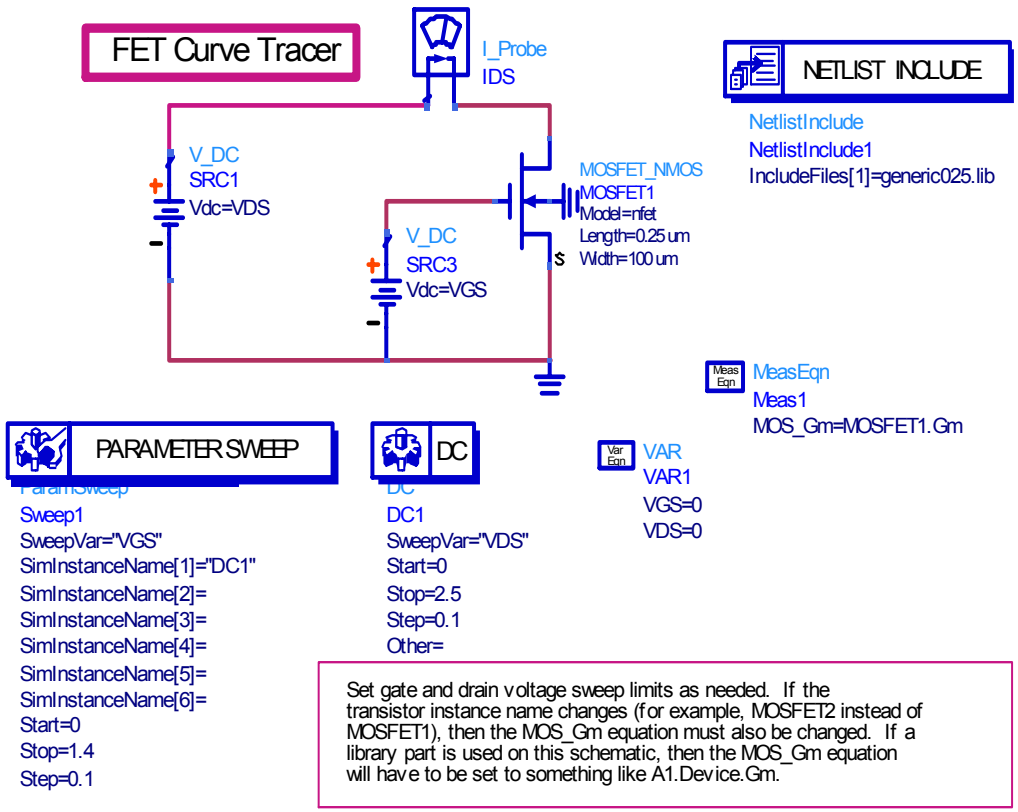
- Apart from the handed-out ADS tour: a lot more info on ADS and simulation tricks, know-how on http://www.agilent.com

Project data

- **Project name:** LNA_PRJ
- **Technology:** CMOS 0.25 um (included via netlist statement)
- **Number of networks:** 9 (plus one sub-network)

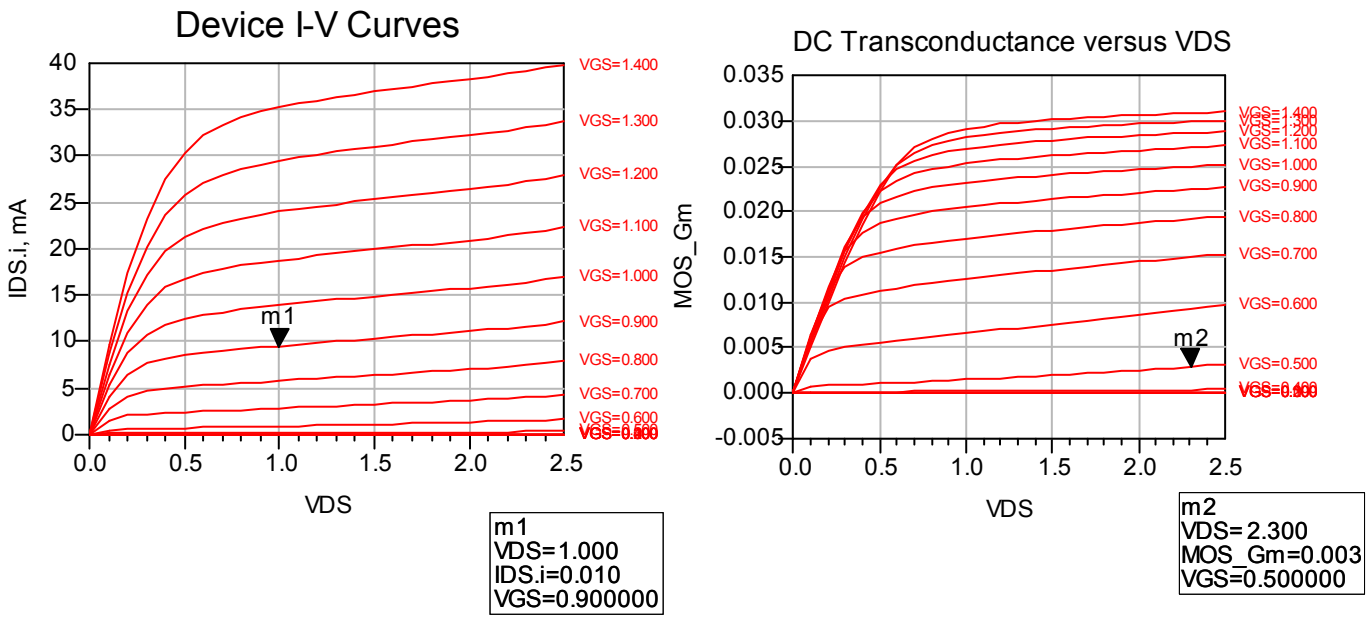
- **Description:** Shows how to simulate all important specifications of a (common-source cascode) LNA. Output matching is not done, because after the LNA no external (50 Ohm) filter is anticipated: hence no need for matching (which cost 3 dB in gain)

Simulation of MOS characteristics



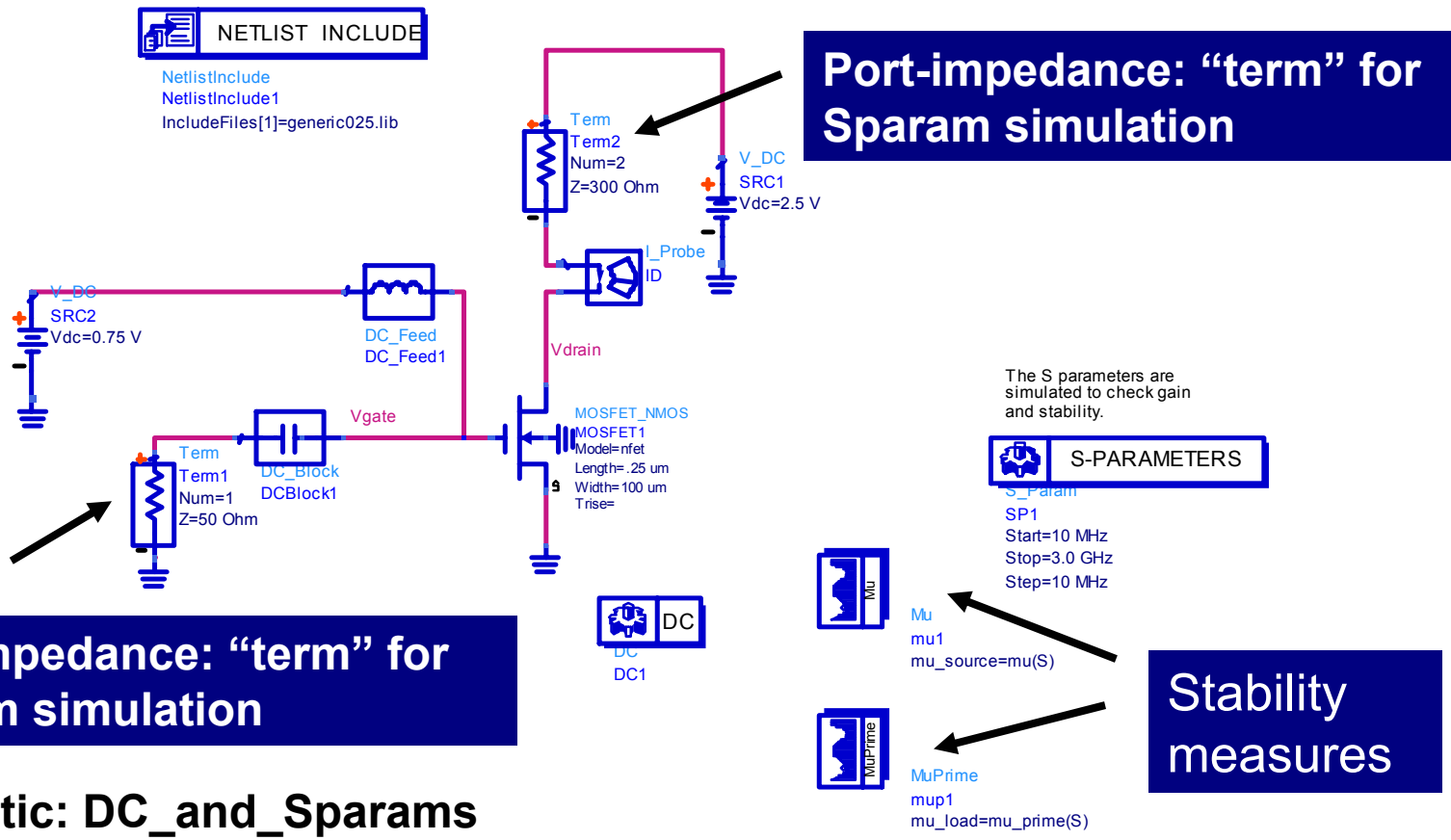
Schematic: FET_curve_tracer

Example of simulation output



DC transfer curves to determine proper biasing voltage Vgs

DC and S-parameter simulation



Schematic: DC_and_Sparams

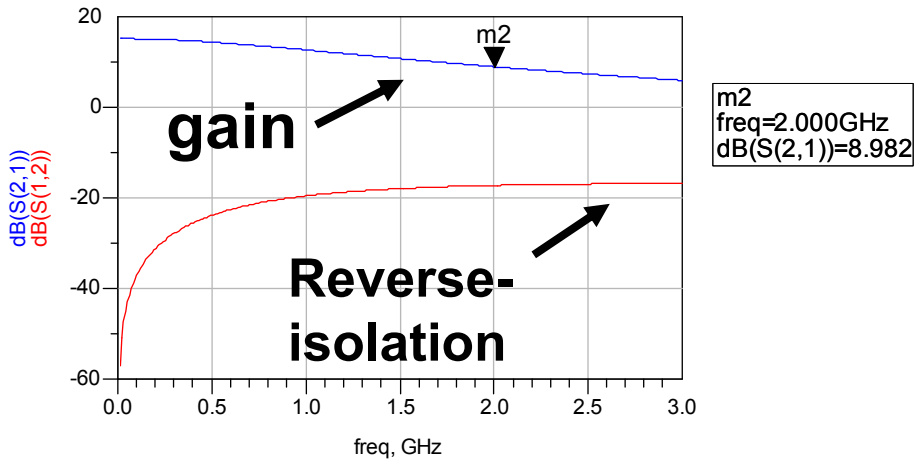
Example of simulation output

freq	Vgate	Vdrain
0.000 Hz	750.mV	1.19 V

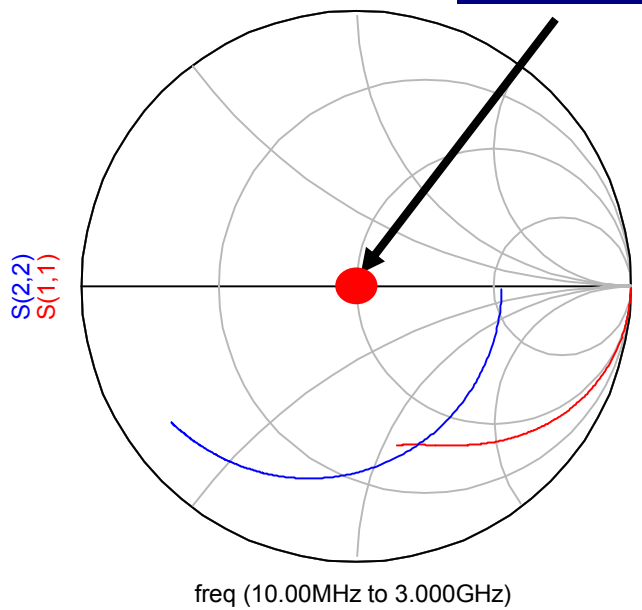
freq	ID.i
0.000 Hz	4.35mA

Dc conditions

Target for S11: 50 Ohm

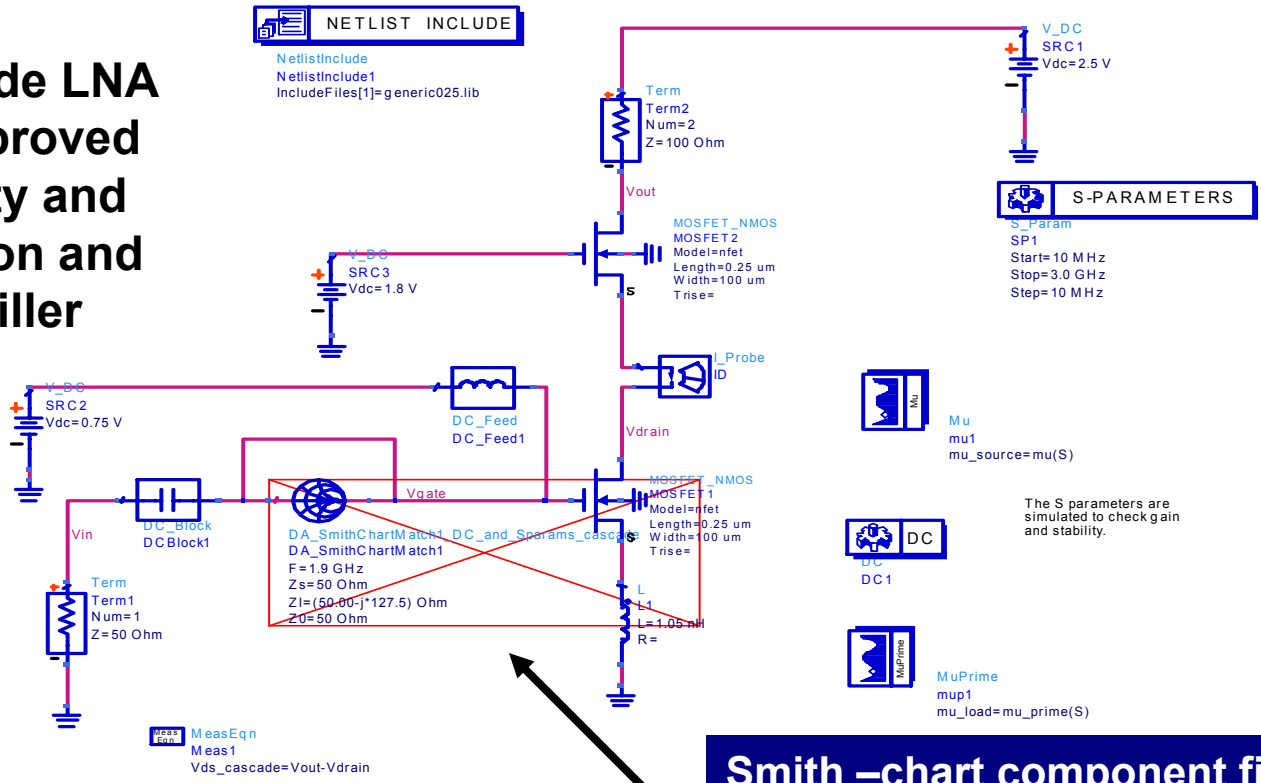


S-parameters



DC and S-parameter simulation: cascode LNA

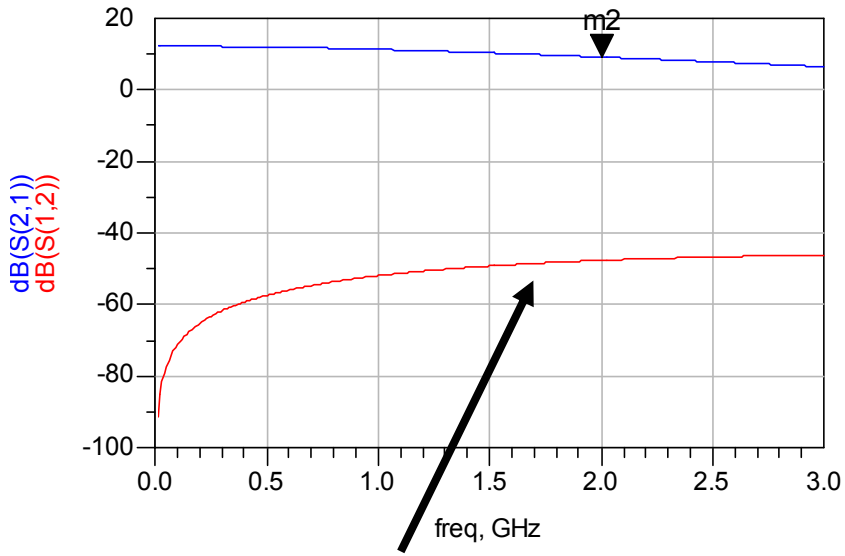
Cascode LNA for improved stability and isolation and less miller effect



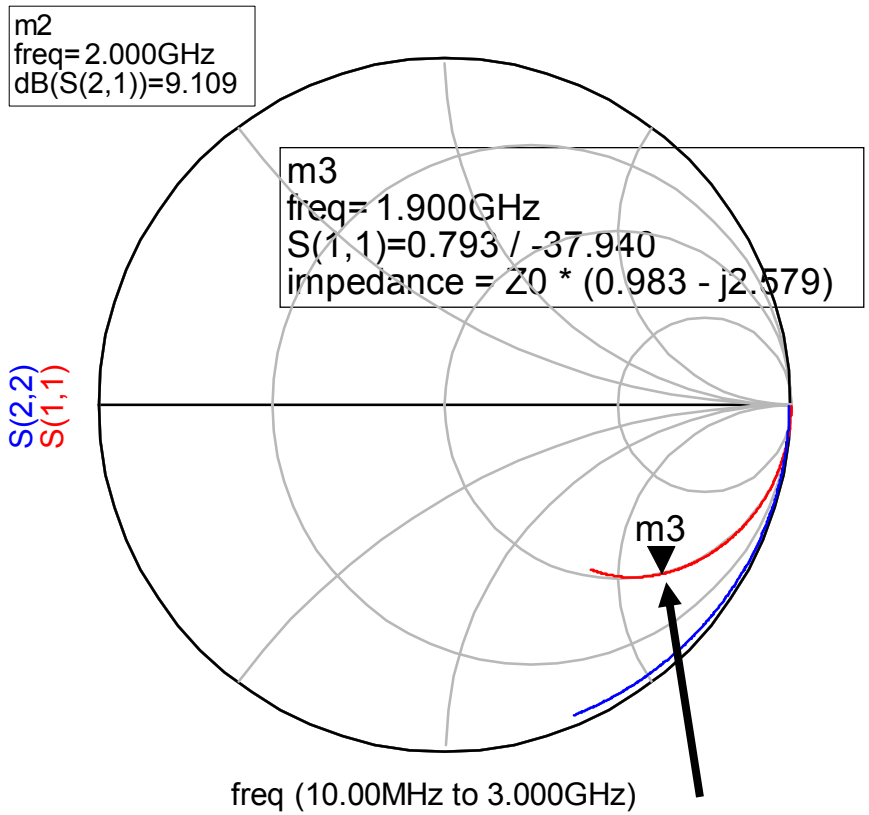
Schematic: DC_and_Sparams_cascode

Smith –chart component first disabled and shorted to see un-matched S11

Example of simulation output



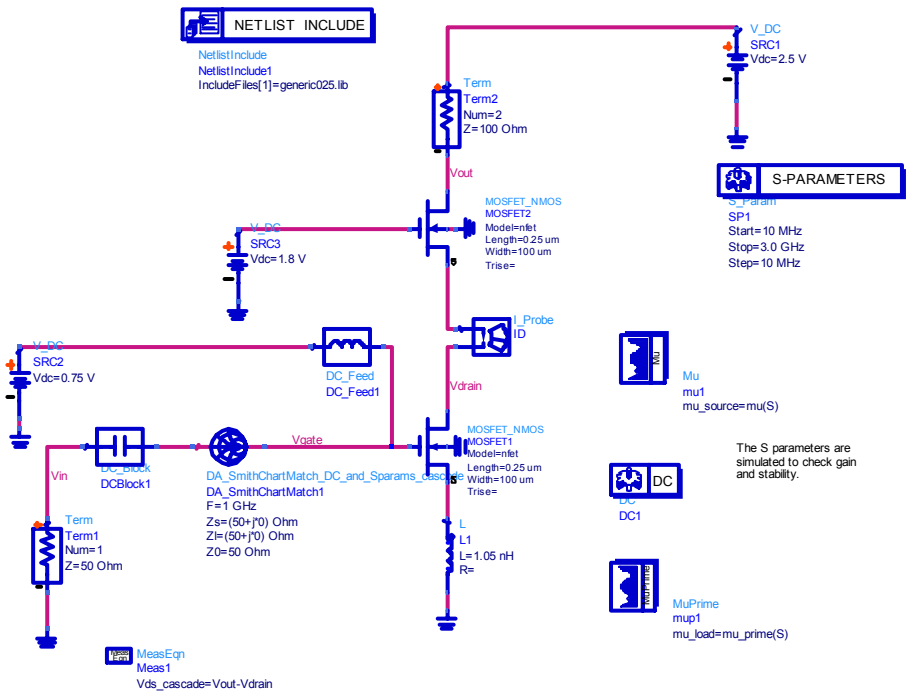
Improved isolation due to cascode stage (and thus stability)



Coil in source has right value, but inductive matching network needed

DC and S-parameter simulation: cascode LNA

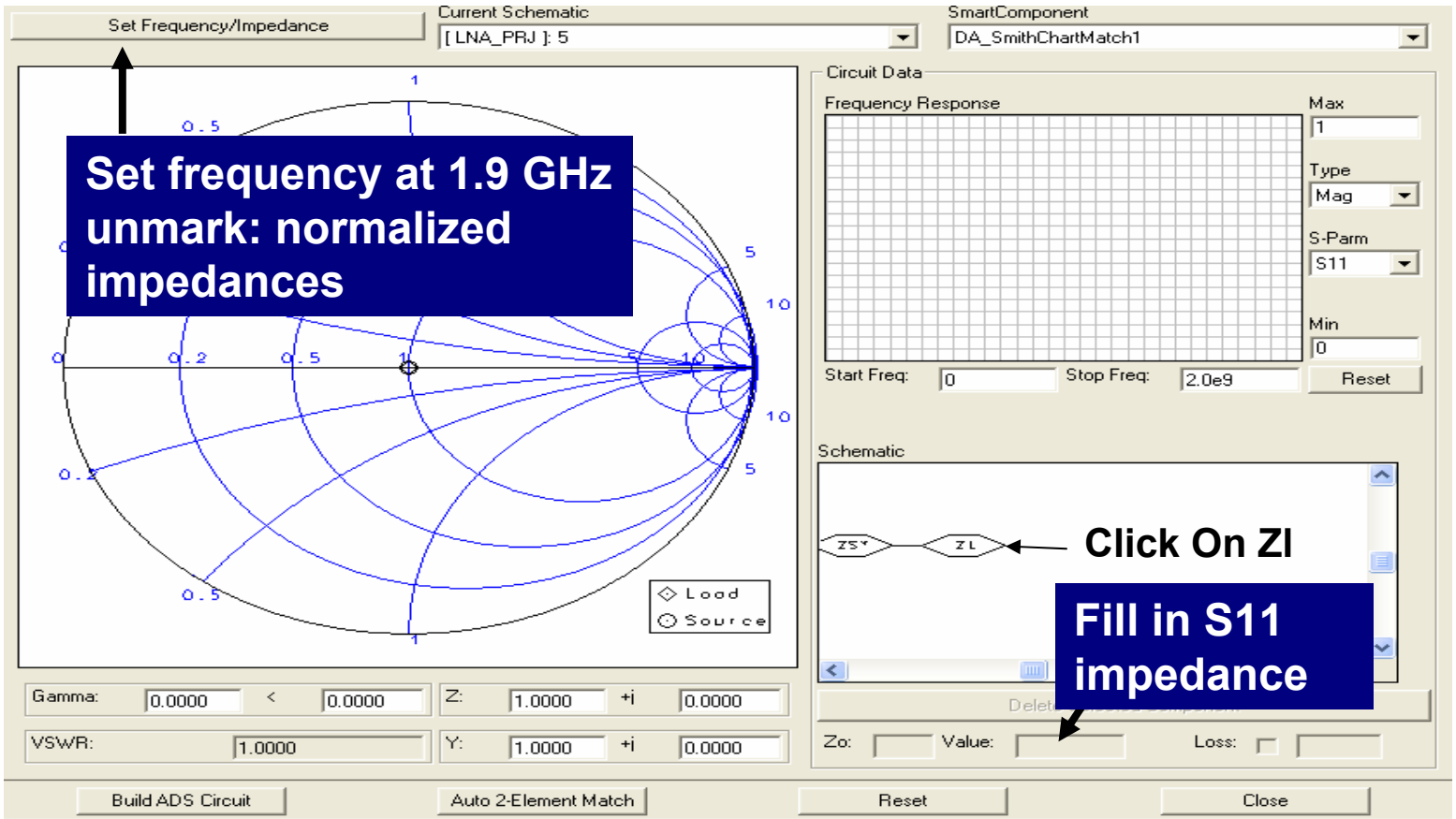
- Same schematic but smith-chart component enabled



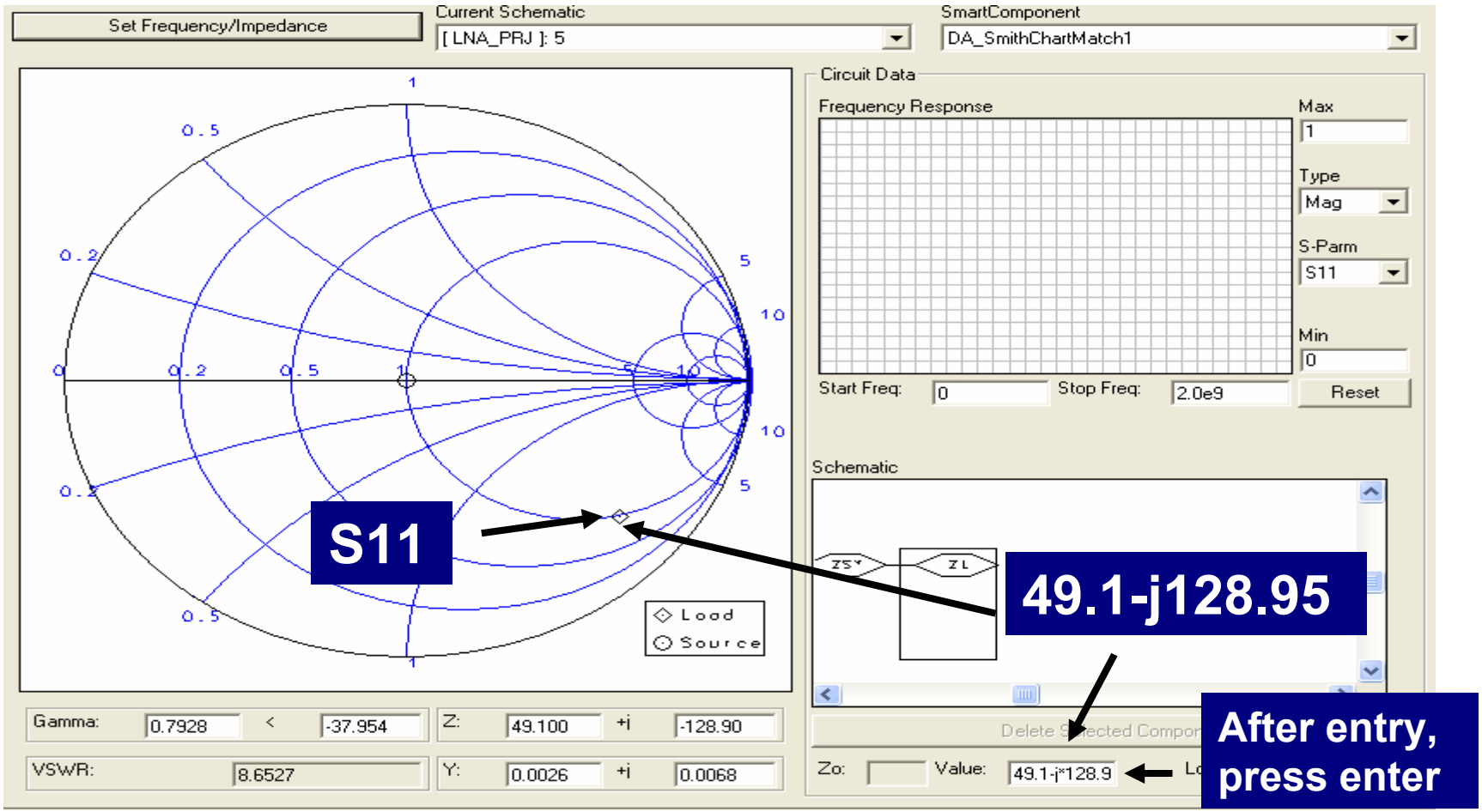
Schematic: DC_and_Sparams_cascode

Use design guide to match input (I)

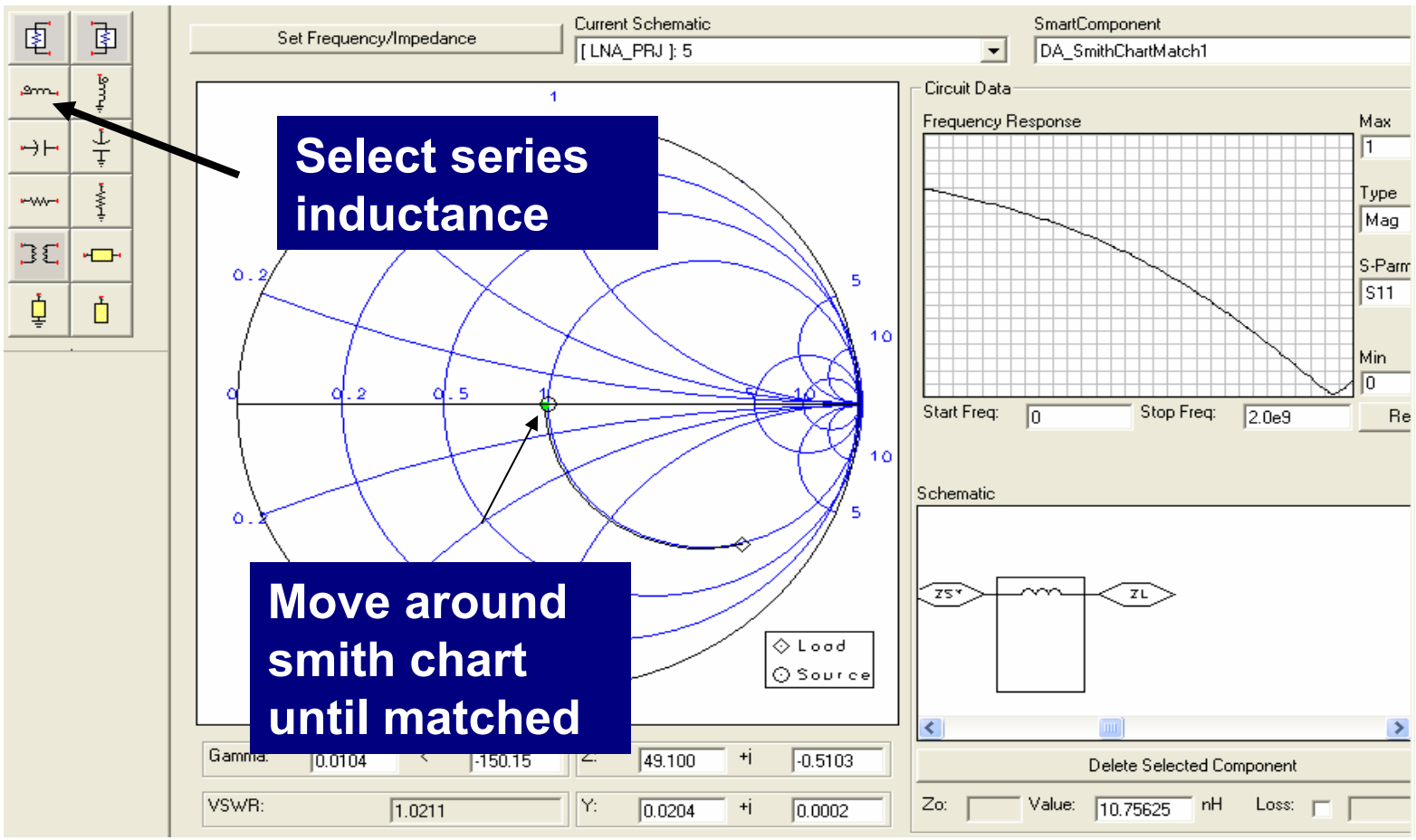
- **In schematic, ADS Menu: DesignGuide→filter→smith chart control window**



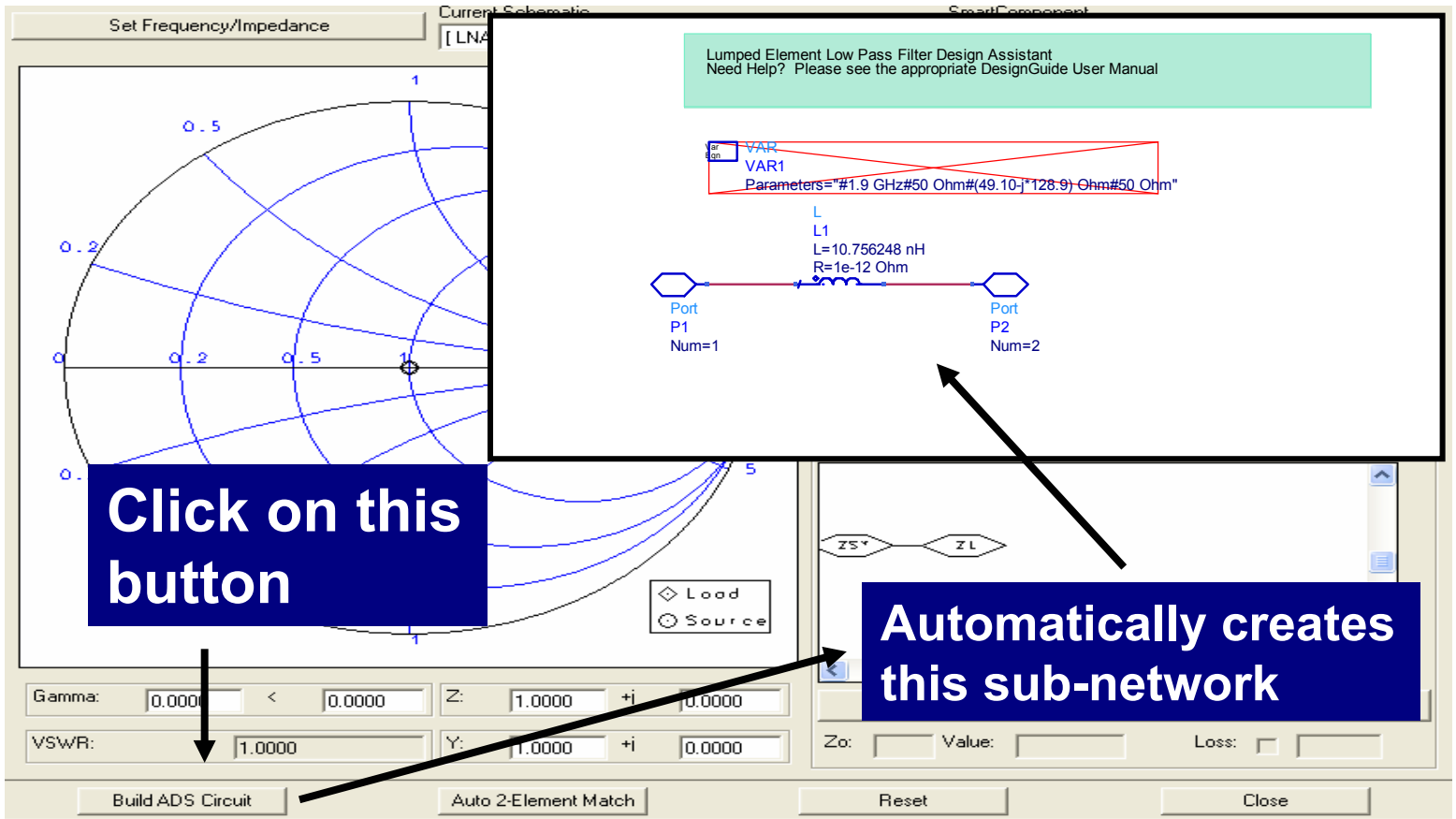
Use design guide to match input (II)



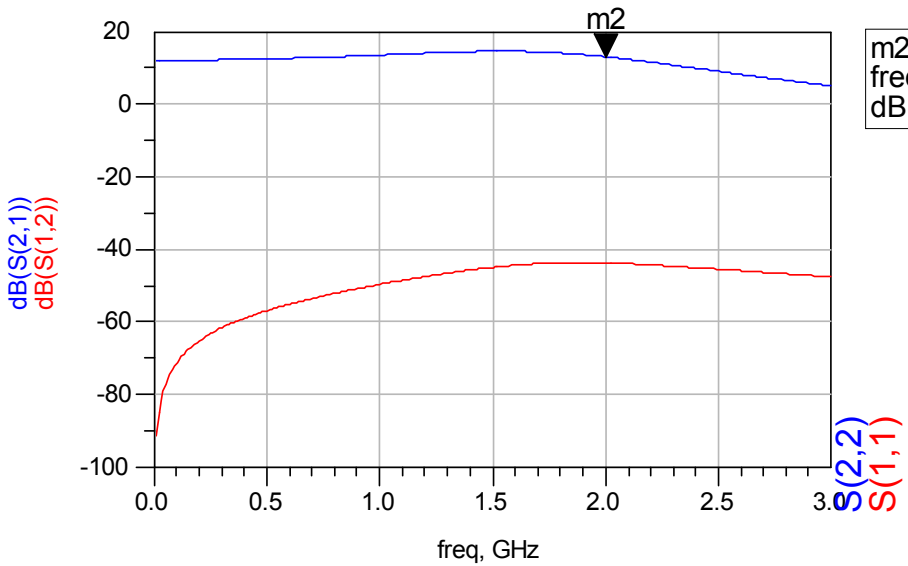
Use design guide to match input (III)

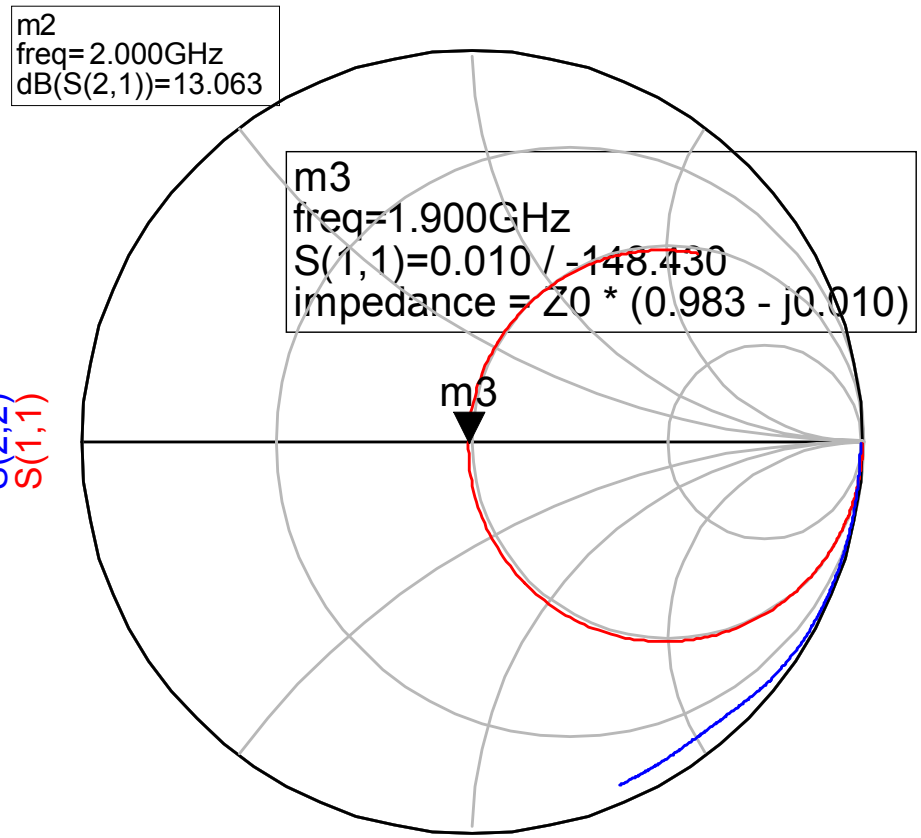


Last step: build ADS circuit



Repeat simulation of schematic: **DC_and_Sparams_cascode**

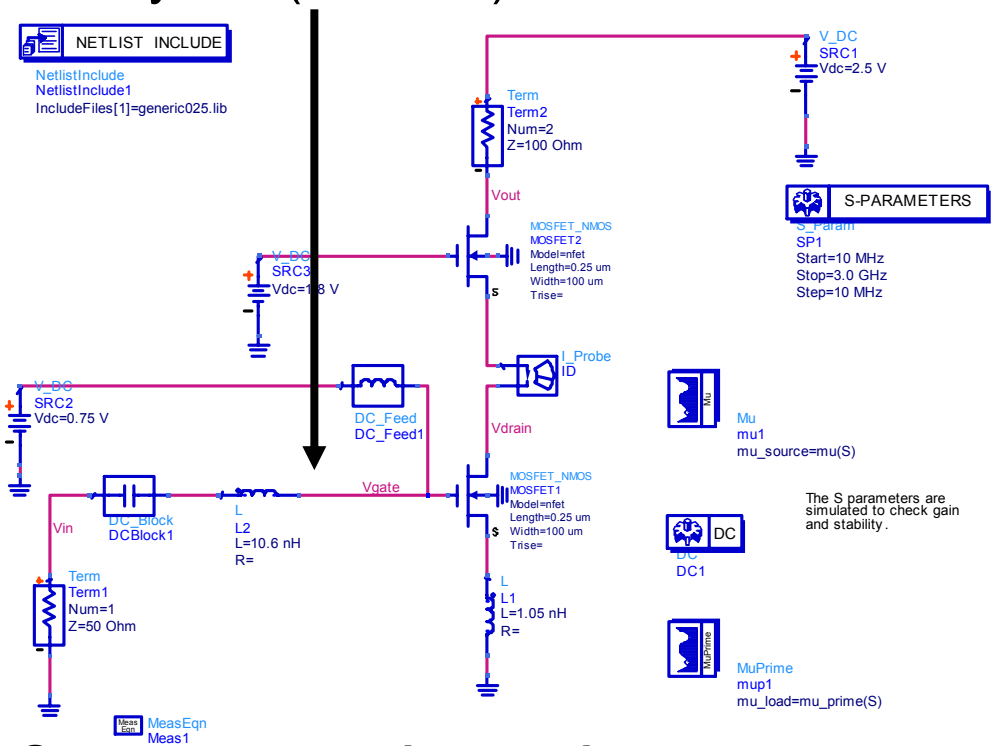




Improved gain (4 dB) and minimum return loss due to input matching.

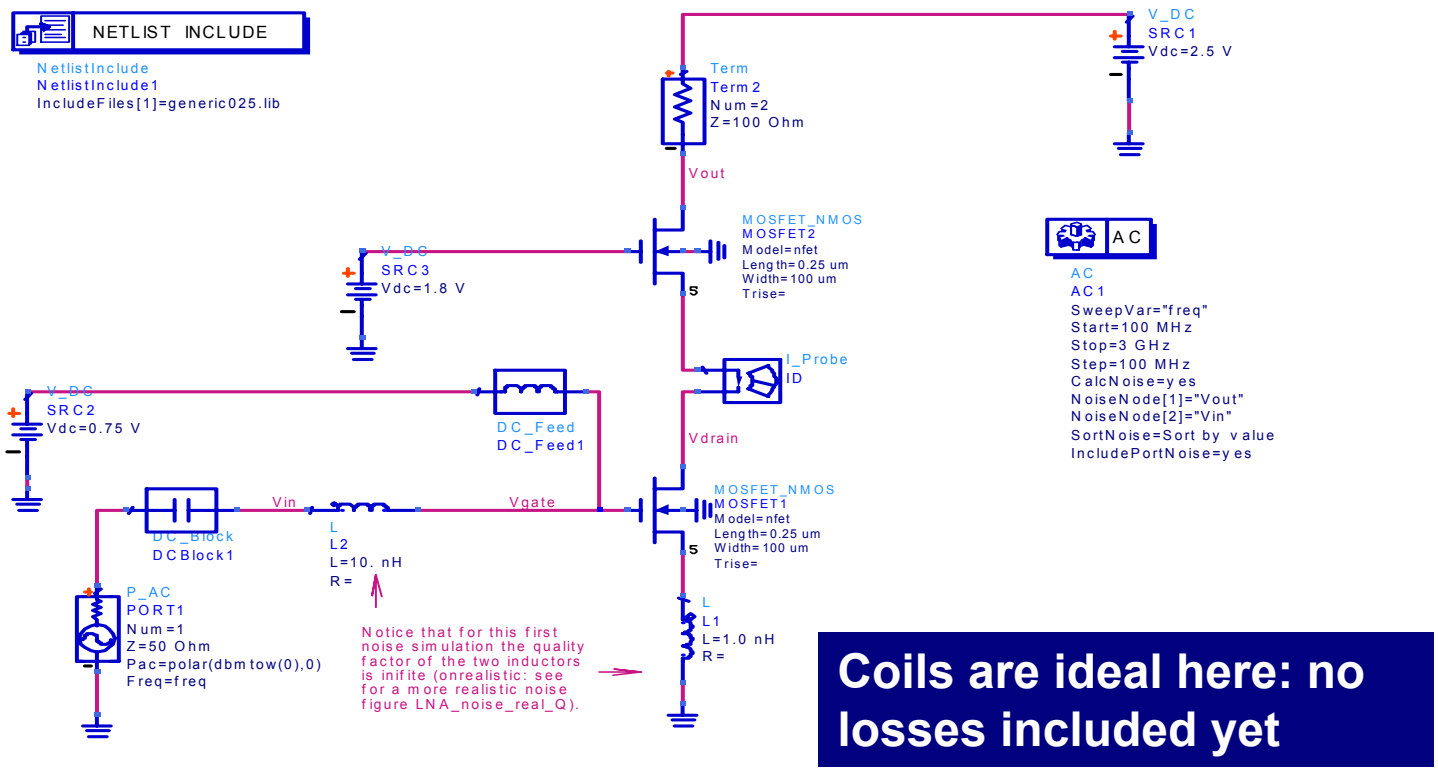
DC and S-parameter simulation: cascode LNA

- Same schematic as previous schematic but with smith chart component replaced by coil (~ 10 nH)



Schematic: DC_and_Sparams_cascode_match

AC simulation for noise figure

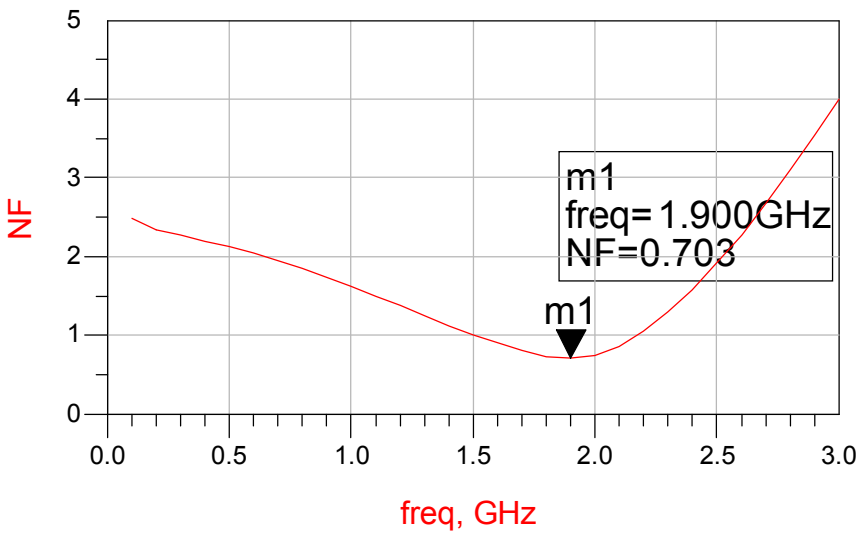


Schematic: LNA_noise

Example of simulation output

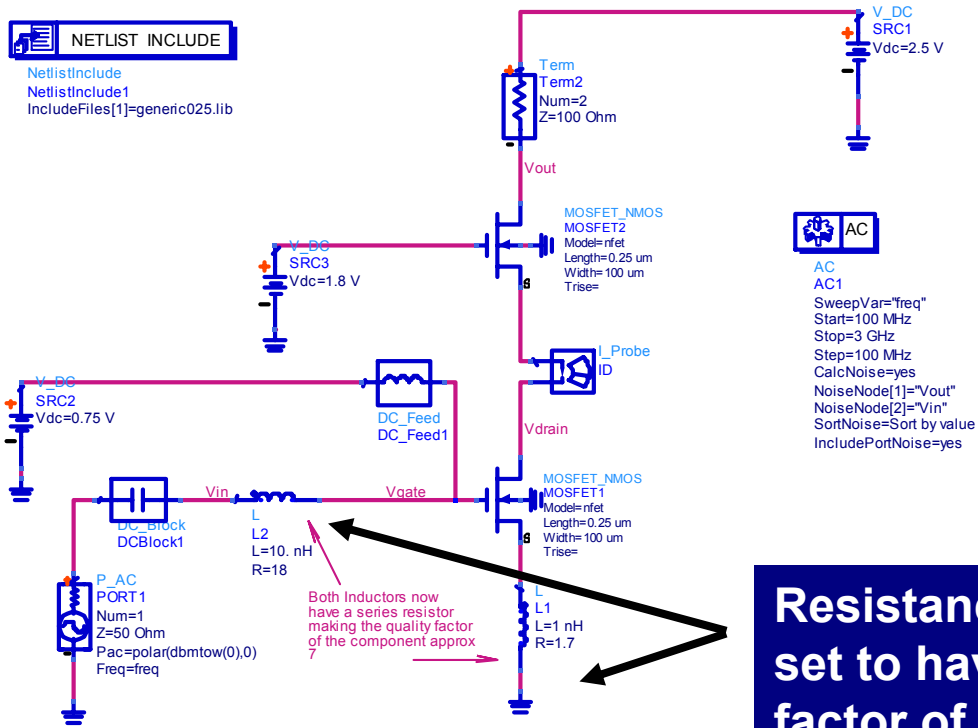
Eqn NF=20*log((Vout.noise/(mag(Vout/Vin)))/PORT1.t1.v.noise)

Measurement equation used to calculated the noise figure



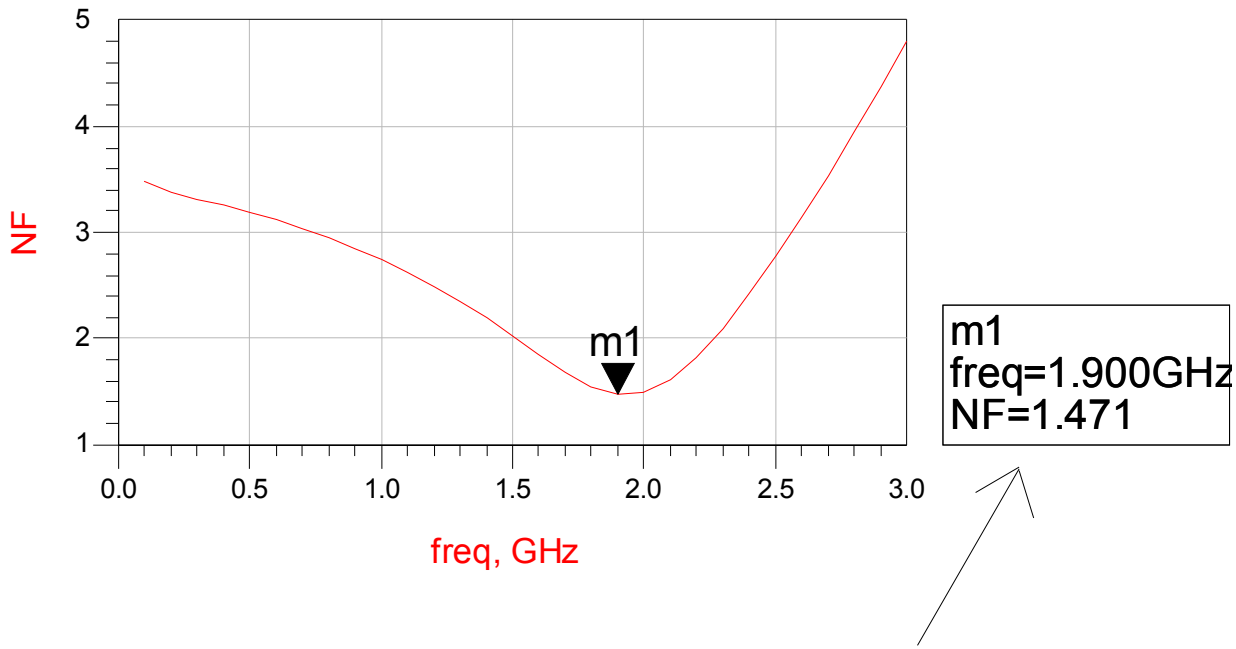
Noise figure versus frequency

AC simulation for noise figure with realistic coils



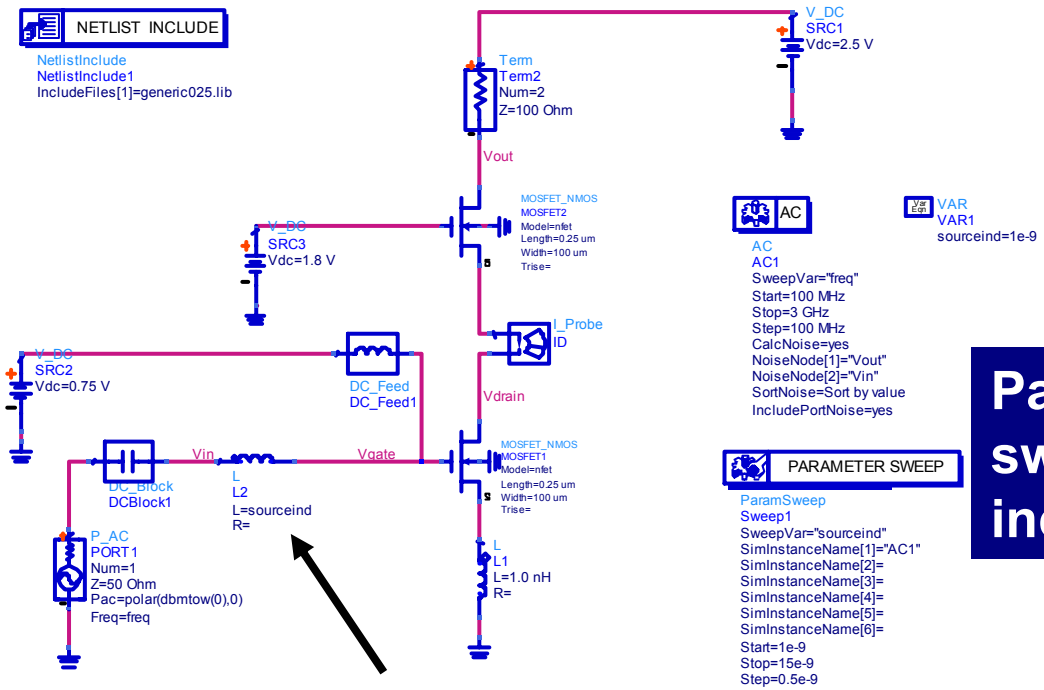
Schematic: LNA_noise_real_Q

Example of simulation output



Notice that the noise figure has degraded significantly due to the thermal noise of the series resistances in the inductors

Example of sweeping a parameter



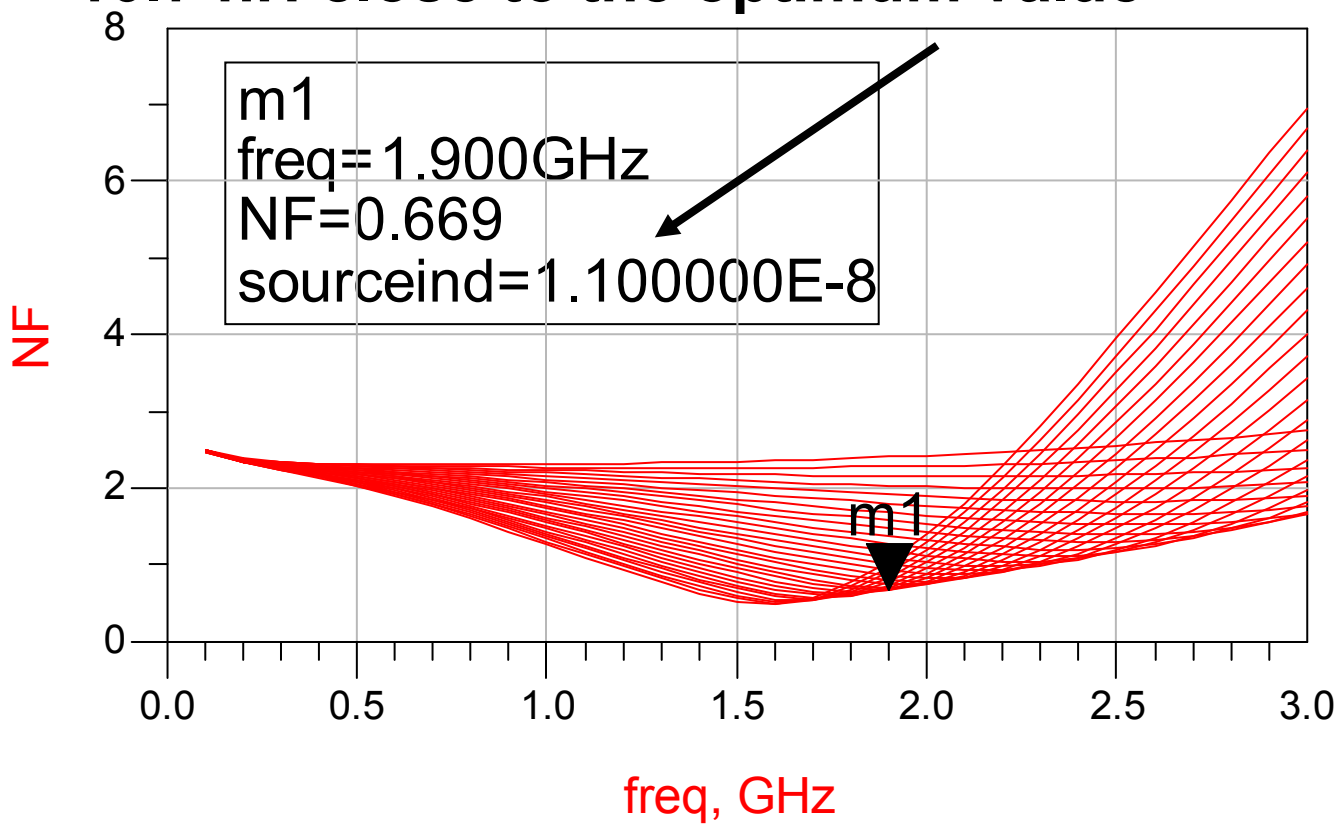
Parameter sweep block included

Schematic: LNA_noise_sweep

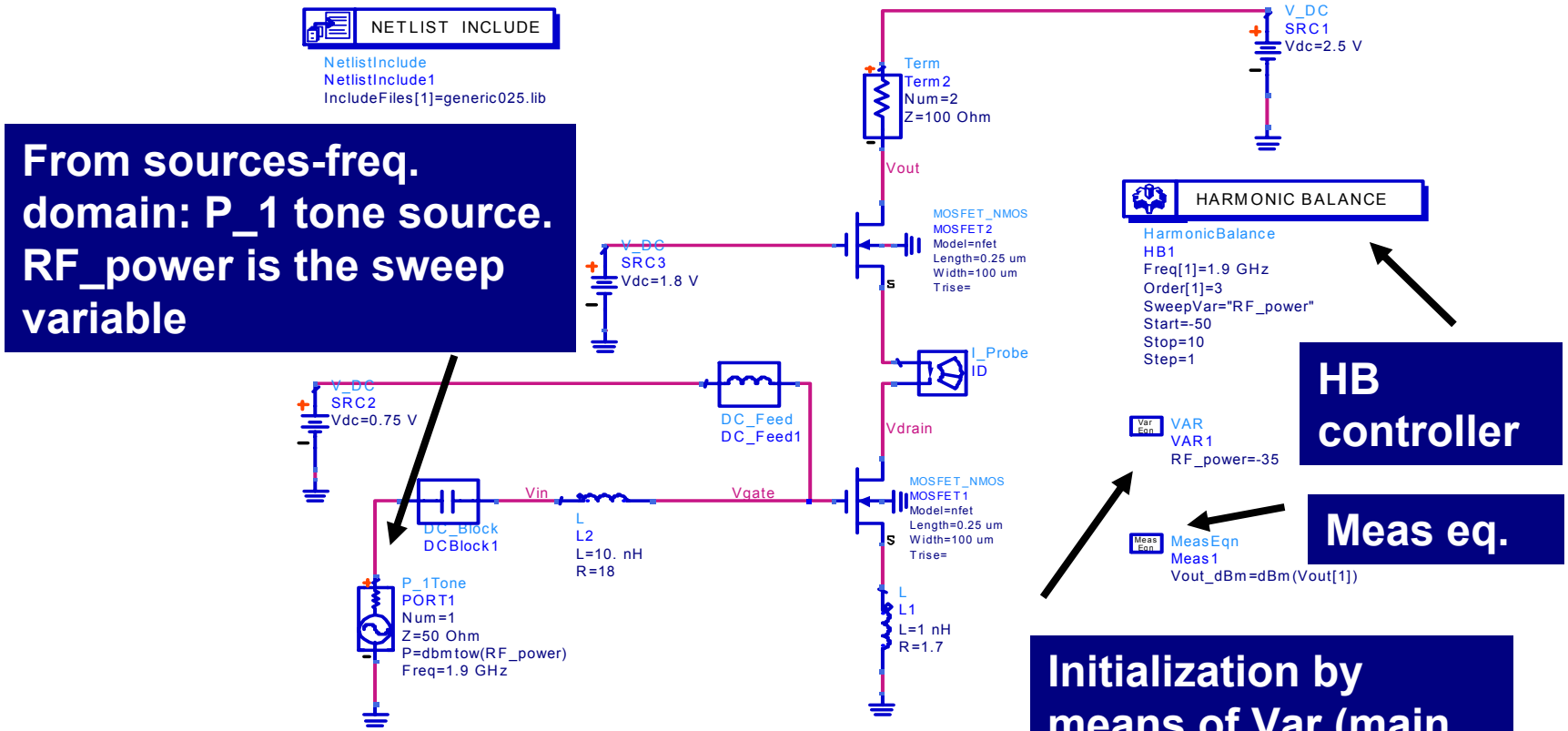
Matching inductor is varied from 1 to 15 nH (coils have infinite Q)

Example of simulation output

Lg ~ 10.7 nH close to the optimum value

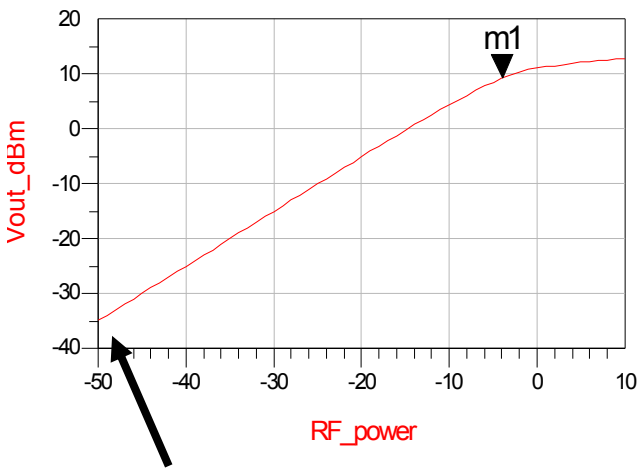


Gain and 1dB compression simulation



Schematic: LNA_1dB_by_power_sweep

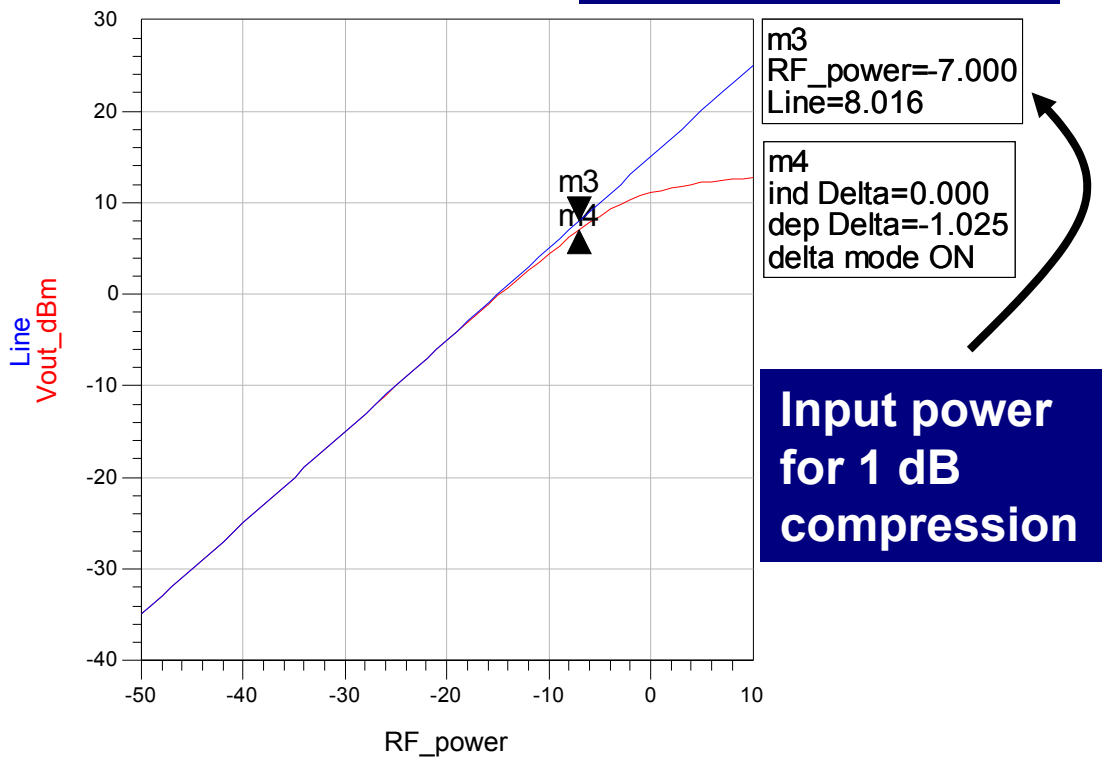
Example of simulation output



Voltage gain ~ 15 dB

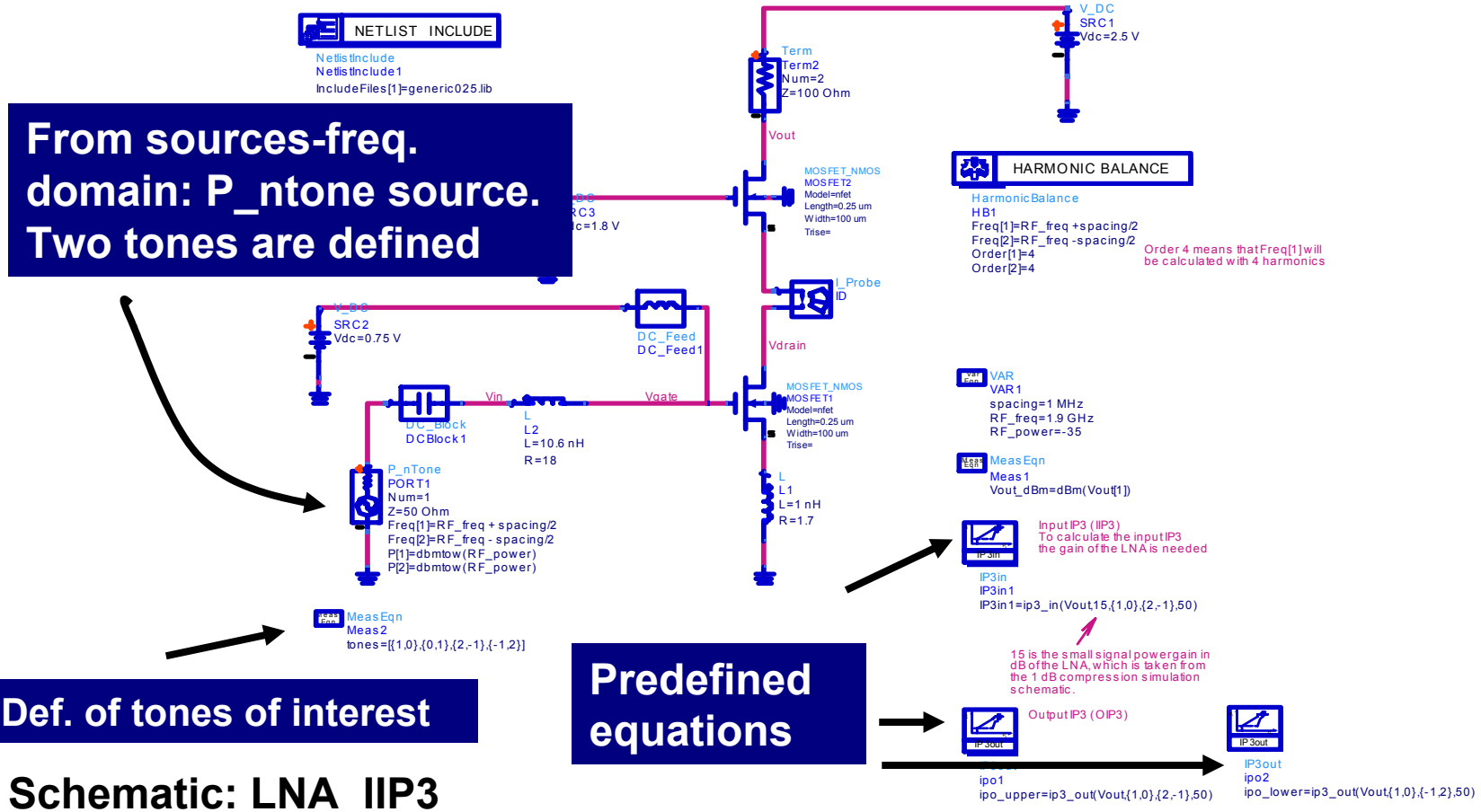
Eqn Line=RF_power+dB_gain[0]

Equation defining the line



Input power for 1 dB compression

Simulation of IIP3



Schematic: LNA_IIP3

Mix –function in ADS

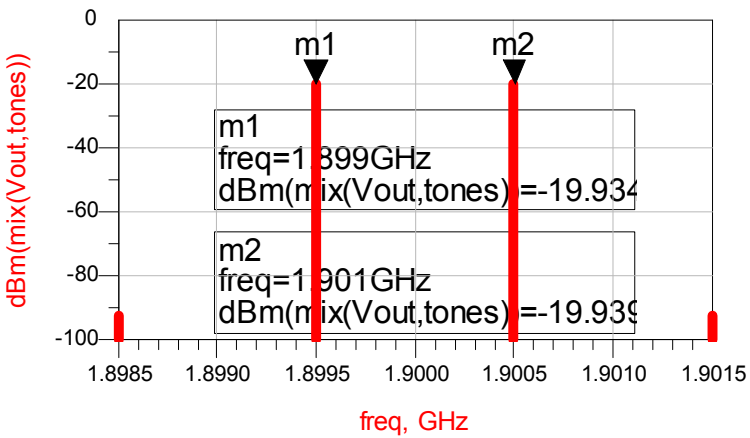
- **Purpose:** Returns a component of a spectrum based on a vector of mixing indices.

- **Synopsis**
  mix(xOut, harmIndex{, Mix})
  - where
  - *xOut* is a voltage or a current spectrum.
  - *harmIndex* is the desired vector of harmonic frequency indices (mixing terms).
  - *Mix* is a variable consisting of all possible vectors of harmonic frequency indices (mixing terms) in the analysis.
- **Example:** y = mix(vOut, {2, -1})

Example of simulation output

IP3in1	ipo_lower	ipo_upper
1.333	16.332	16.333

Notice that the upper and lower third order intercept points are almost symmetrical (ipo_upper and ipo_lower). The input IP3 (IP3in1) is simply 15 dB lower (the small signal gain) than the output IP3



freq	Mix	
	Mix(1)	Mix(2)
0.0000 Hz	0	0
1.000MHz	1	-1
2.000MHz	2	-2
1.898GHz	-1	2
1.899GHz	0	1
1.901GHz	1	0
1.902GHz	2	-1
3.798GHz	-1	3
3.799GHz	0	2
3.800GHz	1	1
3.801GHz	2	0
3.802GHz	3	-1
5.698GHz	0	3
5.699GHz	1	2
5.700GHz	2	1
5.702GHz	3	0
7.598GHz	0	4
7.599GHz	1	3
7.600GHz	2	2
7.601GHz	3	1
7.602GHz	4	0

This is the so-called mix table of the harmonic balance simulation. Number 1 represents the RF tone (with spacing). Zero means that no tone is present (DC). And two represents two times the RF simulation tone (of Freq[1] or Freq[2]).

Corresponding Course book pages

- Read and study:
  - **Chapter 3**

Circuit Design for RF Transceivers

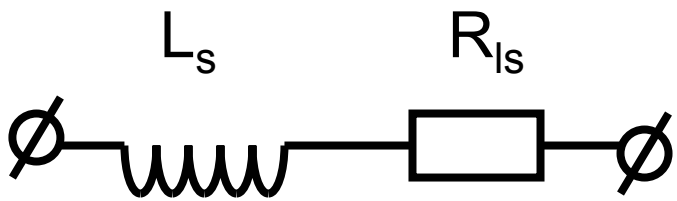
D. Leenaerts,
J. Van der Tang
C. Vaucher

Kluwer

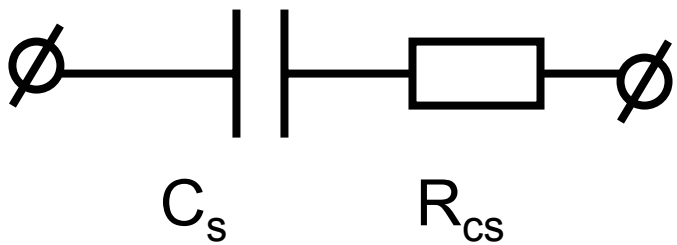
ISBN 0-7923-7551-3

Quality factors of matching components

In general: the quality factor of an (reactive) impedance (Z) is equal to imag(Z)/real(Z)



$$Q_L = \frac{\omega L_s}{R_{ls}}$$



$$Q_c = \frac{1}{\omega C_s R_{cs}}$$