Oscillator Design

- Introduction
  - What makes an oscillator?
- Types of oscillators
  - Fixed frequency or voltage controlled oscillator
  - LC resonator
  - Ring Oscillator
  - Crystal resonator
- Design of oscillators
  - Frequency control, stability
  - Amplitude limits
  - Buffered output – isolation
  - Bias circuits
  - Voltage control
  - Phase noise

Oscillator Requirements

- Power source
- Frequency-determining components
- Active device to provide gain
- Positive feedback

LC Oscillator $f_r = 1/2\pi\sqrt{LC}$

Hartley

Colpitts

Crystal

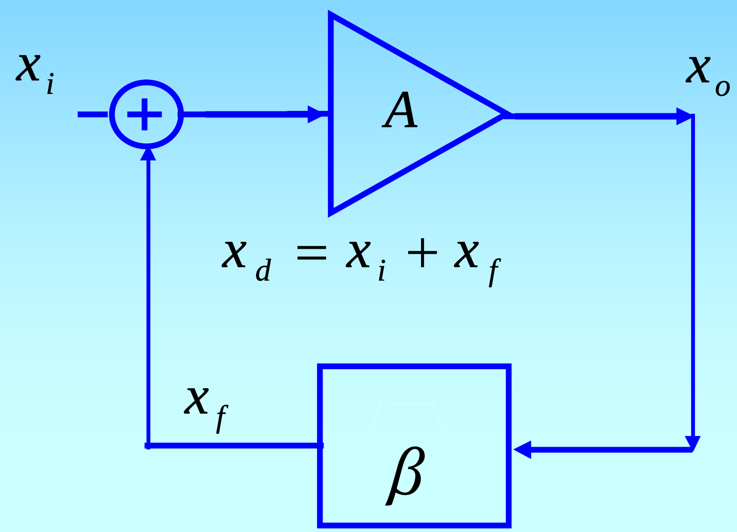
Clapp

RC

Wien-Bridge

Ring

Feedback Model for oscillators



$$A_f(j\omega) = \frac{A(j\omega)}{1 - A(j\omega)\cdot\beta(j\omega)}$$

Barkhausen criteria

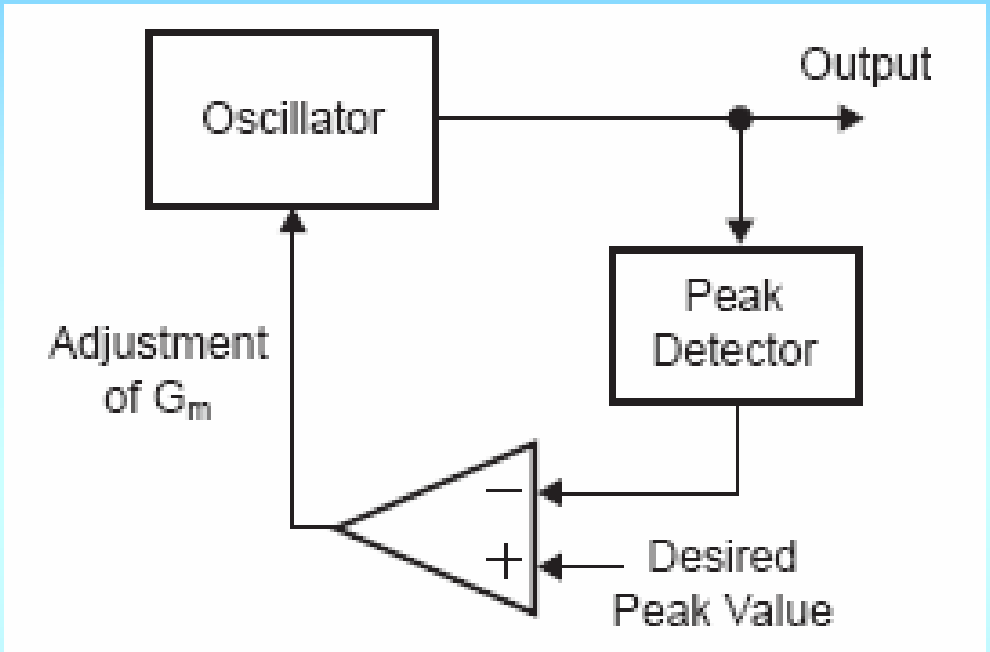
$$A(jw)\cdot b(j\omega) = 1$$

Barkhausen's criteria is necessary but not sufficient.
If the phase shift around the loop is equal to 360^o at zero frequency and the loop gain is sufficient, the circuit latches up rather than oscillate.

To stabilize the frequency, a frequency-selective network is added and is named as resonator.

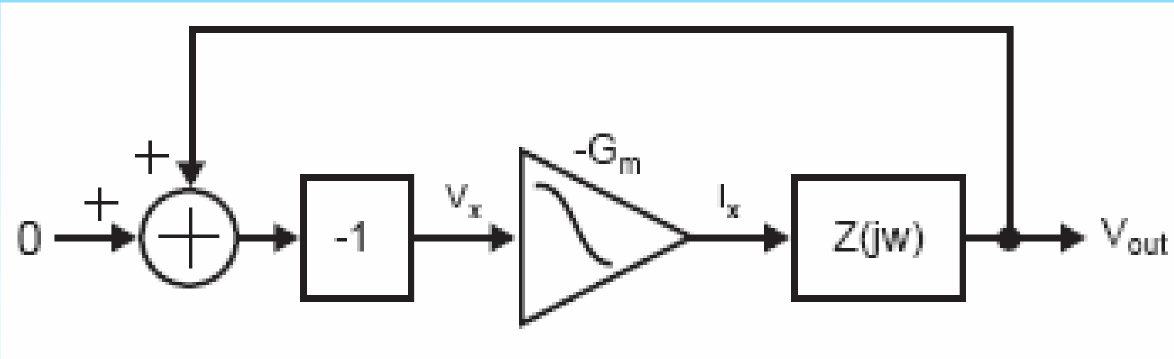
Automatic level control needed to stabilize magnitude

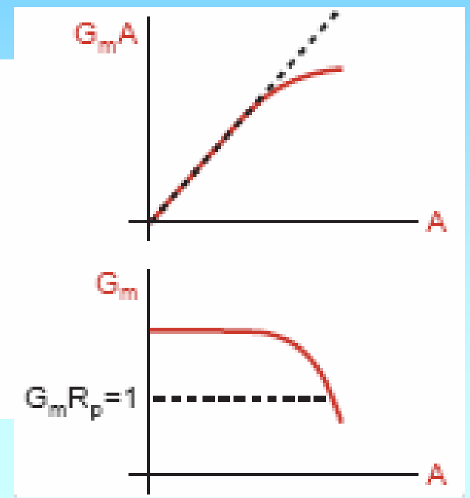
General amplitude control



- One thought is to detect oscillator amplitude, and then adjust Gm so that it equals a desired value
  - By using feedback, we can precisely achieve GmRp = 1
- Issues
  - Complex, requires power, and adds noise

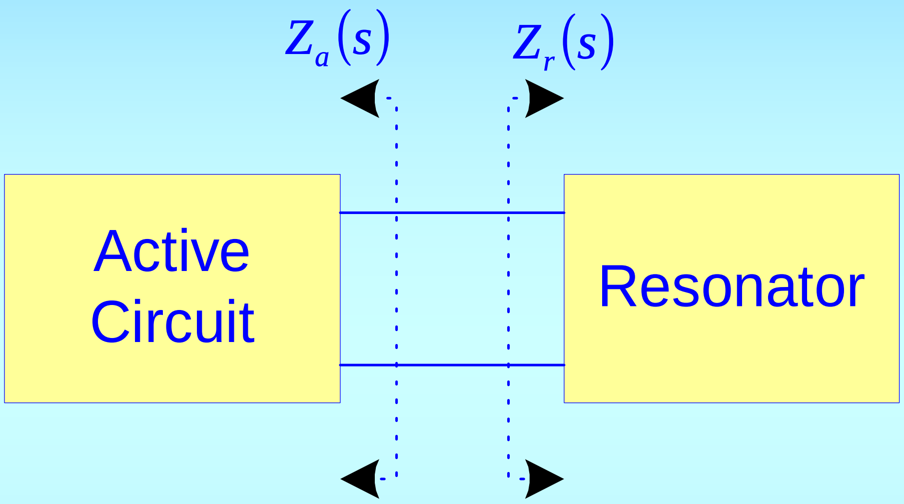
Leveraging Amplifier Nonlinearity as Feedback

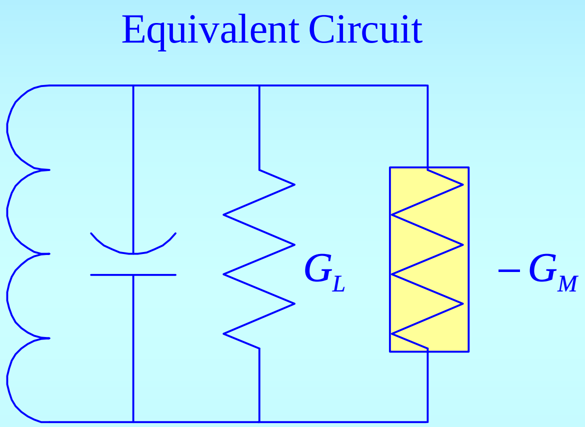




- Practical trans-conductance amplifiers have saturating characteristics
  - Harmonics created, but filtered out by resonator
  - Our interest is in the relationship between the input and the fundamental of the output
- As input amplitude is increased
  - Effective gain from input to fundamental of output drops
  - Amplitude feedback occurs! (GmRp = 1 in steady-state)

Negative-Resistance Model



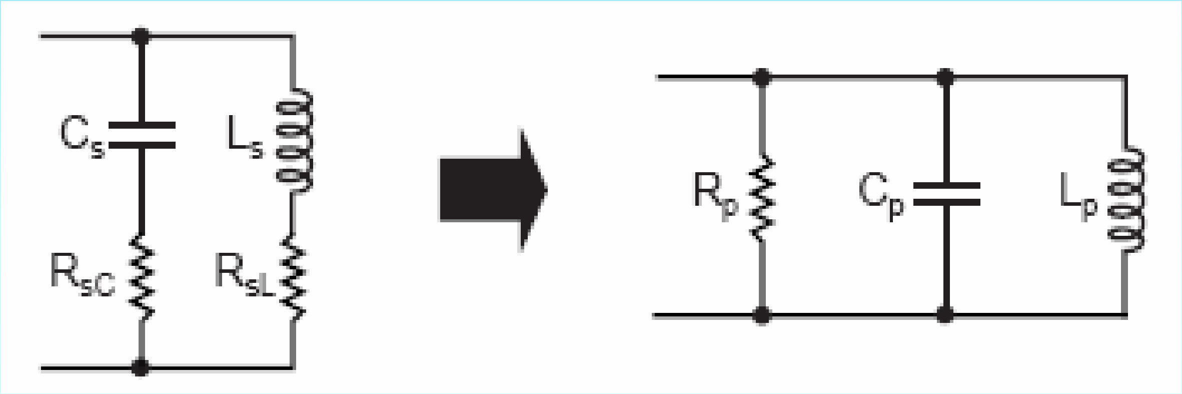


Oscillation:

$$\mathrm{Re}[Z_a(s)] + \mathrm{Re}[Z_r(s)] = 0$$

Resonator with series resisters

- Perform equivalent parallel conversion

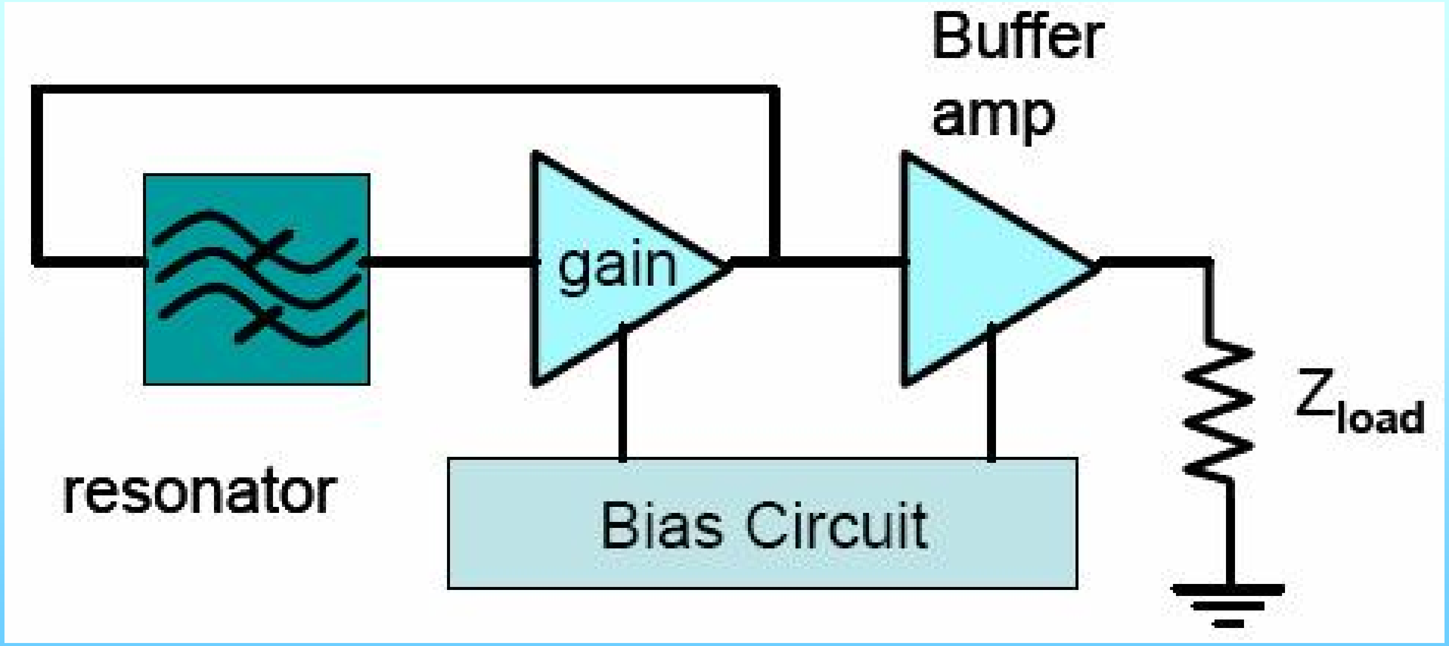


Warning: in practice, RLC networks can have secondary (or more) resonant frequencies, which cause undesirable behavior

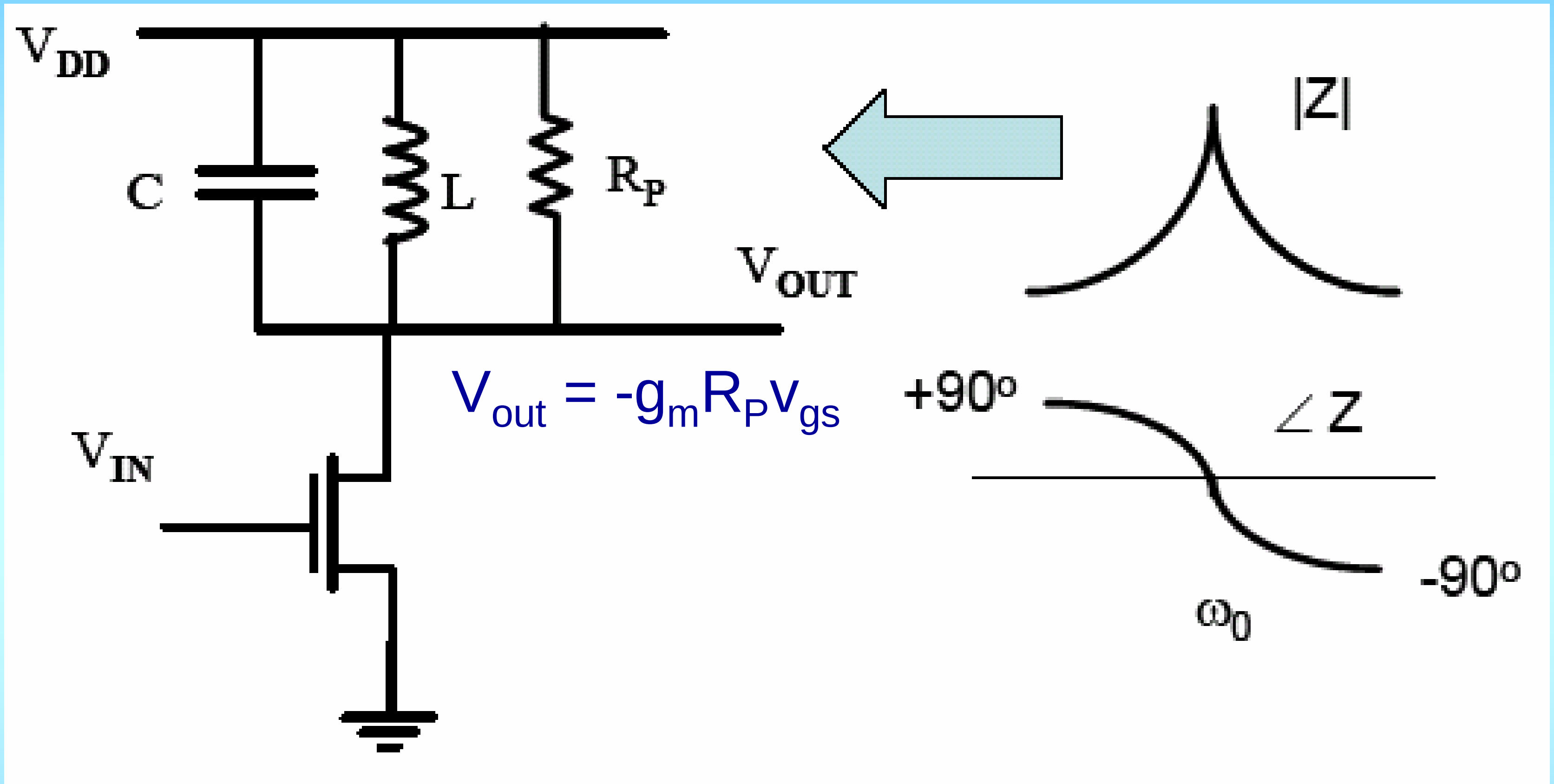
- Equivalent parallel network masks this problem in hand analysis
- Simulation will reveal the problem

LC Oscillators

- LC tank circuit as a resonator to control frequency.
- High Q resonator provides good stability, low phase noise
- Frequency adjusted by voltage using varactor diodes in the resonator.
- For oscillation to begin, open loop gain $A\beta \geq 1$.



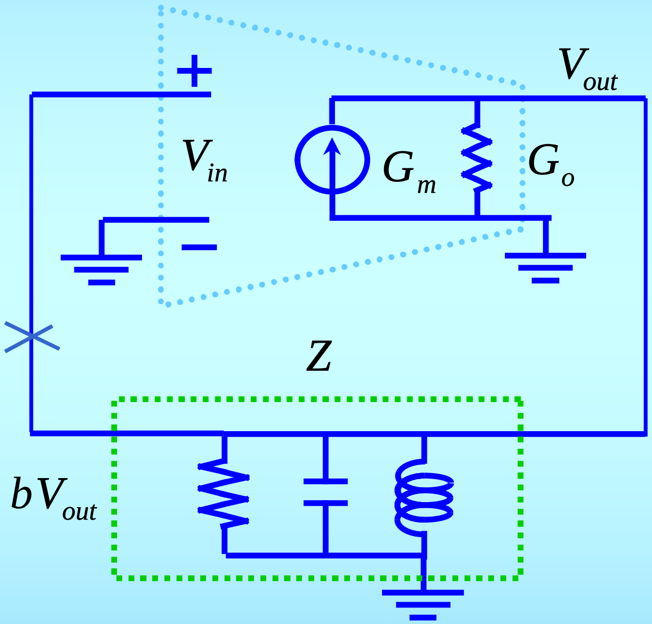
Tuned Amplifier



The impedance of the resonator peaks (= Rp) and the phase is 0° at ω_0 . The susceptances of the L and C cancel at resonance.

PMOS Oscillator Model

$$Y = \frac{1}{R_L} + G_o + sC + \frac{1}{sL} = \frac{1}{R_P} + sC + \frac{1}{sL} = \frac{R_P LCs^2 + Ls + R_P}{R_P Ls}$$



Open loop transfer function:

$$\frac{G_m}{Y} = \frac{G_m R_P Ls}{R_P LCs^2 + Ls + R_P}$$

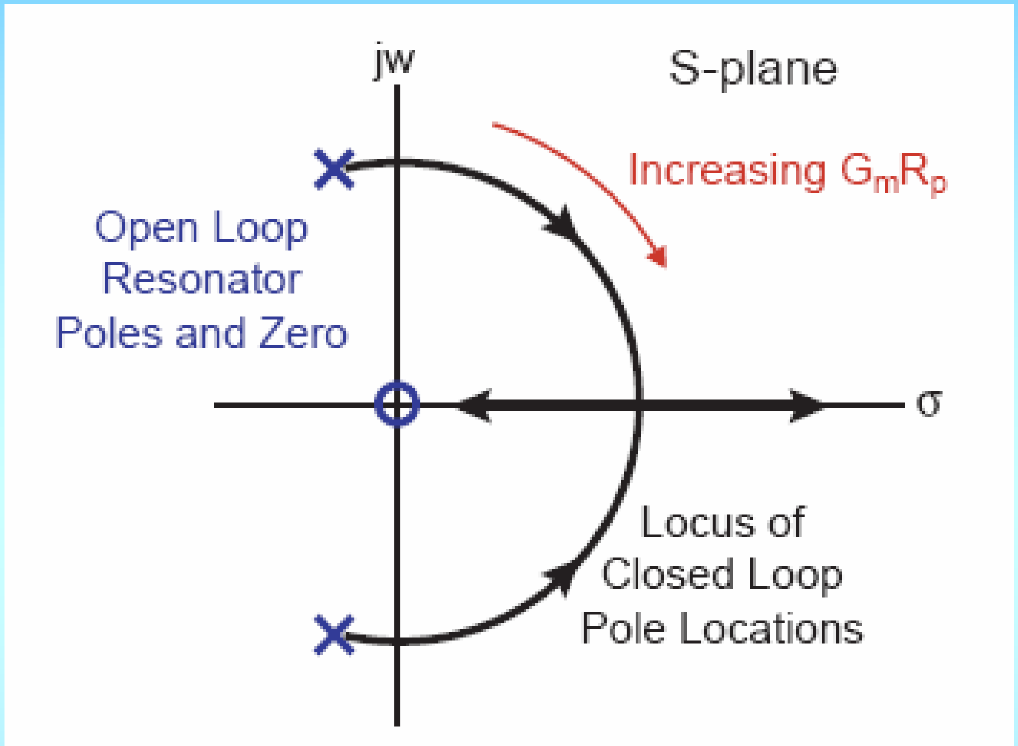
At resonance:

$$LCs^2 = -1 \qquad \frac{G_m}{Y} = \frac{G_m R_P Ls}{Ls} = G_m R_P$$

One zero at s=0

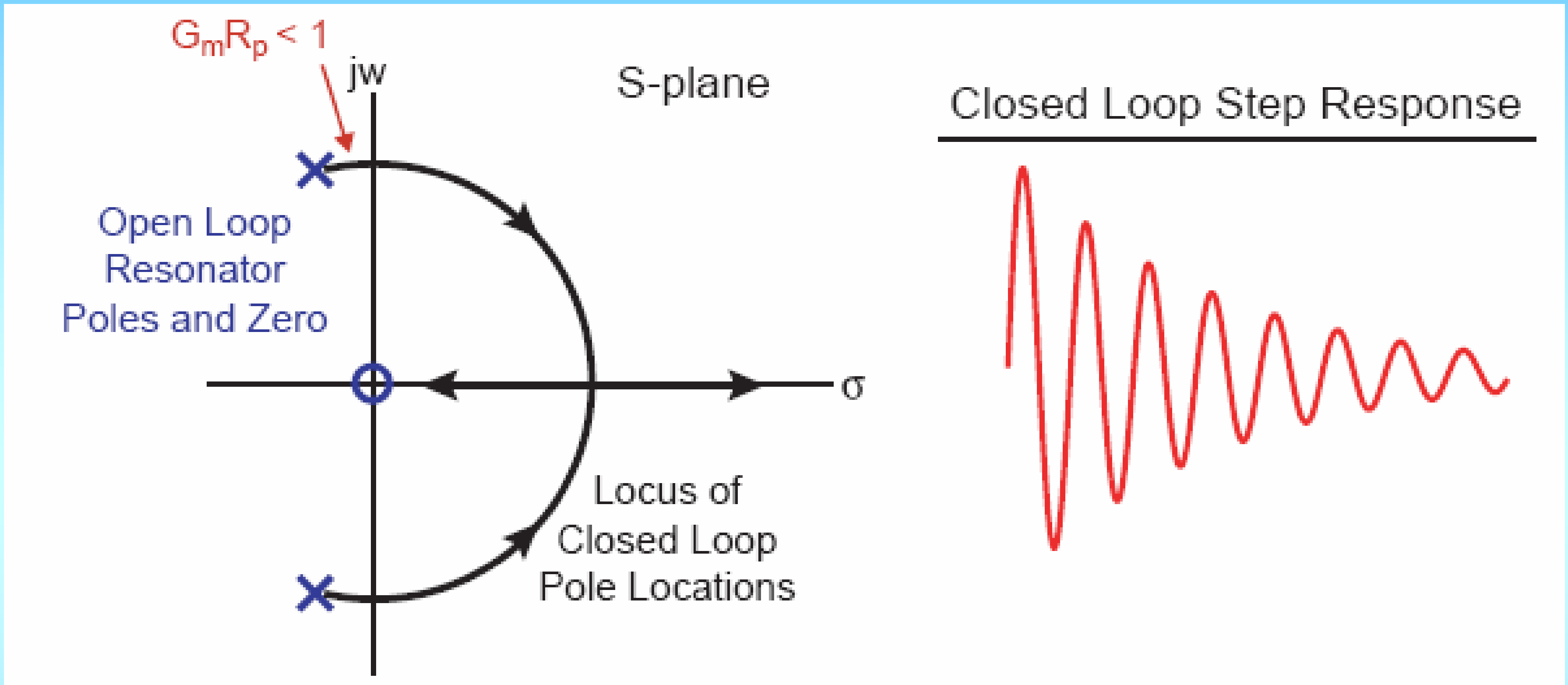
Two poles at: $s \approx -\frac{1}{2R_P C} \pm \frac{1}{\sqrt{LC}}$

Closed loop root locus as G_m changes



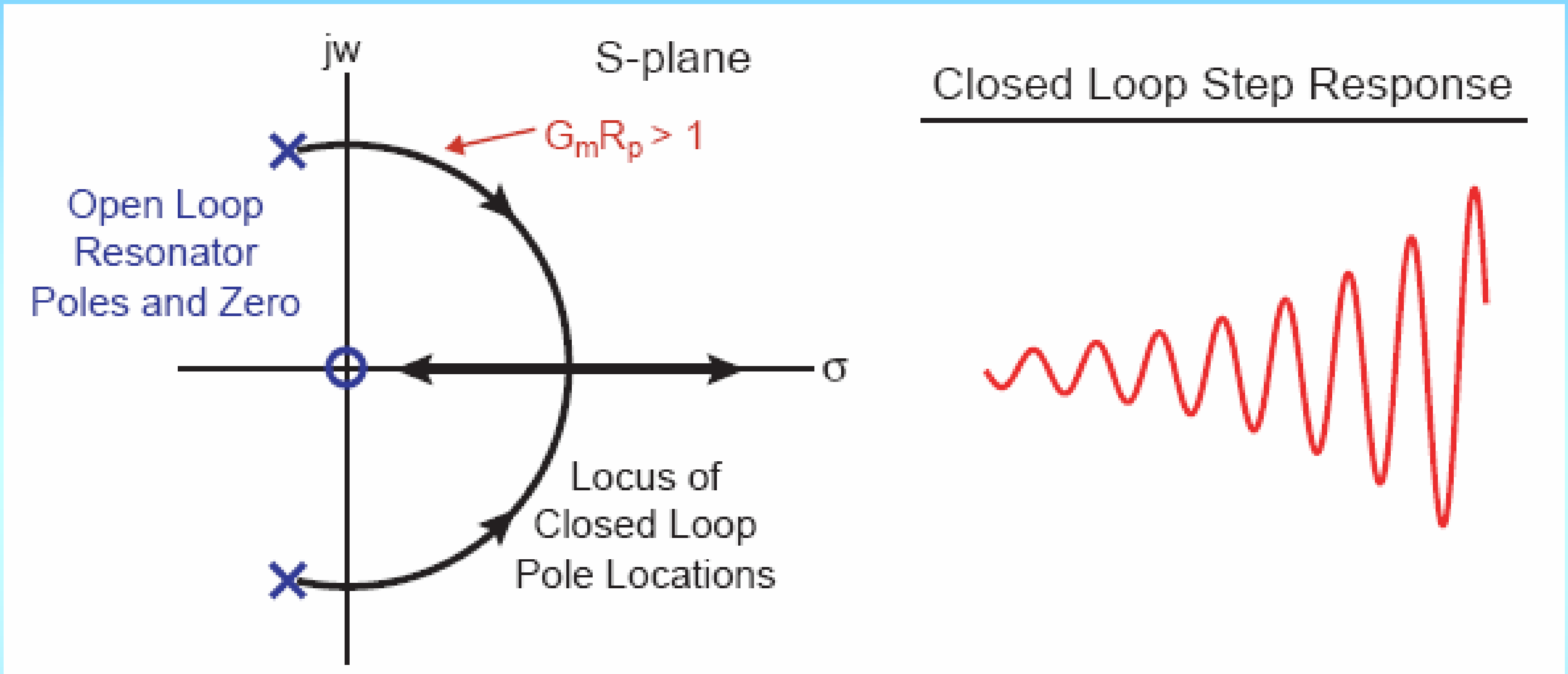
- Root locus plot allows us to view closed loop pole locations as a function of open loop poles/zero and open loop gain (GmRp)
- As gain (GmRp) increases, closed loop poles move into right half S-plane

When $G_mR_P < 1$



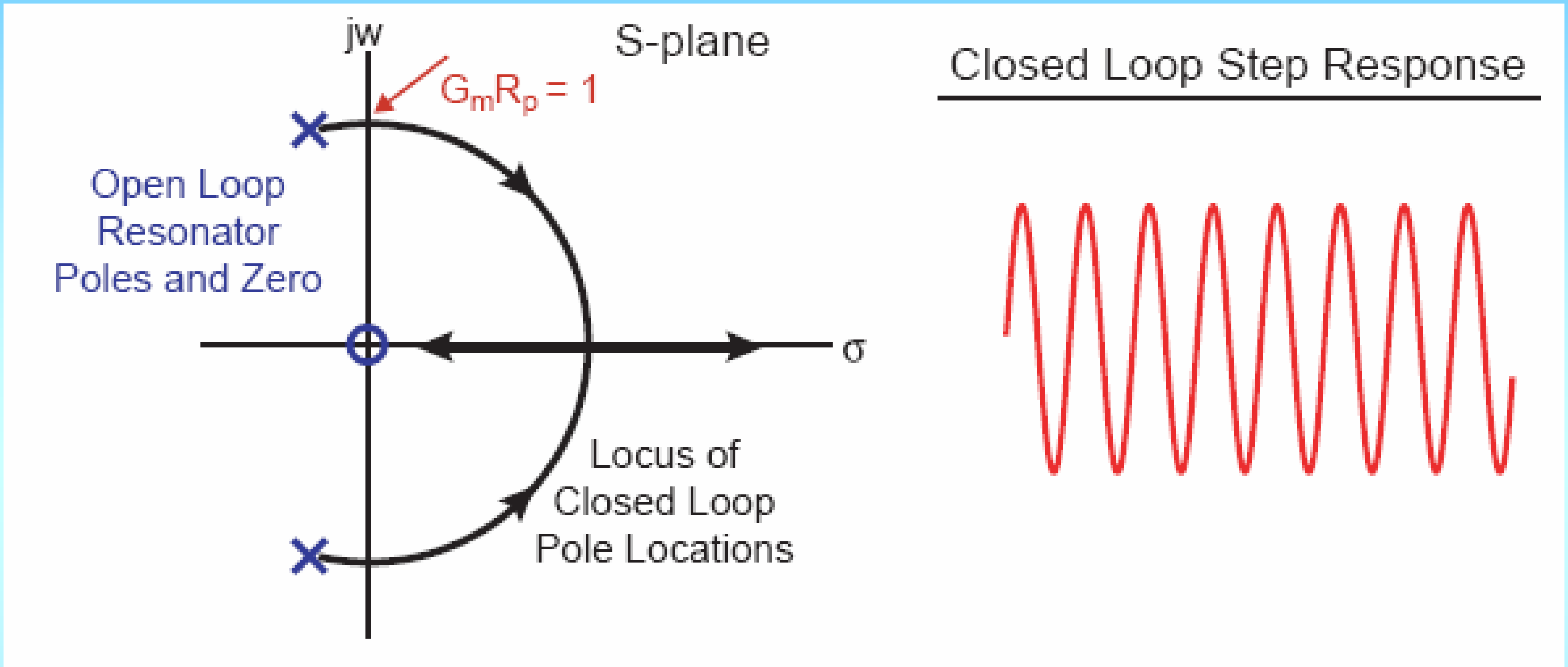
- Closed loop poles end up in the left half S-plane
- Under-damped response occurs
  - Oscillation dies out

When $G_m R_P > 1$



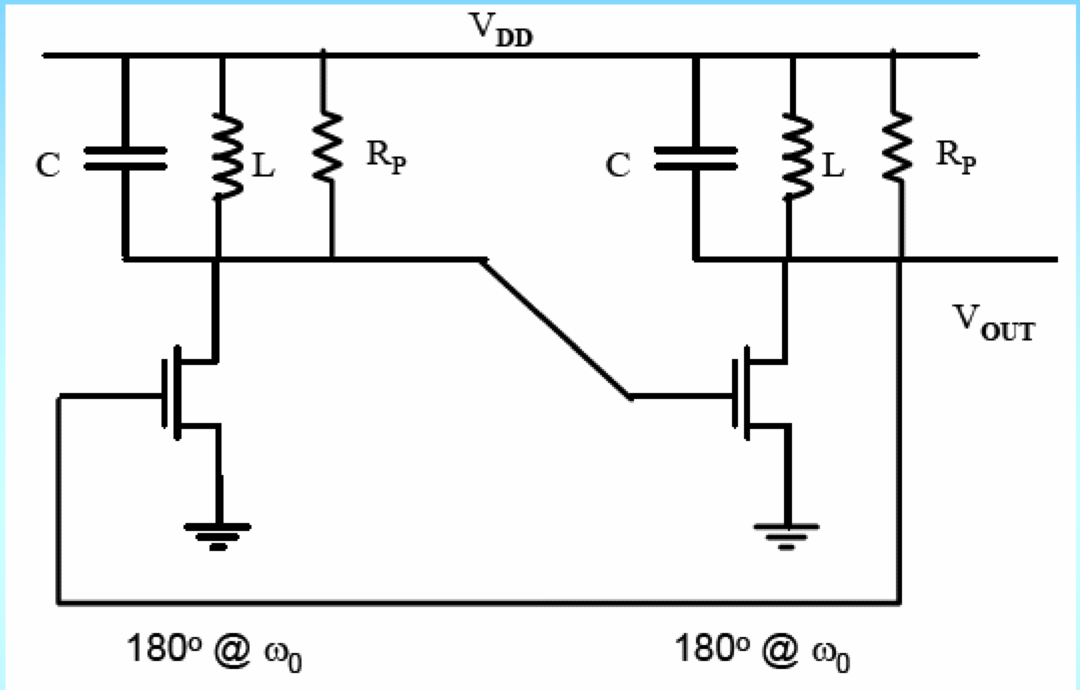
- Closed loop poles end up in the right half S-plane
- Unstable response occurs
  - Waveform blows up!

When $G_mR_P = 1$



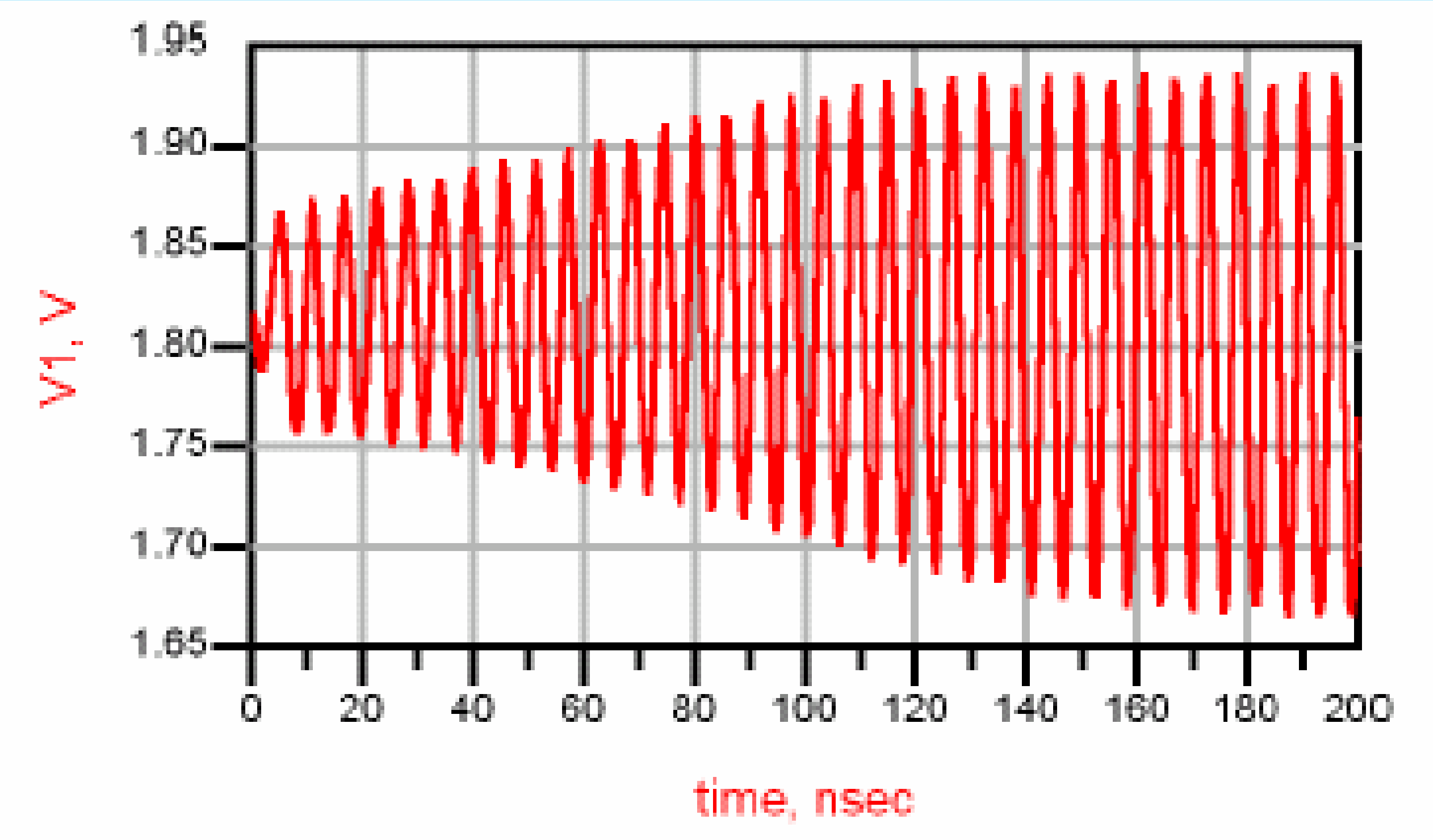
- Closed loop poles end up on jω axis
- Oscillation maintained
- Issues
  - G_mR_p needs to exactly equal 1, discussed earlier
  - How do we get positive feedback

Connect two in series and add feedback

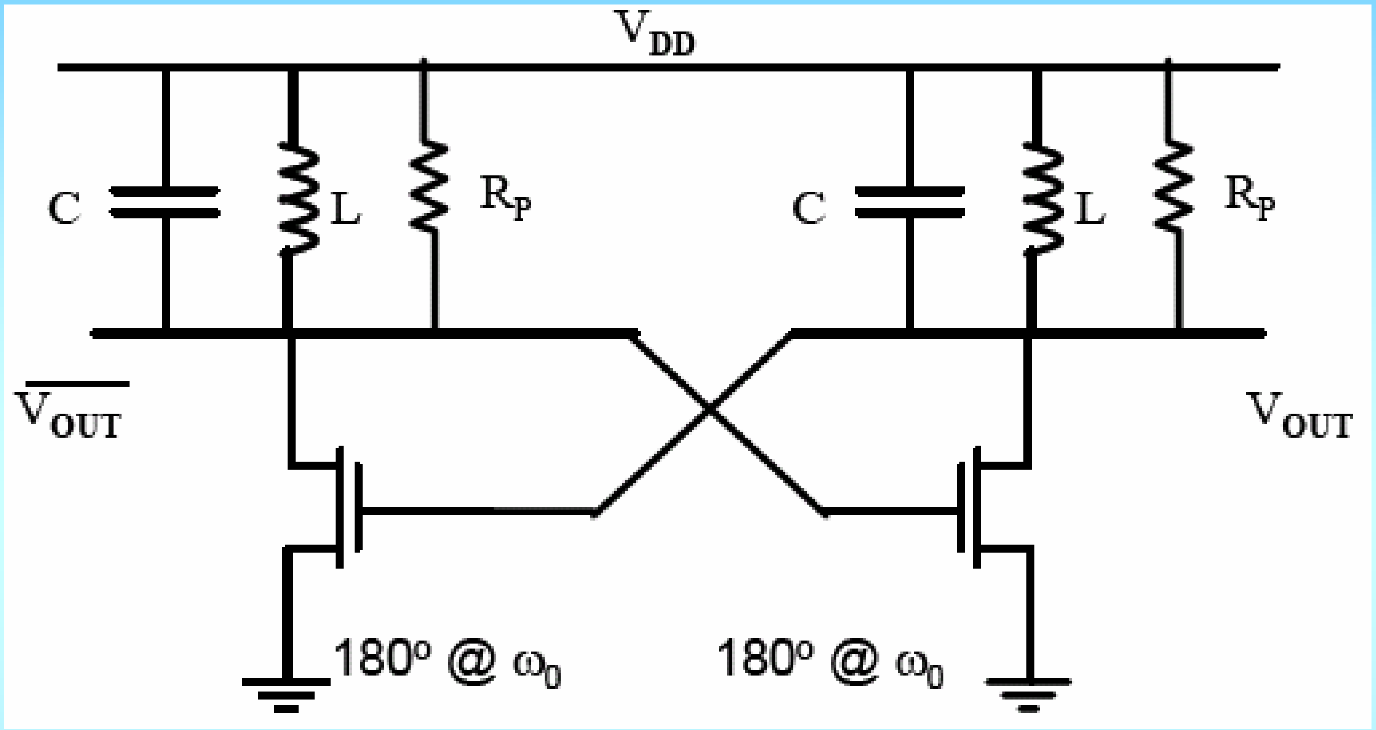


If $(g_m R_P)^2 \geq 1$, this circuit will oscillate. It can only oscillate at ω0, because only at that frequency will we have a total phase shift of 0º.
The oscillations will begin when the noise inherent in the transistors is amplified around the loop. The strength of the oscillations will build exponentially with time. The small signal analysis doesn't provide a limit to this growth. The amplitude will reach a limit either by voltage or current.

Time domain response

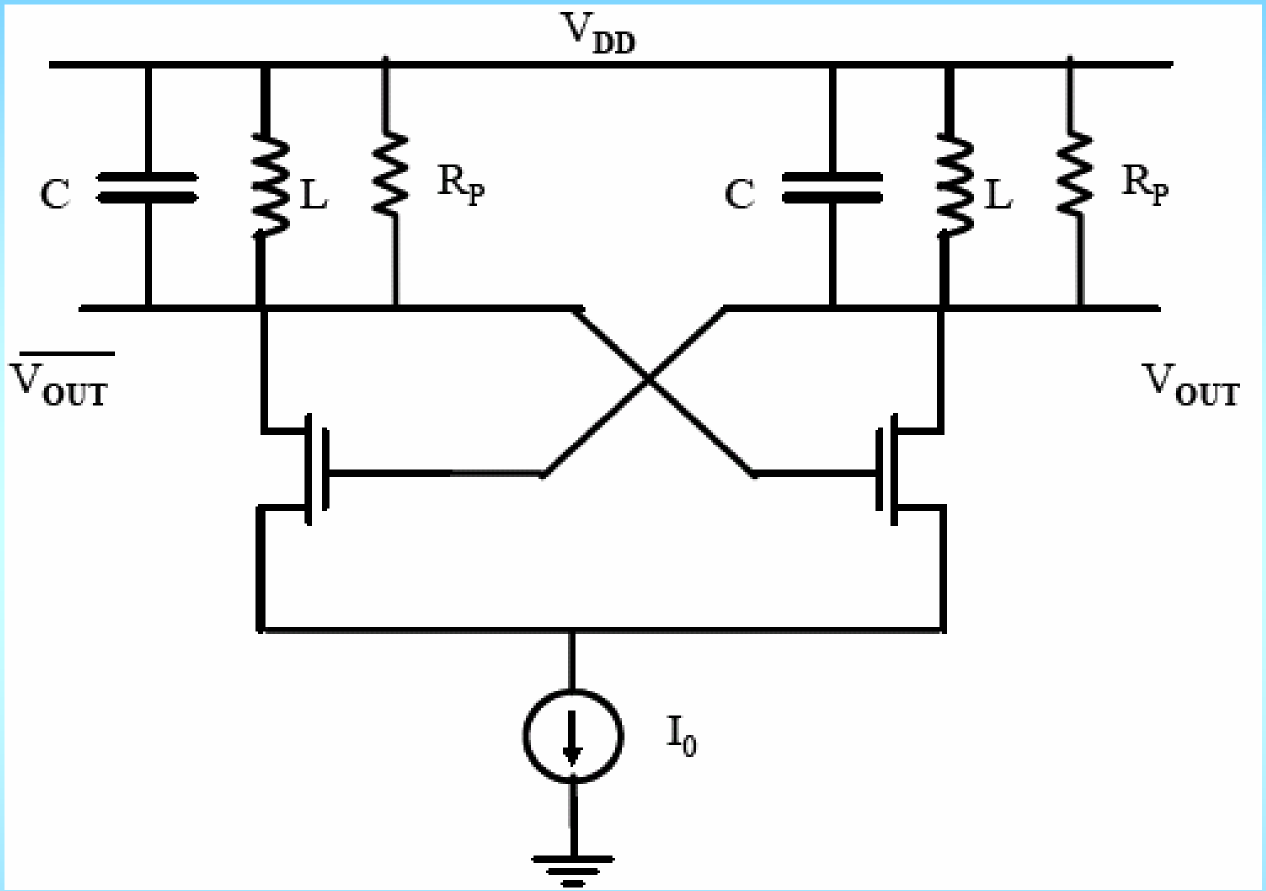


Cross-coupled Oscillator: Redrawn



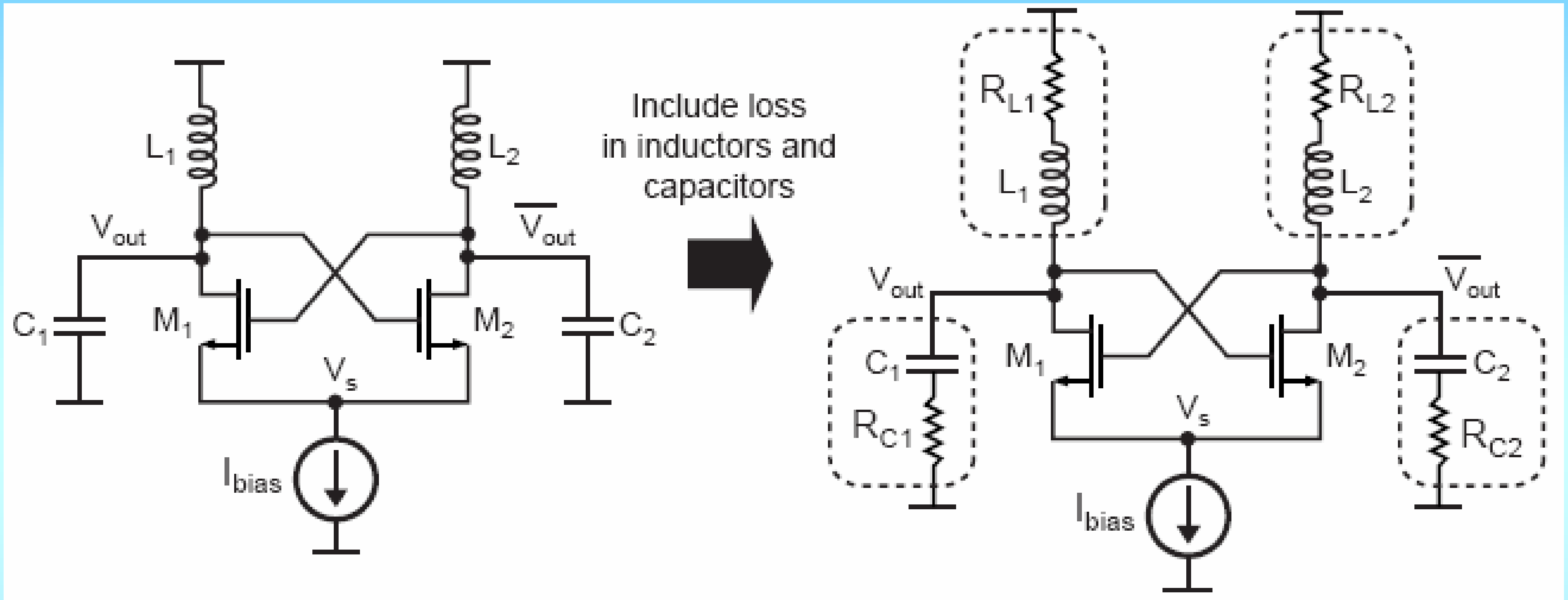
This representation emphasizes the differential topology. The two outputs are 180 degrees out of phase. This can be very useful for many applications – driving a Gilbert cell mixer, for example.

Cross-coupled pair with bias



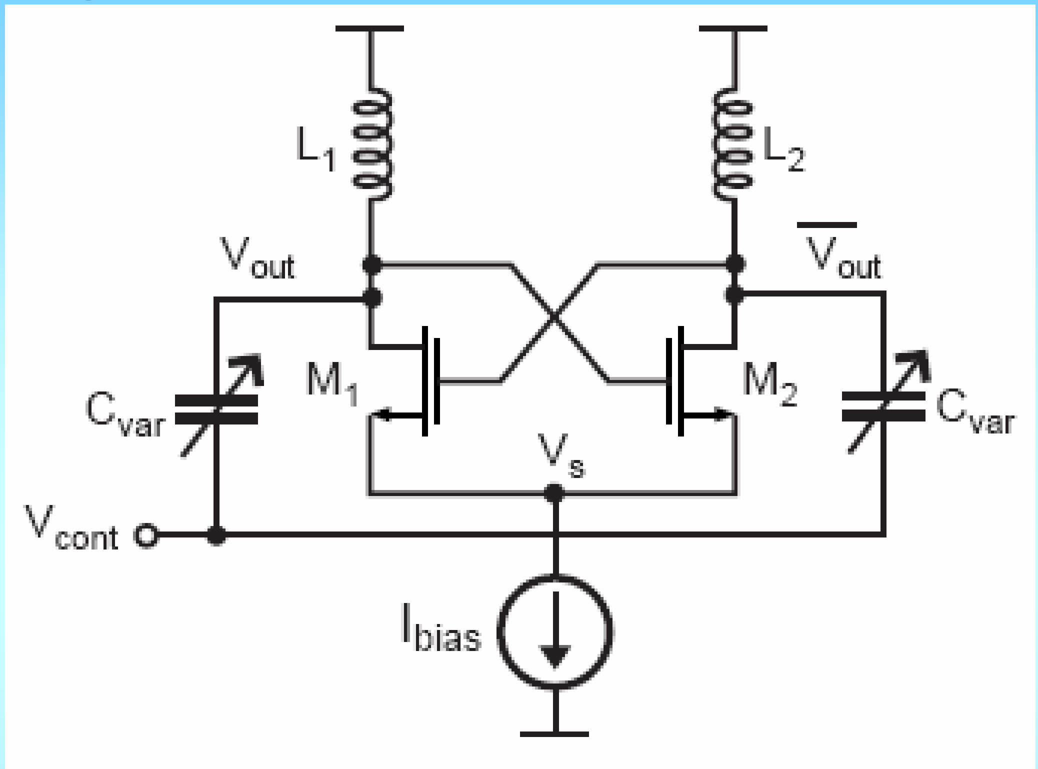
I_0 provides oscillation amplitude control
But it adds noise.

A popular LC oscillator



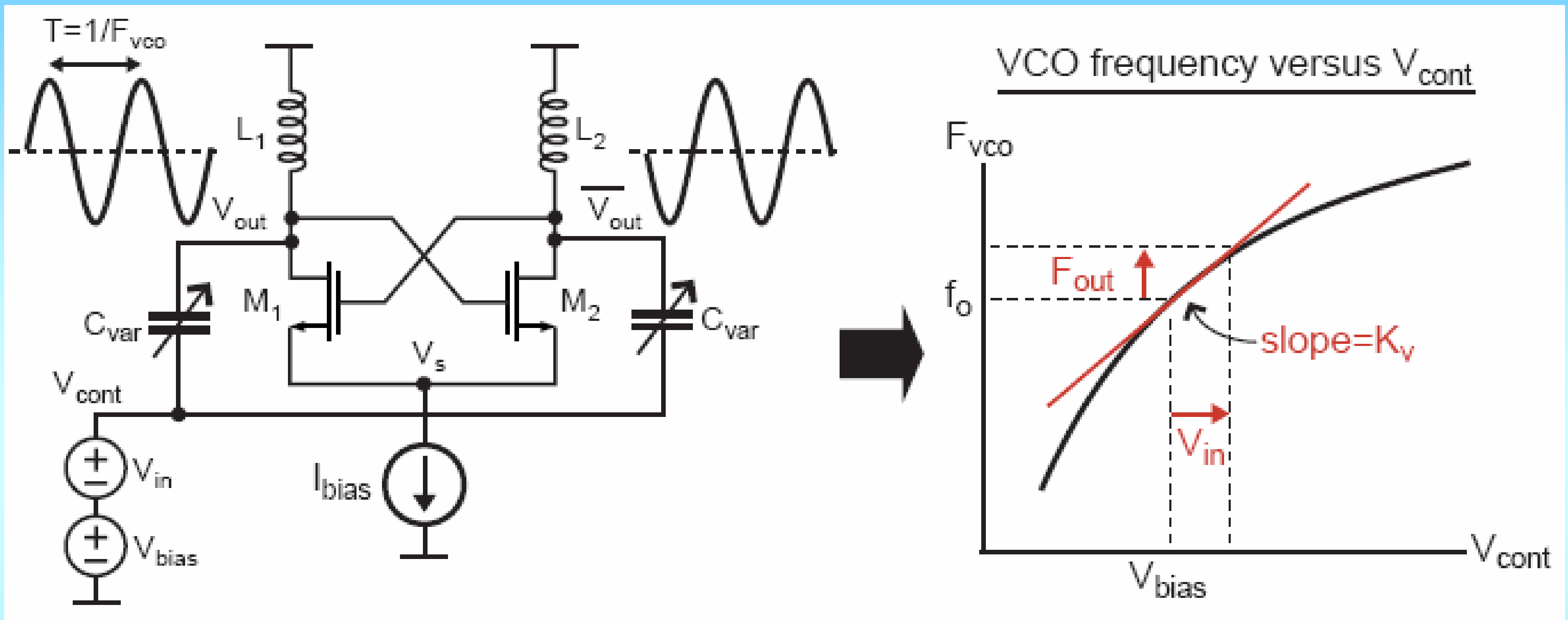
- Simple topology
- Differential implementation (good for feeding differential circuits)
- Good phase noise performance can be achieved

Voltage Controlled Oscillators (LC)



- Variable capacitor (varactor) controls oscillation frequency by adjusting V_{cont}
- Much fixed capacitance cannot be removed
- Fixed cap lowers frequency tuning range

Voltage to Frequency Mapping



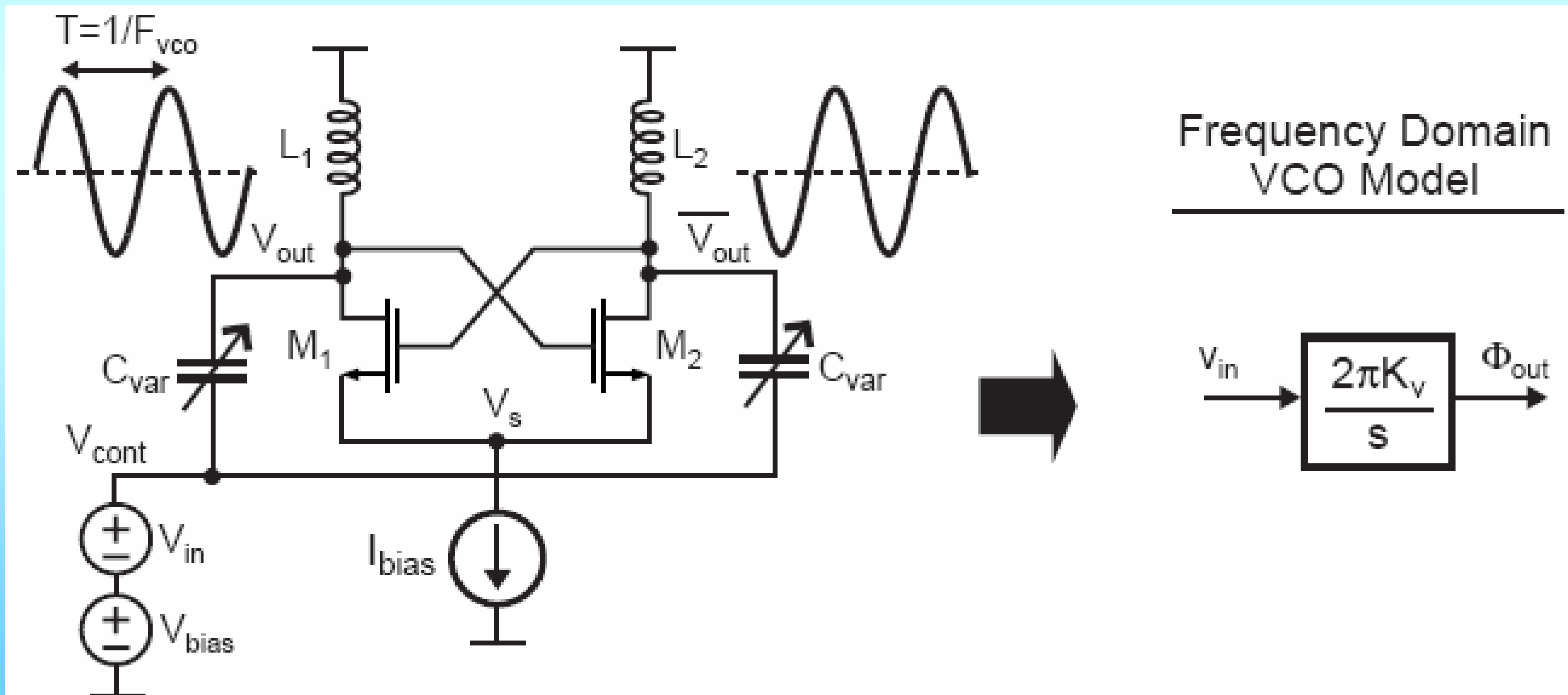
- Model VCO in a small signal manner
- Assume linear relationship in small signal
- Deviations in frequency proportional to control voltage variation

$$\Delta f = K_v v_{in}$$

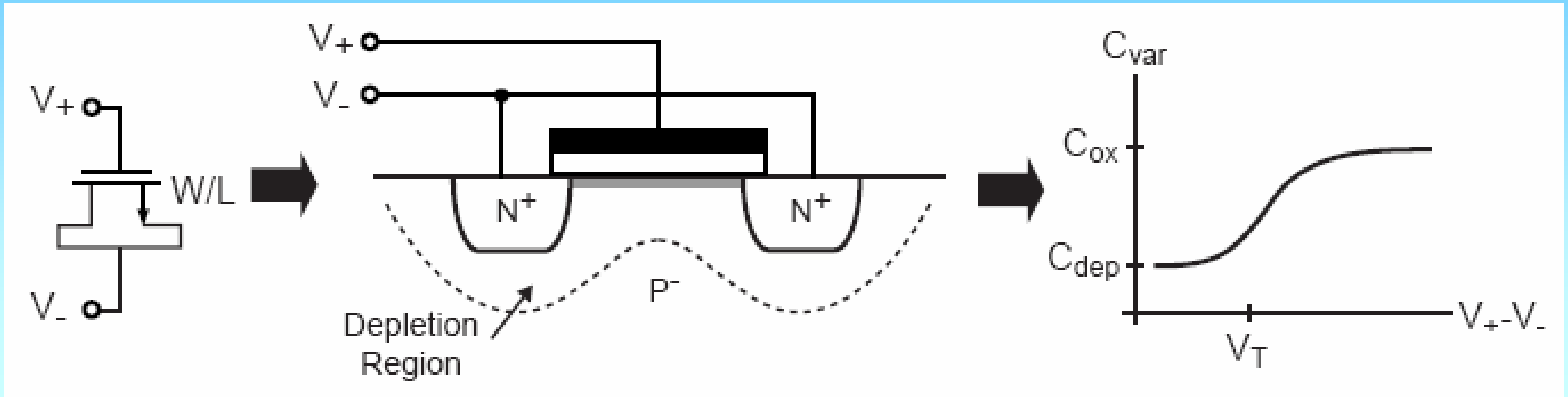
Voltage to phase

- Phase is integration of frequency variation

$$\Phi_{out} = \frac{2pK_v v_{in}}{s}$$

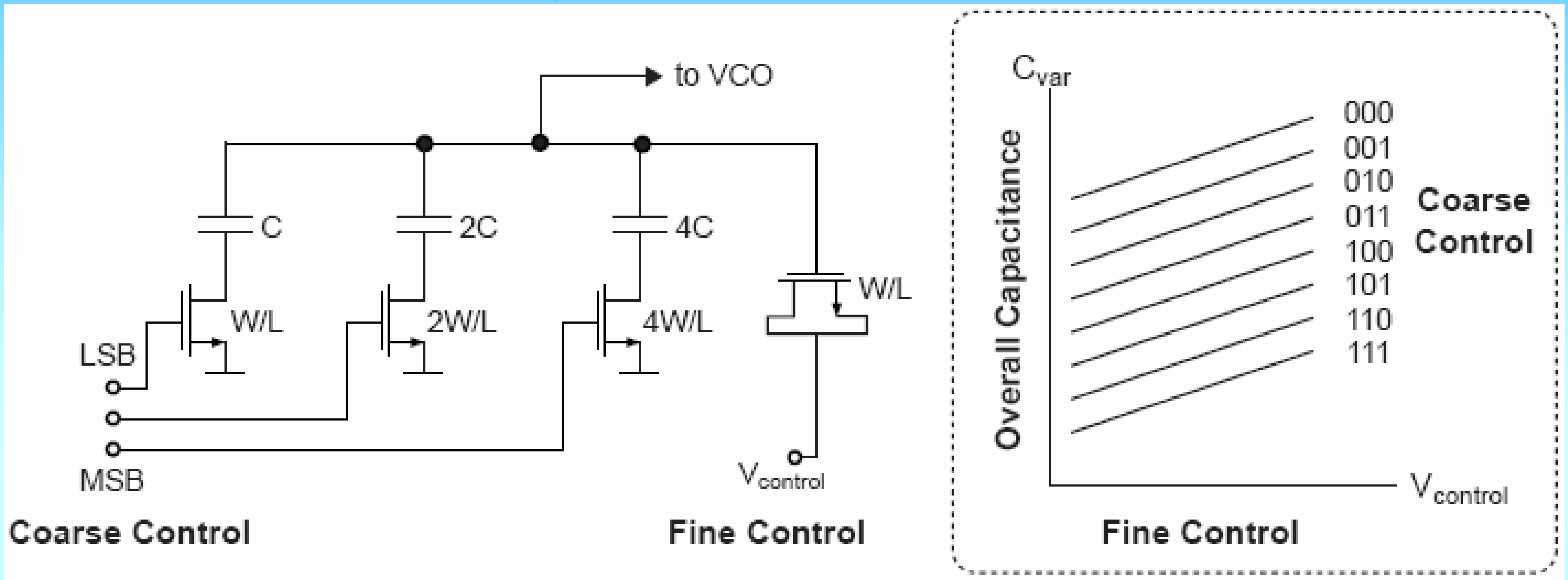


The MOS Varactor



- Consists of a MOS transistor with drain and source connected together
- Abrupt shift in capacitance as inversion channel forms
- Advantage
  - Easily integrated in CMOS
- Disadvantage
  - Q is relatively low in the transition region
  - Note that large signal is applied to varactor
  - Transition region will be swept across each VCO cycle

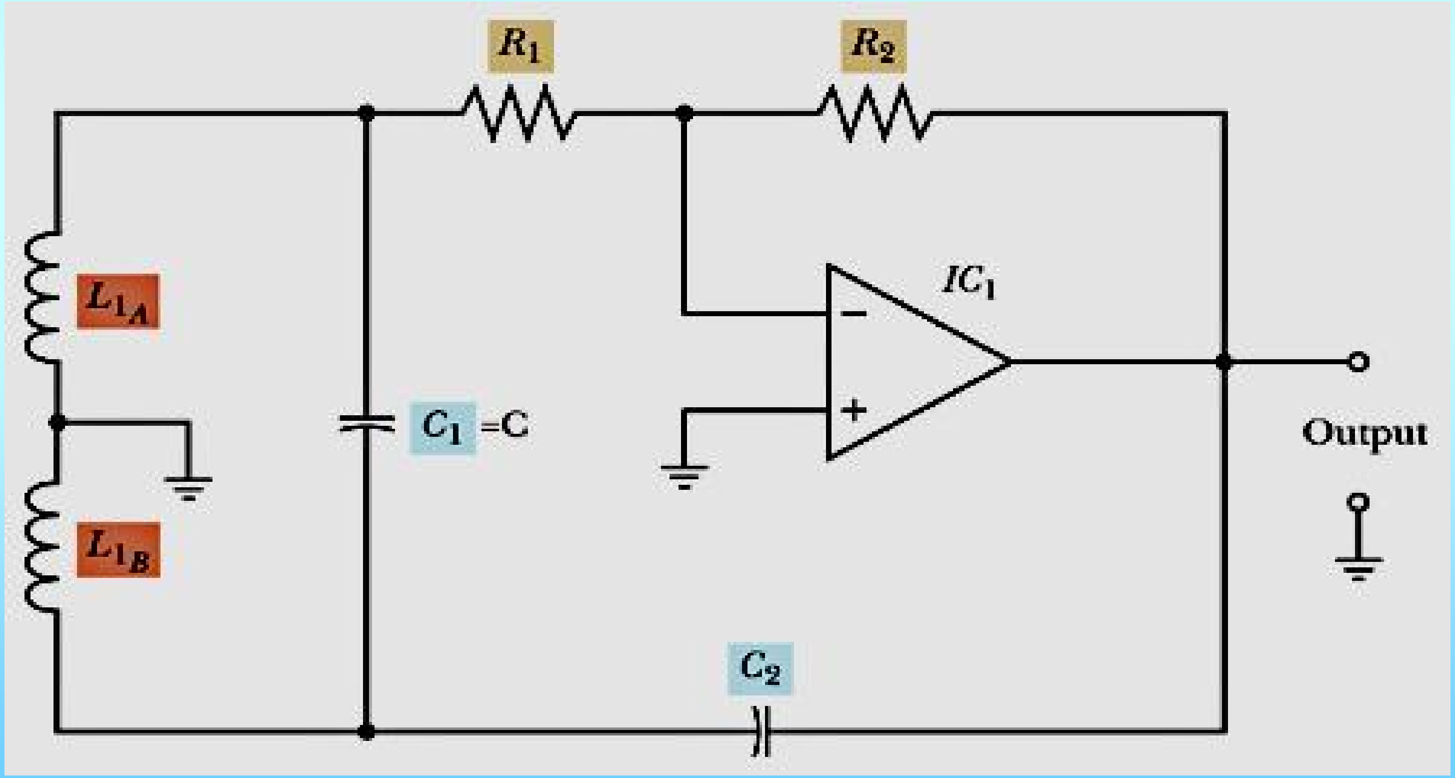
Increasing Q of MOS Varactor



- High Q metal caps are switched in to provide coarse tuning
- Low Q MOS varactor used to obtain fine tuning
- See Hegazi et. al., “A Filtering Technique to Lower LC Oscillator Phase Noise”, JSSC, Dec 2001, pp 1921-1930

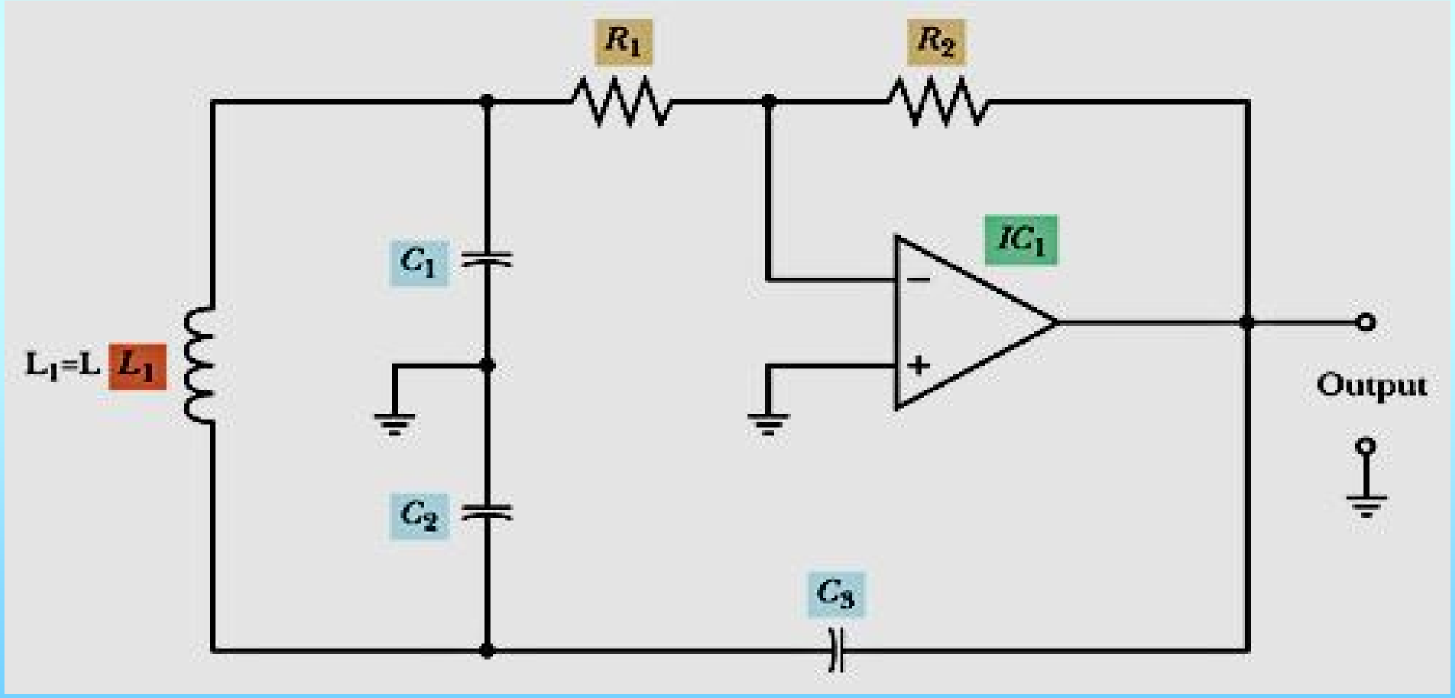
Hartley Oscillator

Uses a tapped inductor
Not popular for IC implementations

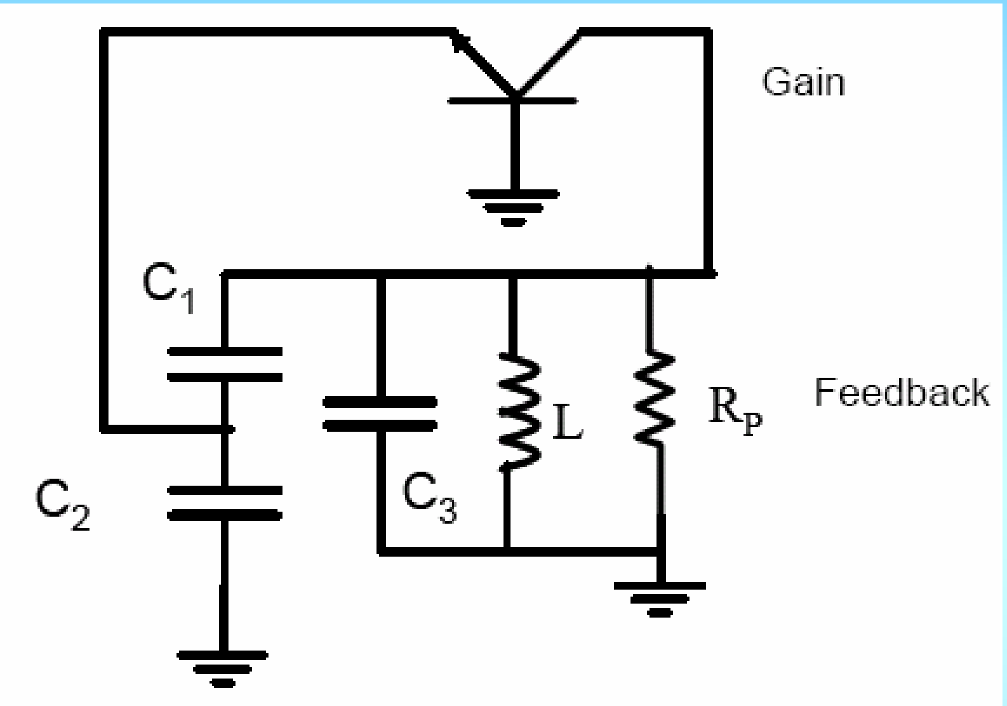


COLPITTS

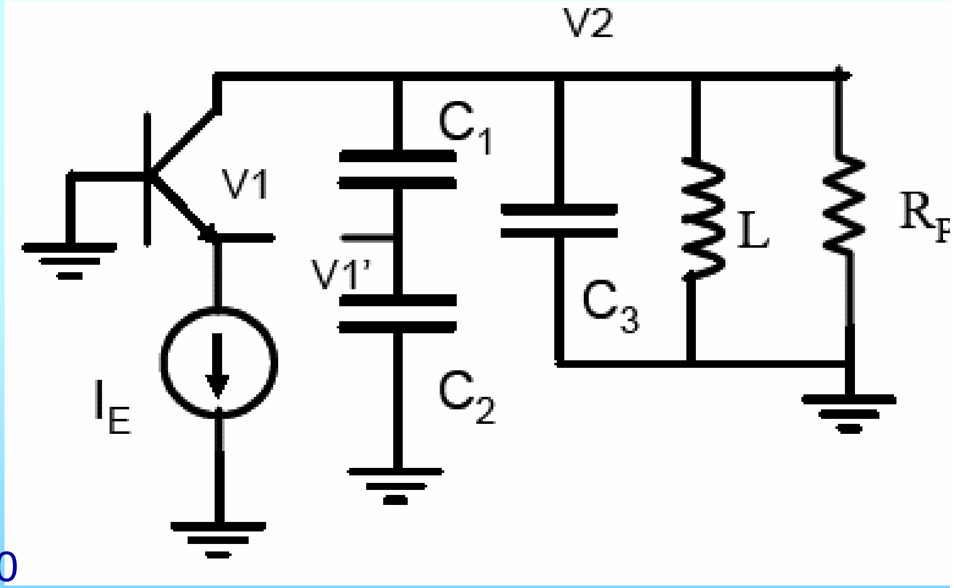
- Similar to Hartley oscillator
- Tapped ground in capacitor circuit



Colpitts Oscillator

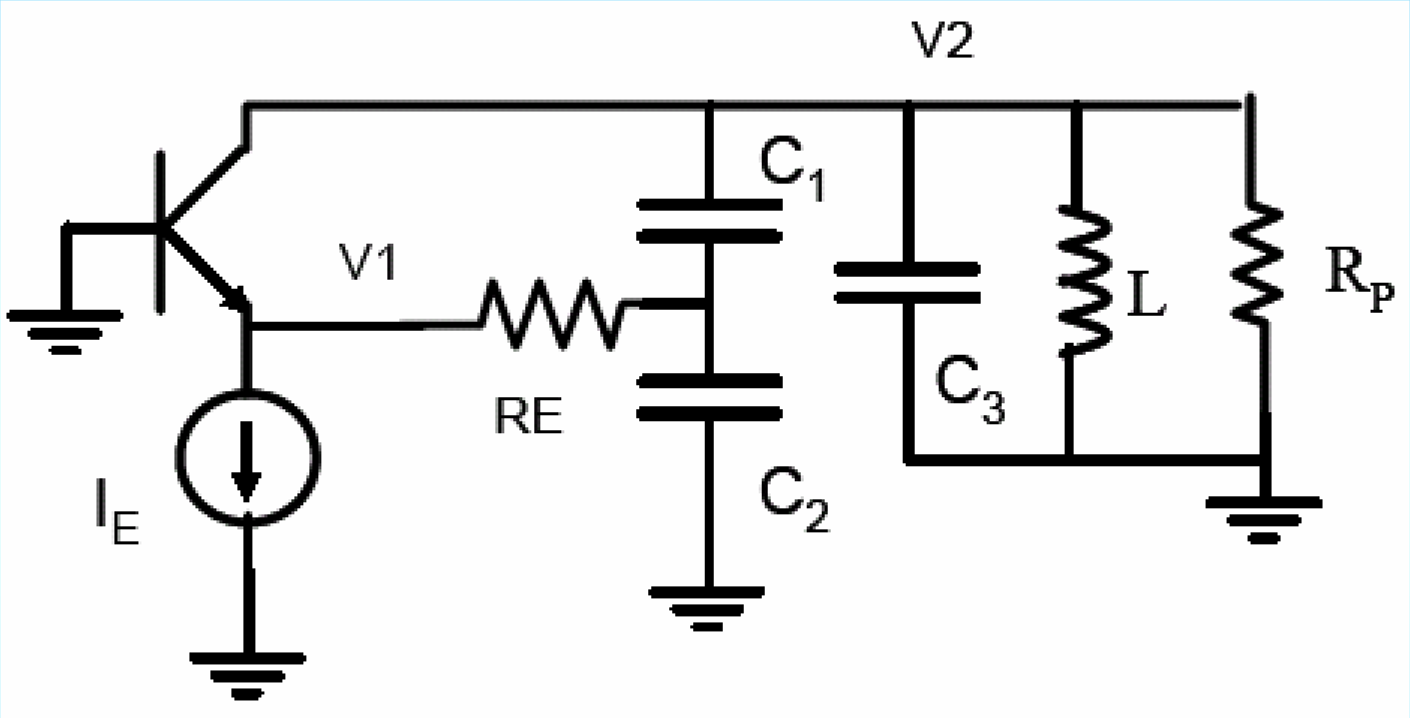


Open-loop for analysis



A= V2/v1 = $g_m R_p$ at ω_0
β=v1'/v2 = C1/(C1+C2)

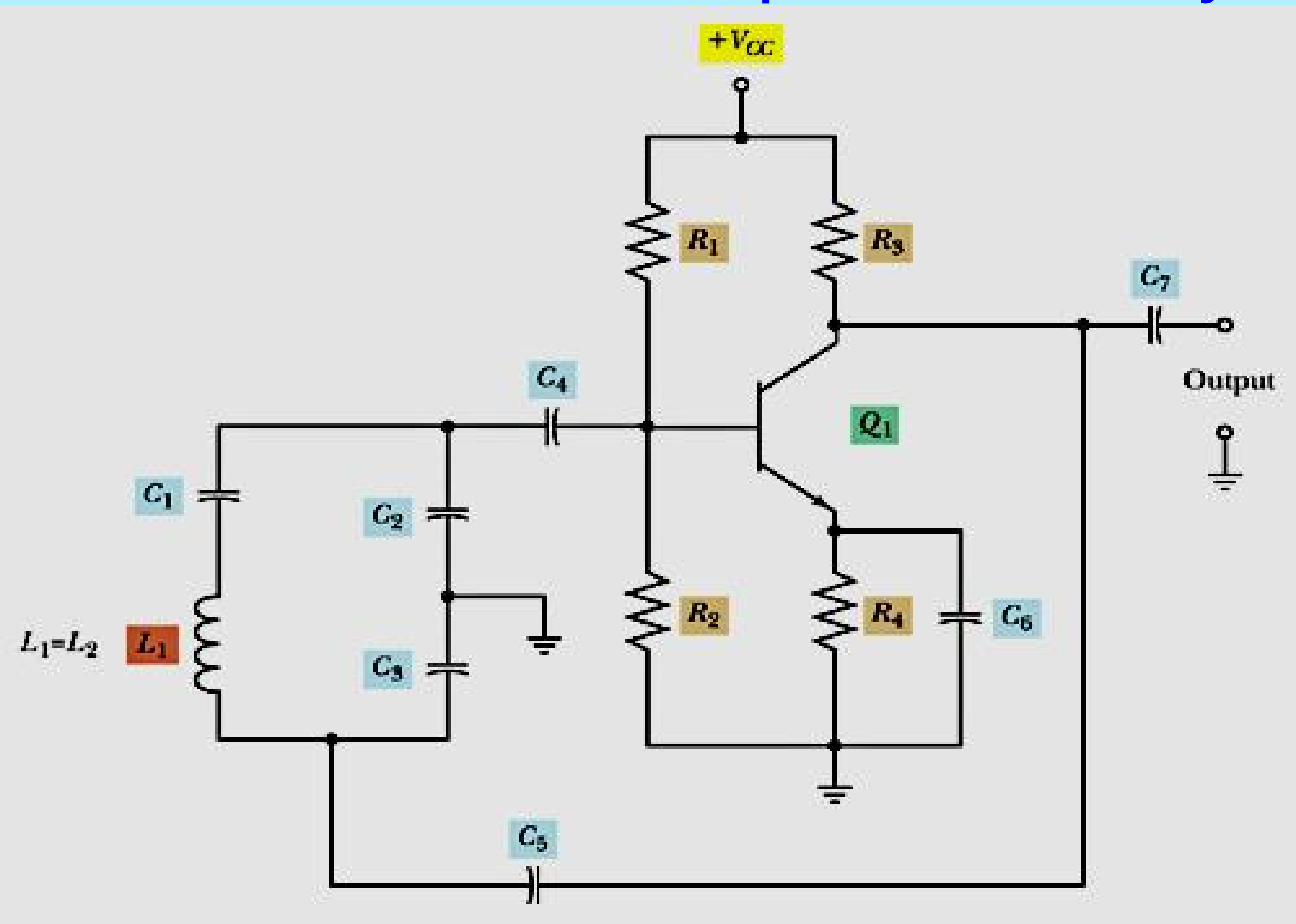
Colpitts with gain and phase control



R_E can help reduce the phase shift by making r_e + $R_E >> \omega C2$. This will also reduce the loop gain.

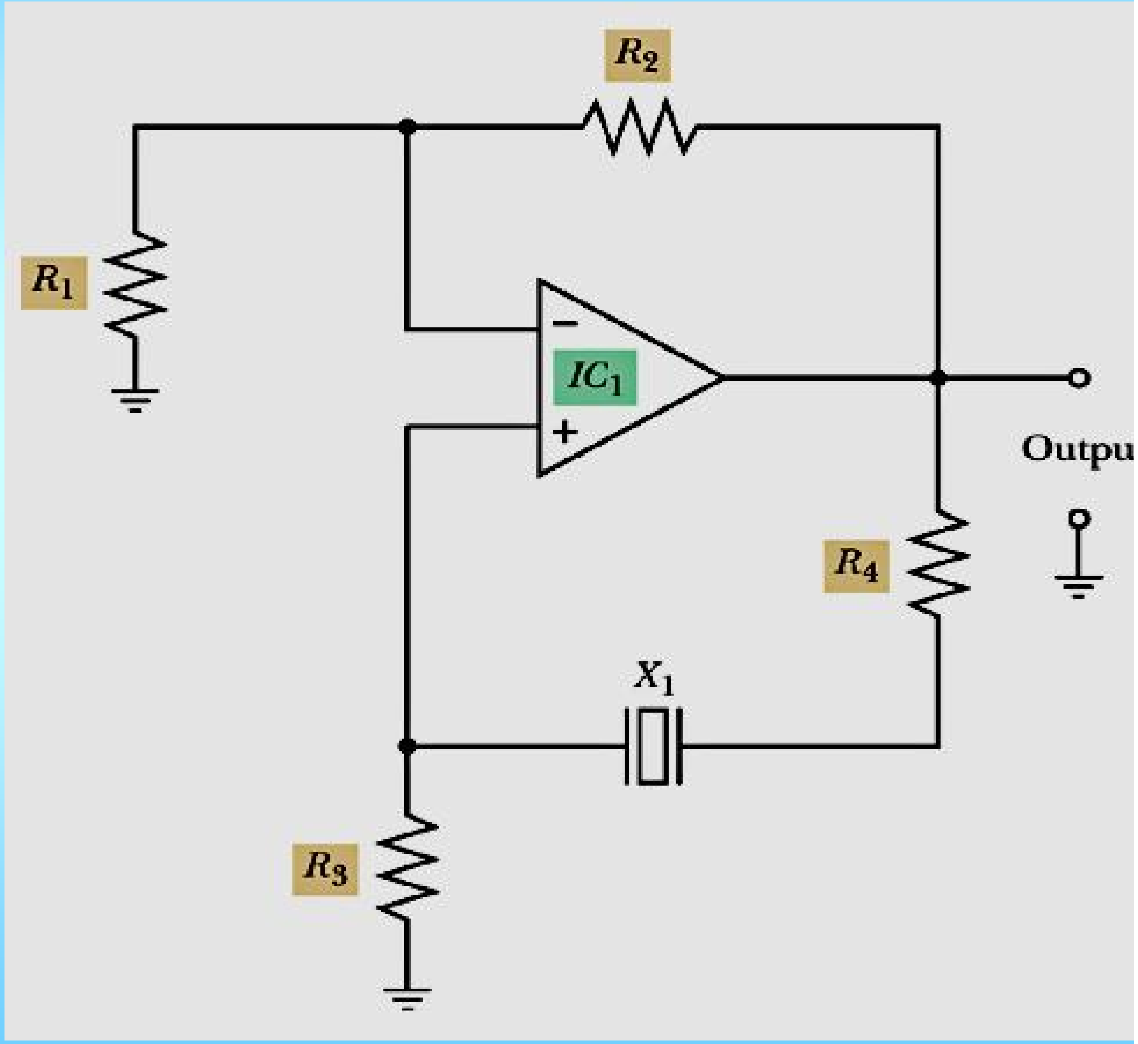
CLAPP OSCILLATOR

- Modified Colpitts oscillator
- Modification done to improve stability



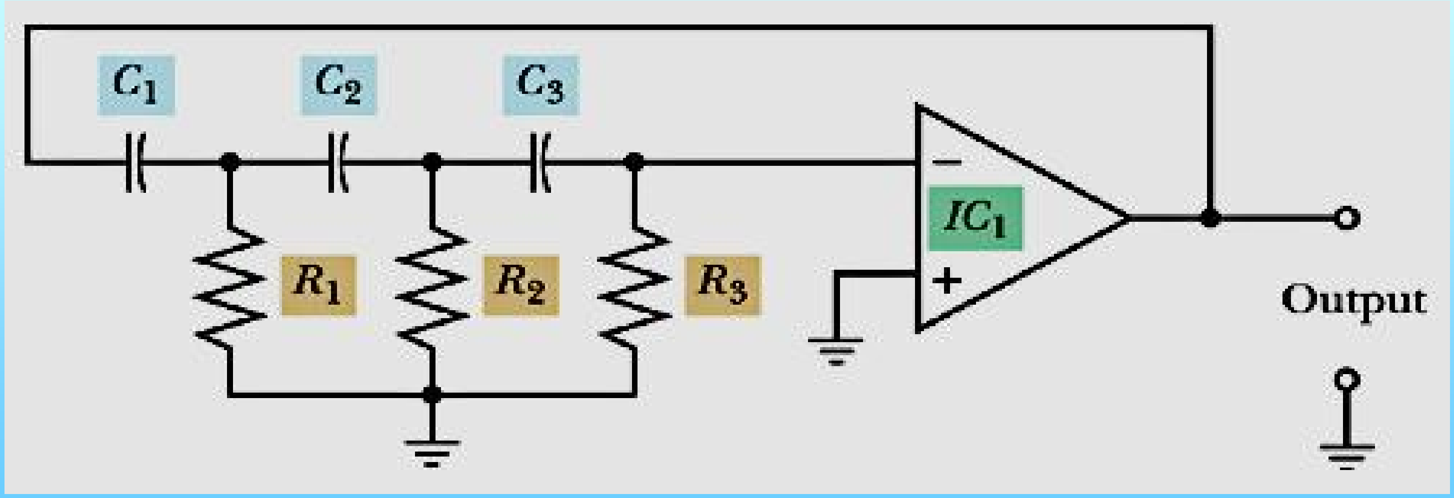
CRYSTAL OSCILLATOR

- Uses crystal for frequency-determining component (parallel)
- Uses crystal in feedback path to frequency determining components (series)
- Very stable circuit

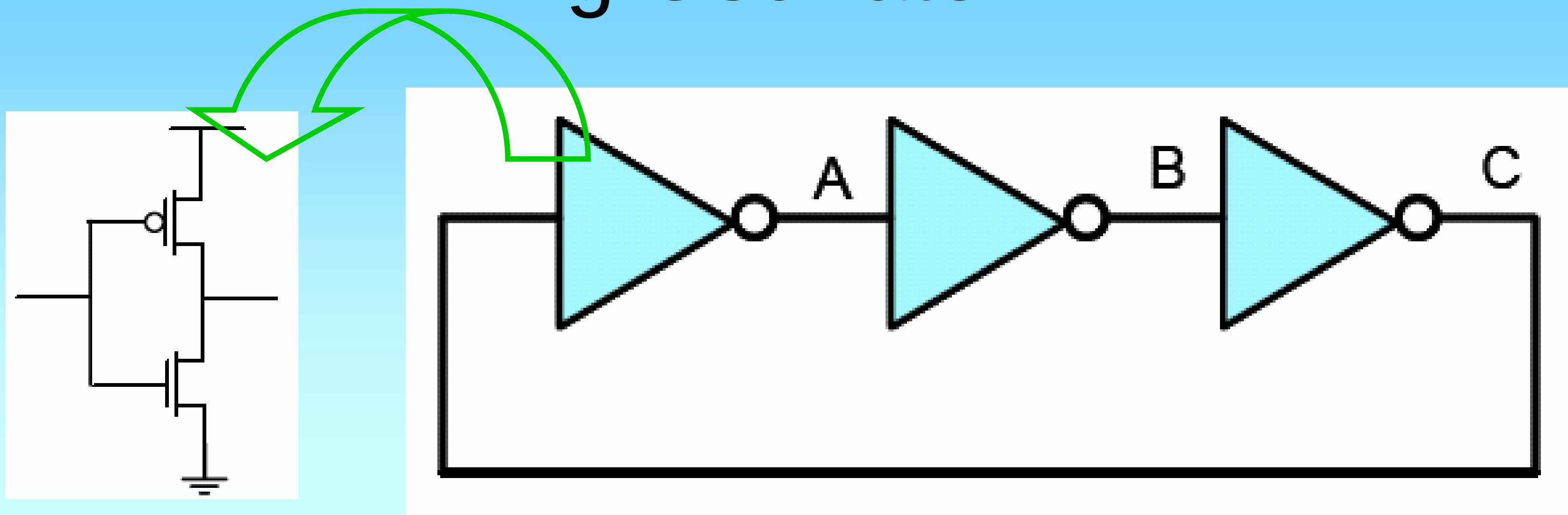


RC OSCILLATOR

- Generates a sine wave
- Uses phase shift of *RC* network for required circuit phase shift
- Uses three *RC* segments
- Low stability $f_r = 1/2\pi RC\sqrt{6}$



Ring Oscillator

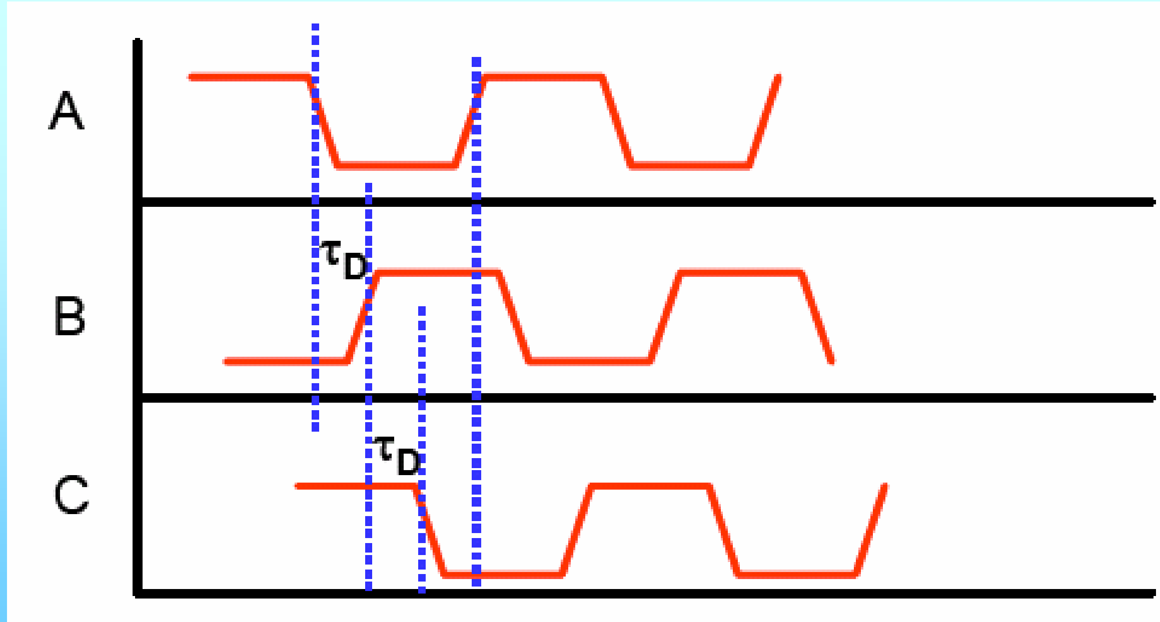


Single ended

Require odd number of stages

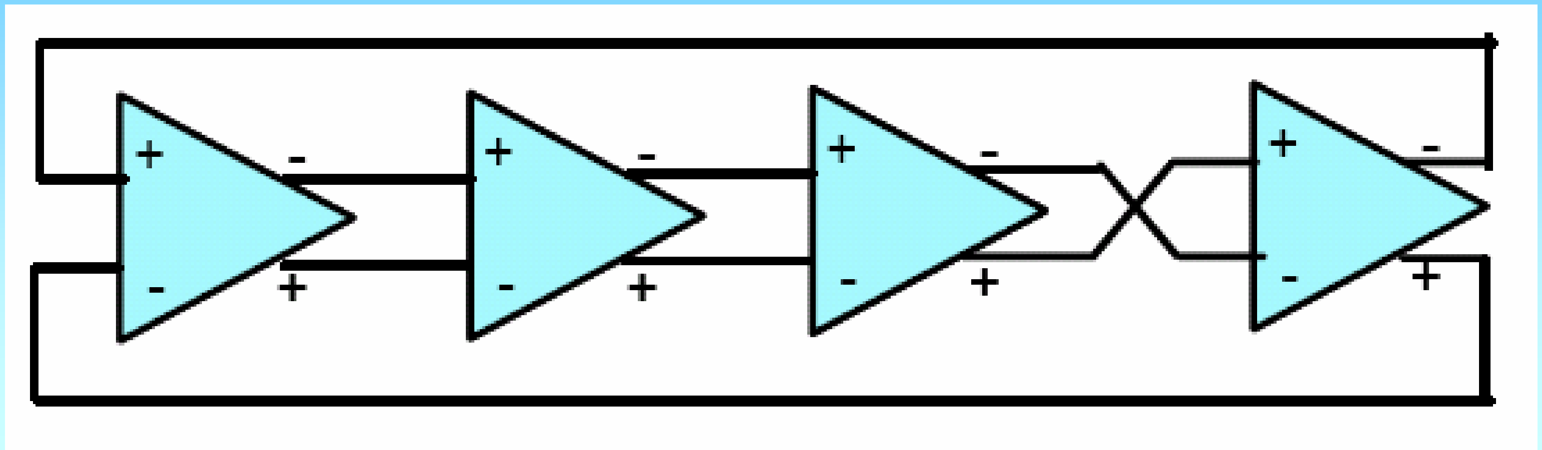
Each stage provides 180/n phase shift

Gain = 1 by saturation



Period of oscillation: $T = 2n\tau_D$ $f = 1/T$

“Twisted Ring” Differential Ring Oscillator



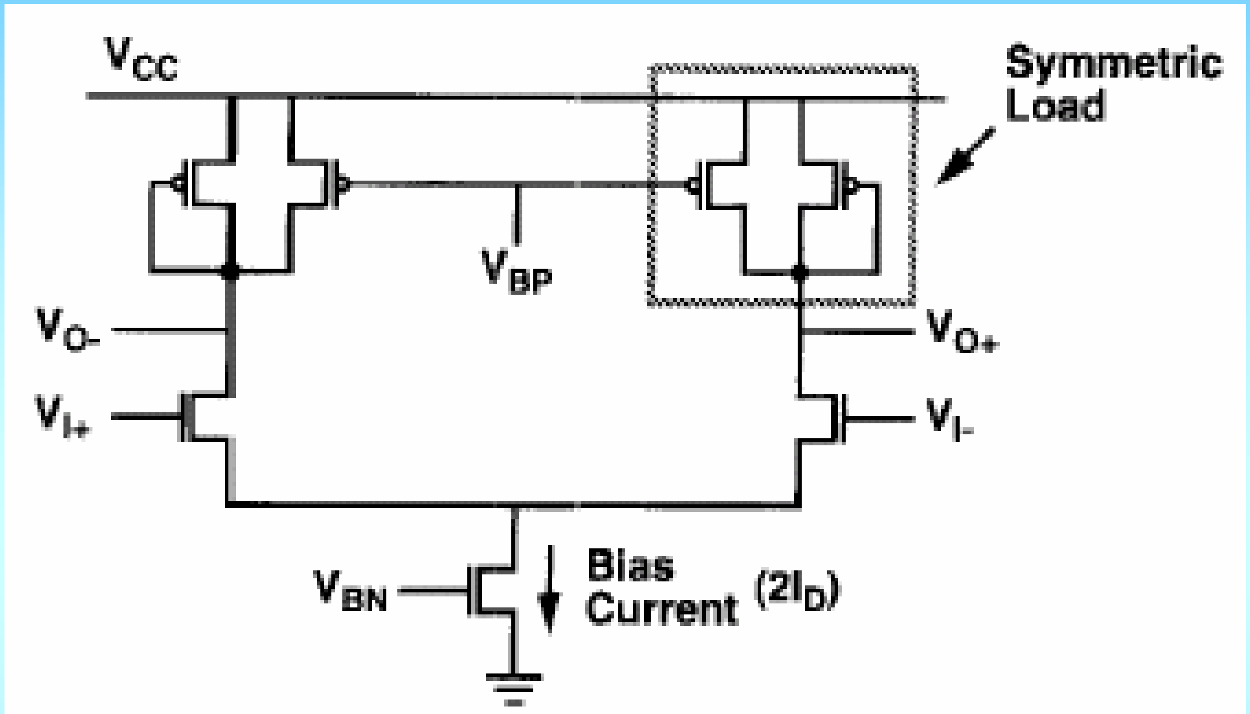
- Common mode rejection of substrate coupled noise
- Easy to control the delay
- Can use an odd or even number of stages
- quadrature or polyphase signals

Popular delay cell: Maneatis delay cell

Maneatis et. al., “Precise Delay Generation Using Coupled Oscillators”, JSSC, Dec 1993 (look at pp 127- 128 for delay cell description)

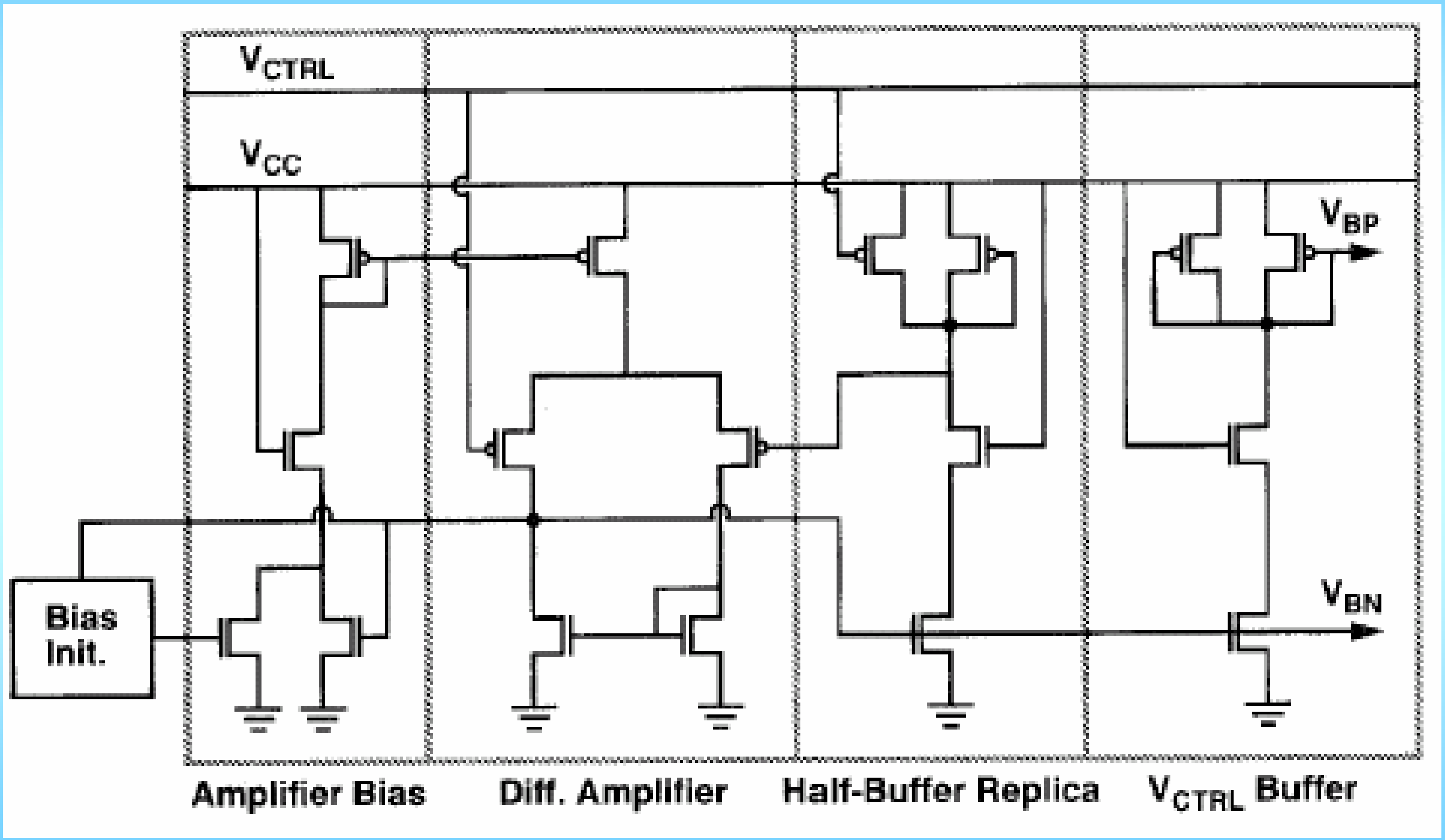
All ring oscillators have large noise as compared to LC oscillators

Maneatis delay cell

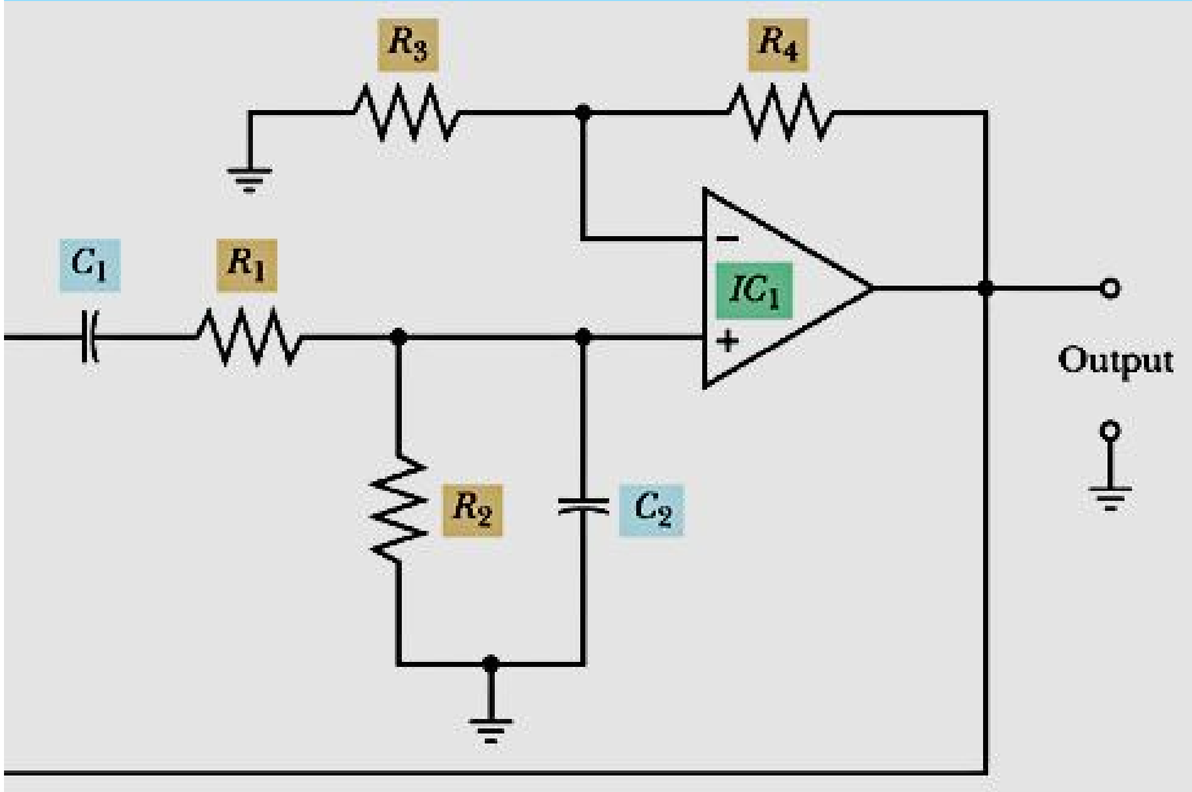


Good power supply rejection
Good substrate noise rejection
Low jitter

Maneatis delay cell bias circuit



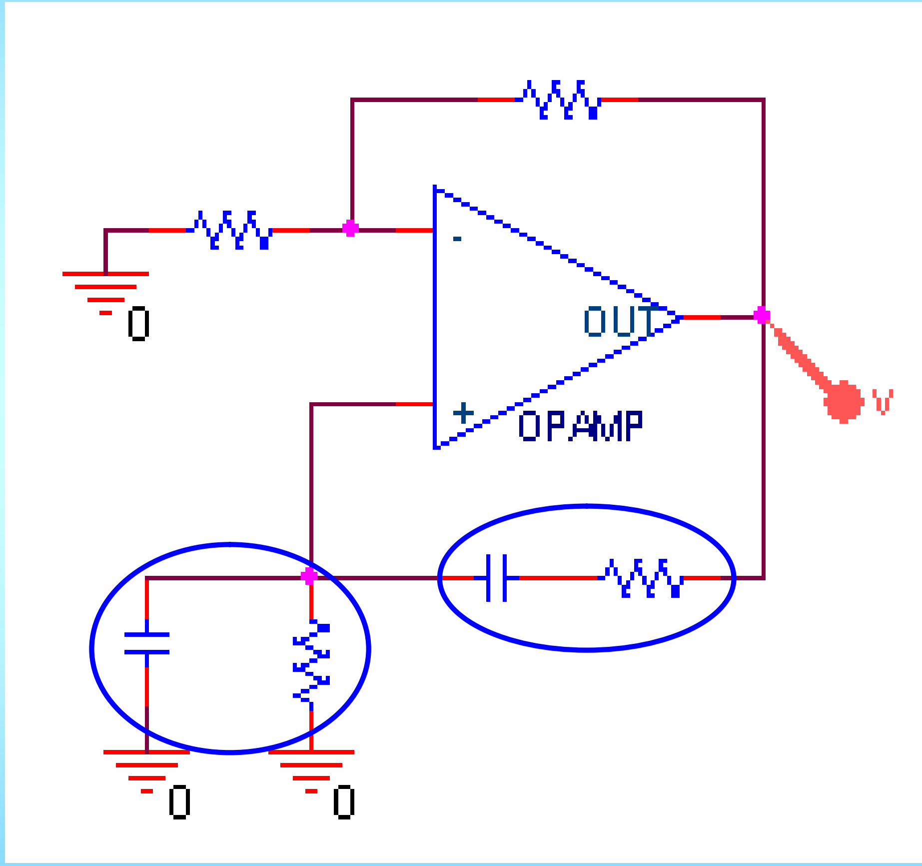
WIEN-BRIDGE



- Uses two RC networks connected to the positive terminal to form a frequency selective feedback network
- Causes Oscillations to Occur
- Amplifies the signal with the two negative feedback resistors

- Simple, Stable, Popular
- Uses resistor and capacitor

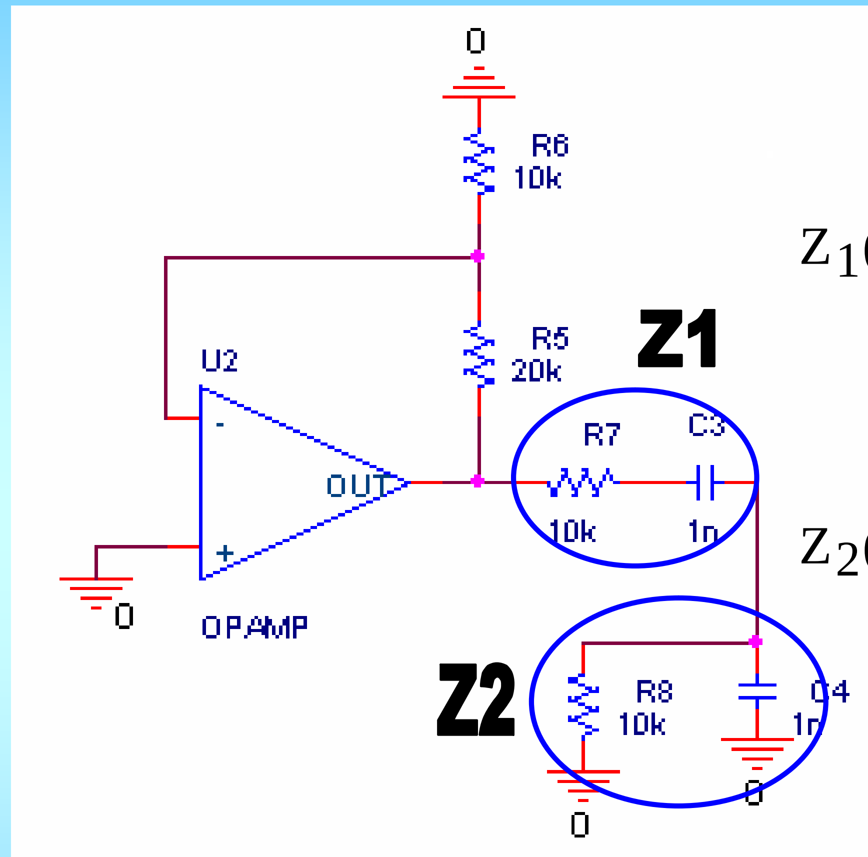
Basics About the Wien-Bridge



Open-loop Analysis

Operational amplifier gain

$$G = \frac{V_1(s)}{V_s(s)} = 1 + \frac{R_2}{R_1}$$



$$Z_1(s) = R + \frac{1}{s \cdot C}$$

$$Z_2(s) = \frac{R \cdot \frac{1}{s \cdot C}}{R + \frac{1}{s \cdot C}}$$

$$V_o(s) = V_1(s) \cdot \frac{Z_2(s)}{Z_1(s) + Z_2(s)}$$

$$V_o(s) = G \cdot V_s(s) \cdot \frac{s \cdot R \cdot C}{s^2 \cdot R^2 \cdot C^2 + 3 \cdot s \cdot R \cdot C + 1}$$

Open-loop Analysis

Simplifying and substituting jw for s

$$T(j\omega) = \frac{j \cdot \omega \cdot R \cdot C \cdot G}{\left(1 - \omega^2 \cdot R^2 \cdot C^2\right) + 3 \cdot j \cdot \omega \cdot R \cdot C}$$

In order to have a phase shift of zero,

$$1 - \omega^2 \cdot R^2 \cdot C^2 = 0$$

This happens at $\omega = 1/RC$ When $\omega = 1/RC$, T(j ω) simplifies to:

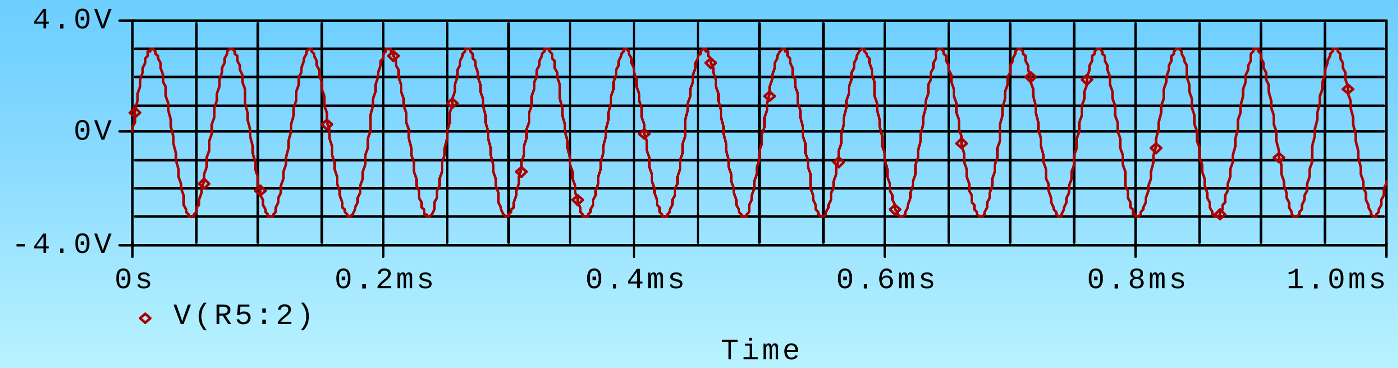
$$T(j\omega) = \frac{G}{3}$$

If G = 3, sustained oscillations

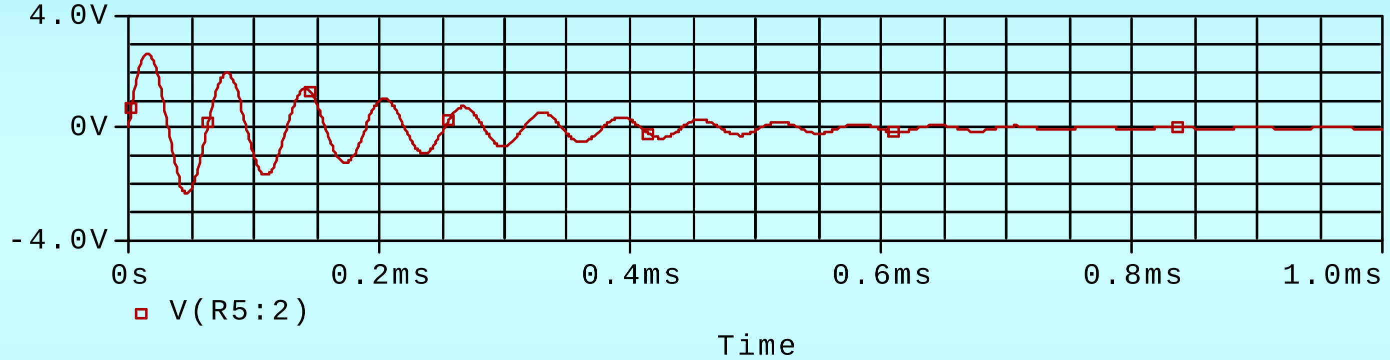
If G < 3, oscillations attenuate

If G > 3, oscillations amplify

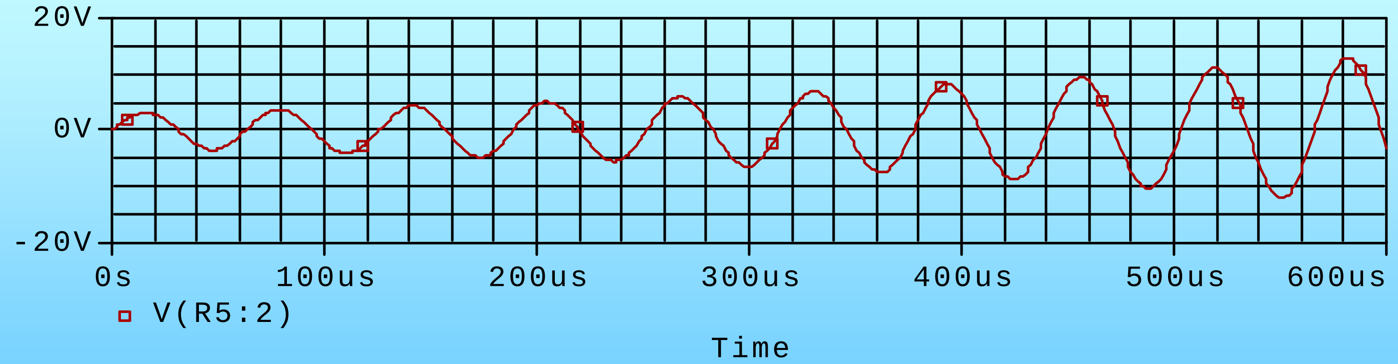
G = 3


4.0V
0V
-4.0V
0s
0.2ms
0.4ms
0.6ms
0.8ms
1.0ms
V(R5:2)
Time

G = 2.9

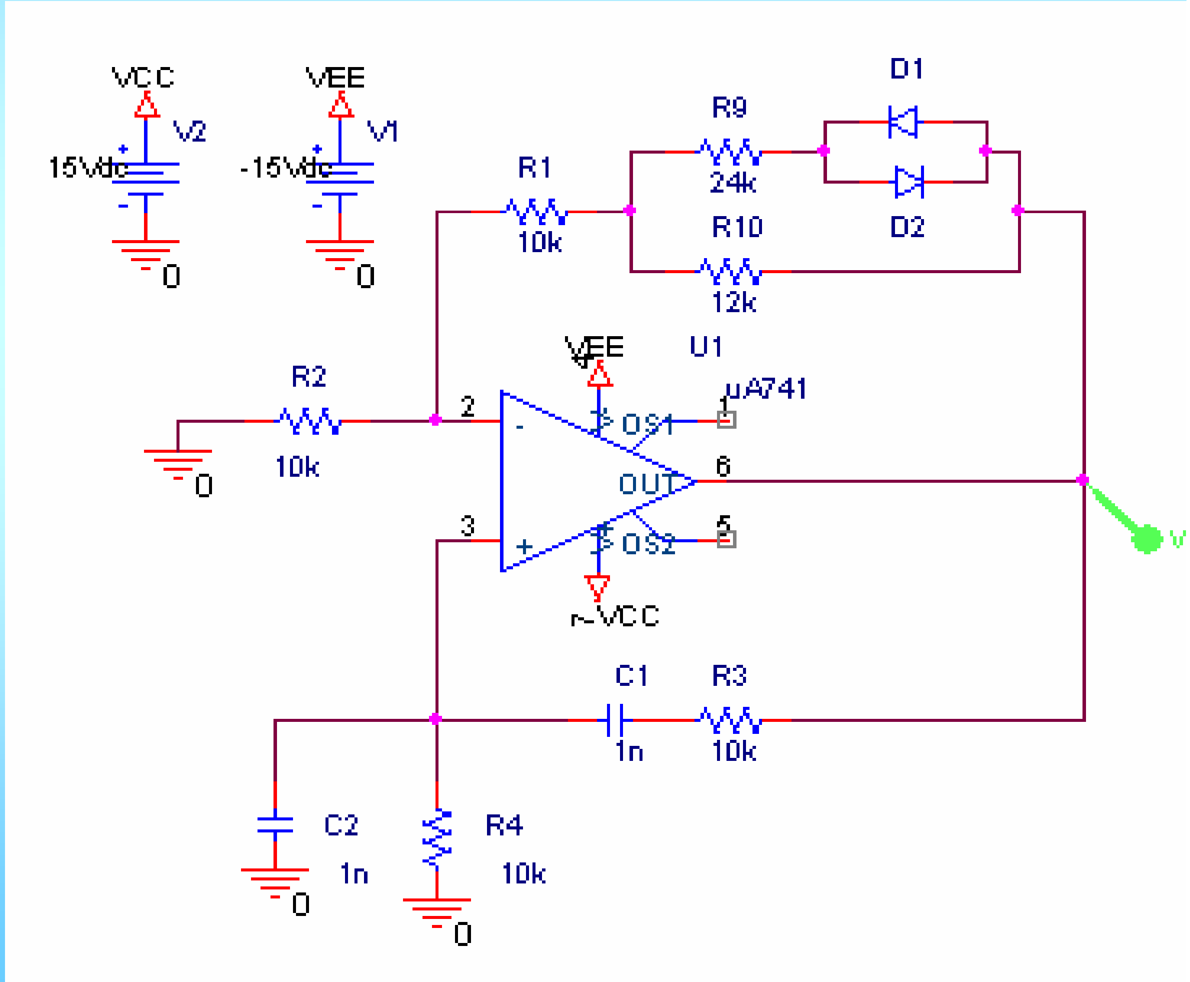

4.0V
0V
-4.0V
0s
0.2ms
0.4ms
0.6ms
0.8ms
1.0ms
V(R5:2)
Time

G = 3.05


20V
0V
-20V
0s
100us
200us
300us
400us
500us
600us
V(R5:2)
Time

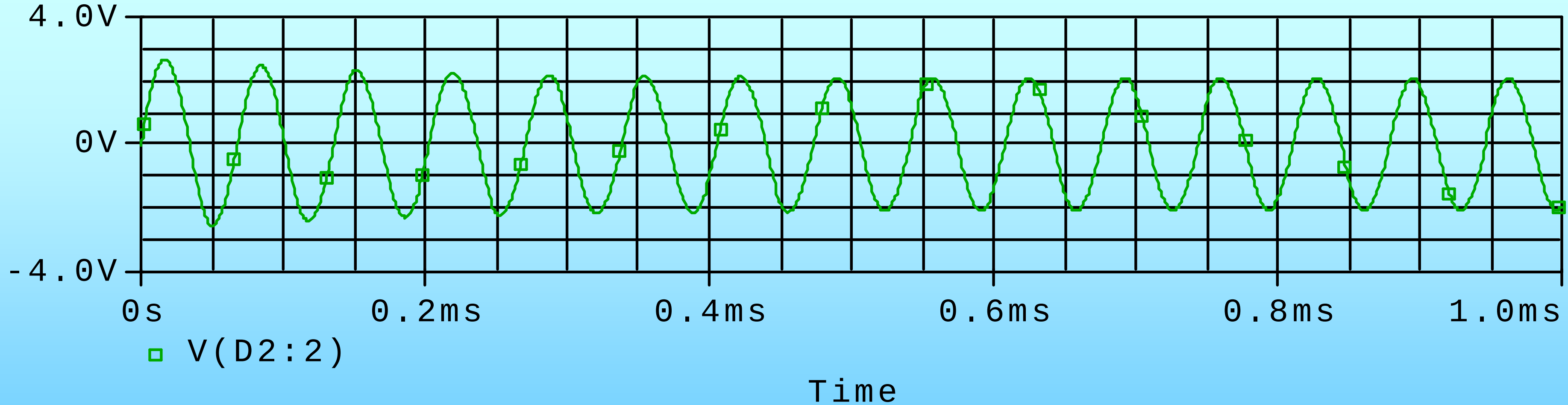
Making the Oscillations Steady

- Add a diode network to keep circuit around G = 3
- If G = 3, diodes are off



Results of Diode Network

- With the use of diodes, the non-ideal op-amp can produce steady oscillations.



Design Issues

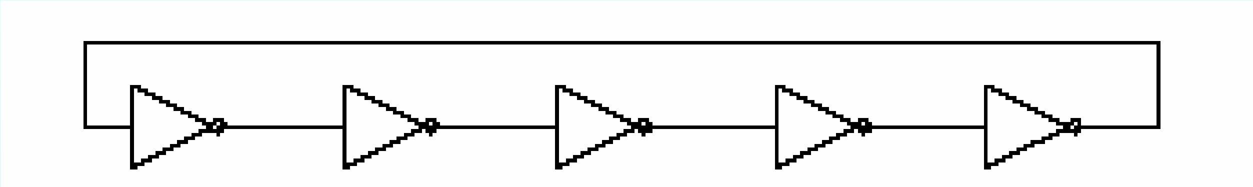
- Wireless applications
  - Tuning Range – need to cover all frequency channels
  - Noise – impacts receiver blocking and sensitivity performance
  - Power – want low power dissipation
  - Isolation – want to minimize noise pathways into VCO
  - Sensitivity to process/temp variations – need to make it manufacturable in high volume
- High speed data link
  - Required noise performance is often less stringent
  - Tuning range is often narrower

Phase Noise and Timing Jitter

- Phase noise and timing jitter
  - Phase noise
    - Measure of spectral density of clock frequency
    - Units: dBc/Hz (decibels below the carrier per Hz)
    - **à** Analog people care about this
  - Timing Jitter
    - Measurement of clock transition edge to reference
    - Units: Seconds (usually pS)
    - **à** More intuitive, useful in digital systems

Phase Noise and Timing Jitter

- Ring oscillators—a general purpose building block in many areas of integrated circuit design
  - Clock and Data Recovery
  - On-Chip Clock Distribution
  - Frequency Synthesis
  - Data Conversion: Pulse Width and Phase Modulation



5-Stage Ring Oscillator

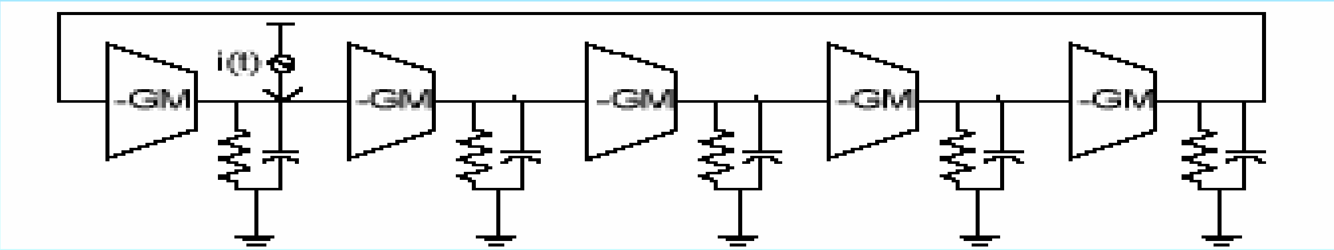
- Timing jitter and phase noise analysis is important

- Real Design Considerations: frequency, power, timing jitter

  à The approach of supply and body bias voltage scaling

Timing Jitter and Phase Noise in Ring Oscillator

- Modified linear model of a five stage ring oscillator



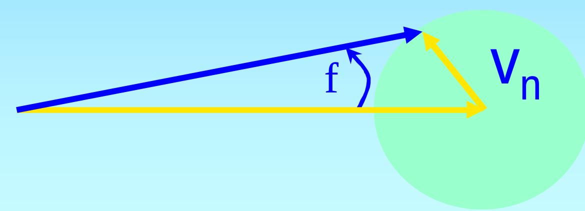
- Two dominant types of noise in a ring oscillator
  - transistor thermal noise
  - power supply noise
- Noise effect modeling: current or charge injected into the load capacitance at each stage

$$Noise \Rightarrow \frac{\Delta q}{Cnode} = \Delta V \Rightarrow \Delta\Phi \Rightarrow Jitter\,!$$

Noise in Oscillators

$$V_{o,\text{ideal}} = A\cos(\omega_o t + \varphi)$$

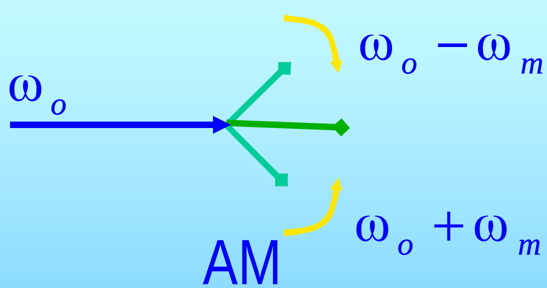
$$V_{o,\text{practical}} = A(t)\cdot \underbrace{f(\omega_o t + \varphi(t))}_{\text{periodic function with period}=2\pi}$$

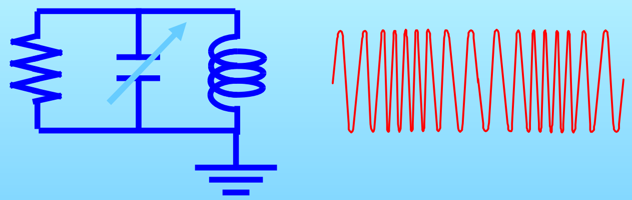


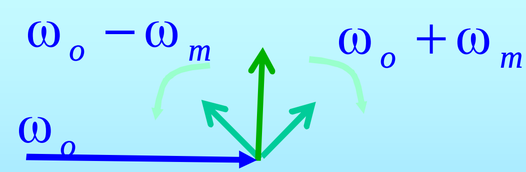
AM

FM

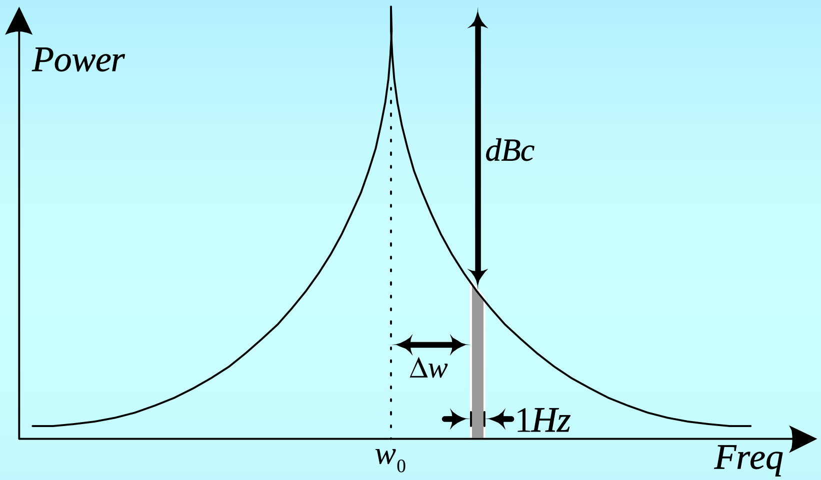
PM

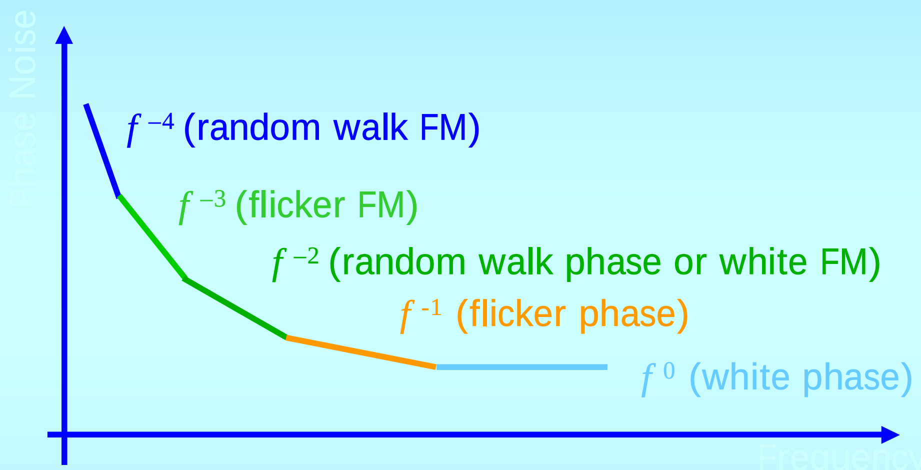






Phase Noise





$$L_{total}\{\Delta\omega\} = 10 \cdot \log\left[\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}}\right]$$

Phase Noise

$$L\{\Delta w\} = 10 \cdot \log\left[\frac{2FkT}{P_s} \cdot \left[1 + \left(\frac{w_0}{2Q_L \Delta w}\right)^2\right] \cdot \left(1 + \frac{w_{1/f^3}}{|\Delta w|}\right)\right]$$

– Phase noise is inversely proportional to power dissipation

– The higher the Q of the tank, the lower the phase noise