3.13 SUMMARY

This chapter has presented only a few of the many DC tests and techniques that the mixed-signal test engineer will encounter. Several chapters or perhaps even a whole book could be devoted to highly accurate DC test techniques. However, this book is intended to address mixed-signal testing. Hopefully, the limited examples given in this chapter will serve as a solid foundation from which the test engineer can build a more diversified DC measurement skill set.

DC measurements are trivial to define and understand, but they can sometimes be excruciatingly difficult to implement. A DC offset of 100 mV is very easy to measure if the required accuracy is ±10 mV. On the other hand, if 1-μV accuracy is required, the test engineer may find this to be one of the more daunting test challenges in the entire project. The accuracy and repeatability requirements of seemingly simple tests like DC offset can present a far more challenging test problem than much more complicated AC tests.

Accuracy and repeatability of measurements is the subject of Chapter 5, following an introductory chapter on data analysis and probability in Chapter 4. This topic pertains to a wide variety of analog and mixed-signal tests. Much of a test engineer's time is consumed by accuracy and repeatability problems. These problems can be one of the most aggravating aspects of mixed-signal testing. The successful resolution of a perplexing accuracy problem can also be one of the most satisfying parts of the test engineer's day.

PROBLEMS

3.1. The output of a 10-V voltage regulator varies from 9.95 V under no-load condition to 9.34 V under a 10-mA maximum rated load current. What is its load regulation?

3.2. The output of a 5-V voltage regulator varies from 4.86 to 4.32 V when the input voltage is changed from 14 to 6 V under a maximum load condition of 10 mA. What is its line regulation?

3.3. A 9-V voltage regulator is rated to have a load regulation of 0.150 V for a maximum load current of 15 mA. Assuming a no-load output voltage of 8.9 V, what is the expected output voltage at the maximum load current?

3.4. A 6-V voltage regulator is rated to have a load regulation of 2% for a maximum load current of 20 mA. Assuming a no-load output voltage of 5.9 V, what is the worst-case output voltage at the maximum load current?

3.5. A voltage of 1.2 V is dropped across an input pin when a 100-μA current is forced into the pin. Subsequently, a 1.254-V level occurs when the current is increased to 200 μA. What is the input resistance?

3.6. The input pin of a device is characterized by the $i - v$ relationship: $i = 0.001\ v + 100$. What is the resistance seen looking into this pin?

3.7. Voltages of 1.2 and 3.3 V appear at the output of an amplfier when currents of –10 and +10 mA, respectively, are forced into its output. What is the output resistance?

3.8. The no-load output voltage of an amplifier is 4 V. When a 600-Ω load is attached to the output, the voltage drops to 3 V. What is the amplifier's output resistance?

3.9. For a ×10 amplifier characterized by $V_{OUT} = 10V_{IN} - V_{IN}^2 + 5$ over a ±5-V range, what are its input and output offset voltages?

3.10. A voltmeter introduces a measurement error of –5% while measuring a 1-V offset from an amplifier. What is the actual reading captured by the voltmeter?

3.11. A voltmeter with an input impedance of 500 kΩ is used to measure the DC output of an amplifier with an output impedance of 500 kΩ. What is the expected relative error made by this measurement?

3.12. A differential amplifier has outputs of 2.4 V (OUTP) and 2.7 V (OUTN) with its input set to a V_{MID} reference level of 2.5 V. What are the single-ended and differential offsets? The common-mode offset? (All offsets are to be measured with respect to V_{MID}.)

3.13. A perfectly linear amplifier has a measured gain of 9.8 V/V and an output offset of 1.2 V. What is the input offset voltage?

3.14. Voltages of 1.3 V and 10.3 V appear at the output of a single-ended amplifier when inputs of 110 mV and 1.3 V are applied, respectively. What is the gain of the amplifier in V/V? What is the gain in decibels?

3.15. An amplifier is characterized by $V_{OUT} = 3.5V_{IN} + 1$ over the input voltage range 0 to 5 V. What is the amplifier output for a 2-V input? Similarly for a 3-V input? What is the corresponding gain of this amplifier in V/V to a the 1-V swing centered around 2.5-V? What is the gain in decibels?

3.16. An amplifier is characterized by $V_{OUT} = 1.5V_{IN} + 0.35V_{IN}^2 + 1$ over the input voltage range 0 to 5 V. What is the amplifier output for a 1-V input? Similarly for a 3-V input? What is the corresponding gain of this amplifier in V/V to a signal with a 1-V swing centered at 1-V? What is the gain in decibels?

3.17. For the nulling amplifier setup shown in Figure 3.19 with R_1 = 100 Ω, R_2 = 200 kΩ, and R_3 = 50 kΩ, an SRC1 input swing of 1 V results in a 130-mV swing at the output of the nulling amplifier. What is the open-loop gain of the DUT amplifier in V/V? What is the gain in decibels?

3.18. For the nulling amplifier setup shown in Figure 3.19 with R_1 = 200 Ω, R_2 = 100 kΩ, and R_3 = 100 kΩ, and a V_{MID} of 2.5 V, an offset of 3.175 V (relative to ground) appears at the output of the nulling op amp when the input is set to V_{MID}. What is the input offset of the DUT amplifier?

3.19. For the nulling amplifier setup shown in Figure 3.19 with R_1 = 100 Ω, R_2 = 300 kΩ, and R_3 = 100 kΩ, and the DUT op amp having an open-loop gain of 1000 V/V, what is the output swing of the nulling amplifier when the input swings by 1 V?

3.20. The input of a ×10 amplifier is connected to a voltage source forcing 1.75 V. The power supply is set to 4.9 V and a voltage of 1.700 V is measured at the output of the amplifier. The power supply voltage is then changed to 5.1 V and the output measurement changes to 1.708 V. What is the PSS? What is the PSRR if the measured gain is 9.8 V/V?

3.21. For nulling amplifier CMRR setup shown in Figure 3.22 with R_1 = 100 Ω, R_2 = 300 kΩ, and R_3 = 100 k Ω, SRC1 is set to +3.5 V and a differential voltage of 130 mV is measured between SRC1 and the output of the nulling amplifier. Then SRC1 is set to 1.0 V and the measured voltage changes to –260 mV. What is the CMRR of the op amp in decibels?

3.22. An amplifier has an expected CMRR of –85 dB. For a 1-V change in the input common-mode level, what is the expected change in the input offset voltage of this amplifier?

3.23. A comparator has an input offset voltage of 6 mV and its negative terminal is connected to a 2.5-V level, at what voltage on the positive terminal does the comparator change state?

3.24. A slicer circuit is connected to a 2-V reference and has a threshold voltage error of 20 mV. At what voltage level will the slicer change state?

3.25. If a slicer's 2.5-V reference has an error of +100 mV and the comparator has an input offset of –10 mV, what threshold voltage should we expect?

3.26. A comparator has a measured hysteresis of 10 mV and switches state on a rising input at 2.5 V. At what voltage does the comparator change to a low state on a falling input?

3.27. For an amplifier characterized by $V_{OUT} = 6V_{IN} + 0.5V_{IN}^2 - 2$ over a ±1-V input voltage range, determine the input offset voltage using a linear search process, starting with two points at ±1 V. After how many iterations did the answer change by less than 1 mV? How many iterations would have been required using a binary search from –1 to +1 V?

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