Test Time Reduction with SATOM:
Simultaneous AC-DC Test with Orthogonal Multi-excitations

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Abstract

Test time controls the competitiveness and viability of new precision products in two fundamental ways: it determines final test cost which is a major part of the recurring manufacturing cost, and it determines characterization test time which directly adds to time to market. This paper introduces a new test strategy aimed at dramatically reducing test time for precision analog and mixed signal products. The strategy is termed SATOM for Simultaneous AC-DC Test with Orthogonal Multi-excitations. In SATOM, a device under test is excited with multiple mutually-orthogonal stimulus signals that are simultaneously applied at different input points of the device. A single set of response data is acquired and an intelligent processing algorithm is used to simultaneously compute multiple AC and DC test specifications for the device. This results in a reduction of well over 90% in test time for those specs, with no negative impact on test coverage and test accuracy. Extensive measurement results demonstrated effectiveness, efficiency and robustness of the new method.

1. Introduction

As process technology continues its consistent and rapid progress, die cost has been dropping exponentially and has gone down by many orders of magnitude. New packaging technologies have also brought significant reduction in package cost. In contrast, test cost has proven to be tenacious. Despite decades of great efforts from both industry and academia, progress in test technology for analog and mixed-signal integrated circuits has been relatively slow. Essentially all parametric specifications are still tested one by one according to their definitions as initially introduced [1]. Consequently, test cost as a percentage of overall manufacturing cost is becoming unacceptable. The 2011 International Technology Roadmap for Semiconductors (ITRS) [2] has placed Cost of Test and Overall Equipment Efficiency at the top of its priority list of difficult challenges among grand challenges in the Test and Test Equipment area. It further states: “Test cost is an ever increasing concern for the test community. While there have been many efforts to confront the rise in test cost, the reality is that increasing complexity is driving increased cost of test.” Based on the current state and projected challenges, the ITRS states that “the industry is reaching a strategic inflection point for the semiconductor business.” Major semiconductor companies are making test cost reduction a major corporate priority.

For over three decades, code density test and spectral analysis [3, 4] have been the most widely used techniques for mixed signal test. Both test accuracy and test speed were important considerations for practical implementations [5, 6]. Built-in self-test is seen as an eventual solution to reducing production test requirement [7-10]. Various improvements to the histogram test and sine wave test methods have been proposed for decades [11, 12]. Various alternative test methods have also been proposed, including linear regression model based tests [13, 14], low frequency nonlinearity estimation [15, 16], reduced code testing [17], and so on. Due to reduced accuracy or reduced test coverage, the application of these alternative tests is limited. In [18, 19], the authors *attempted to combine large signal spectral testing and small signal ramp test to achieve overall linearity test results with reduced test time*. In [20-22], the authors introduced new histogram based linearity test algorithms which dramatically relaxed the linearity requirement for stimulus generation so that 7 or 8 bit linear ramp signals could be used to test high resolution analog to digital convertors (ADCs), achieving test accuracy beyond 16 bits. In [23-25], computationally efficient algorithms were introduced to relax one of the most stringent precision clock timing requirements: coherent sampling. In [26], a system identification approach was used to identify the parameters in a pipeline ADC which were then used to reconstruct the full code linearity information. In [27, 28], Kalman filtering was combined with the standard histogram method to significantly reduce data acquisition time. In [29, 30], polynomial fitting and segmented measurements were used to test high resolution ADCs with low resolution digital to analog convertors (DACs) as excitation sources. In [31, 32], a new method was introduced for testing the ADC’s spectral performance from available linearity test results, thus eliminating the data acquisition time for spectral testing.

In last year’s International Test Conference (ITC) paper [33], a new algorithm was introduced for accurate linearity test that reduced data acquisition time by over 100 times while maintaining or even improving test precision. The new method is different from all existing reduced time test strategies in that it produces accurate integral non-linearity /differential non-linearity (INL/DNL) test at each and every ADC code. Measurement results for 16 bit successive approximation register (SAR) ADCs demonstrate that the INL/DNL tested by the new method with 1/4 hit per code on average agrees remarkably well with INL/DNL tested by the gold standard servo loop test, at all 65K code locations. A limitation, though, is that the method does not apply to delta sigma ADCs.

In this paper, a new test method is introduced to significantly reduce test time for high performance delta sigma ADCs. The new method, termed SATOM, achieves simultaneous test of many AC and DC specifications using a single data acquisition set obtained with orthogonal multi-excitations. It has been validated with measurement results for test accuracy, computational efficiency, and test

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environment robustness. Test time reduction of well over 90% was achieved versus current state of the art.

2. The SATOM Concept

For ultra-high precision applications, high resolution delta-sigma ADCs are almost exclusively used. For such ADCs, full code linearity (INL(k)/DNL(k)) test is impossible due to the extremely large number of codes and the very slow sampling speed. Instead, linearity test is only done at a significantly reduced number of codes. For 24 bit and higher resolution ADCs, it is not uncommon that only less than 0.0001% of the ADC codes are actually tested in production test in order to limit the test time. Even at such a dramatically reduced code level, linearity test time is still by far the largest component of final test time.

In bench test during post-silicon validation, it is required to test the ADC linearity more rigorously, typically at many more points and many times at 100s times more points. Hence, each linearity test can take several minutes or even much longer. Since the characterization process involves testing for many parameter settings, many voltage levels and at multiple temperatures, the total linearity test time can be many days to many weeks. Therefore, dramatically faster linearity tests can lead to significant reduction in engineering time and time to market.

In addition to linearity test, these ultra-high precision ADCs also require other time consuming tests which are not normally done for other types of ADCs. For example, power supply rejection (PSR) and common mode rejection (CMR) are usually guaranteed by design for low to medium, or even high resolution ADCs, but for ultra-high resolution ADCs customers may require these parameters to be guaranteed for individual devices, thus mandating production test. Testing PSR for analog voltage supplies (AV_{dd} and AV_{ss}) and digital voltage supply (DV_{dd}) may require a significant amount of time.

Depending on the customer requirements and individual company's test flows, several other small signal and large signal tests must also be done at production. Regardless the fine differences, linearity test, PSR test, CMR test, and noise test generally consume the vast majority of total final test time. The goal of this paper is to reduce the test time associated with these tests by a factor of 10 or more comparing to the state-of-the-art production test, but provide test coverage and accuracy similar to bench test.

In the current state-of-the-art, each of these tests are done separately and each with a different methodology. For example, linearity may be tested by applying very stable constant input voltages to the ADC that are also measured by very accurate volt meters and by comparing the ADC output against the meter output. The ADC's offset and noise root meat square (RMS) value may be tested by shorting the ADC input to ground and performing statistical analysis of the ADC output codes. Signal to noise ratio may be tested by applying a near full scale pure sine wave input and performing discrete Fourier transform (DFT) analysis of the ADC output. PSR of AV_{dd} may be tested by shorting the ADC input, applying a square wave at AV_{dd}, and analyzing the ADC output codes. These differences in testing mandate separate tests for these specifications. However, these specifications do not have to be tested as outlined above. In fact, they can be tested all with sine wave inputs applied at various terminals of the ADC. For example, for PSR of AV_{dd}, a small signal sine wave can be added on top of a constant AV_{dd} while the ADC input is shorted. The sine wave component at the ADC output can then be used to compute the ADC's PSR. Similarly, other specifications can also be tested by using appropriate small signal sine waves.

In the SATOM approach, a unified test framework will be undertaken by using sinusoidal signals with appropriate amplitudes and frequencies at various test points. The ADC under test is viewed as what it actually is: a multi-input single output device. The single output is the digital output codes generated by the ADC in response to signals, disturbances, and noise present at various ADC terminals. The desired and main input signal is the differential input voltage to the ADC. The common mode input, the input referred noise, and the variations at terminals that are supposed to be constant are all unwanted inputs to the ADC. This is graphically illustrated in Figure 1. The 4 Δ's represent the small signal variations in the 4 corresponding constant quantities. Ideally, we would like the ADC to respond only to the differential input and reject all other inputs, that is, $D_{out} = V_{id}$.

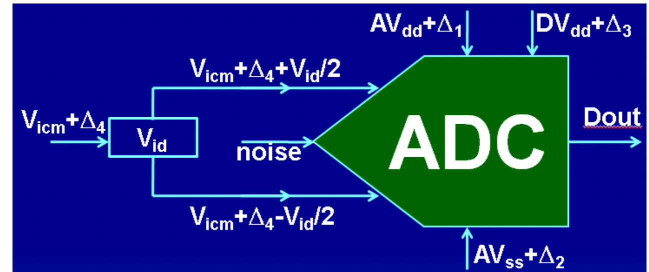

Figure 1. ADC as a multi-input single-output device

In reality, we will have $D_{out} = f(V_{id}, \Delta_1, \Delta_2, \Delta_3, \Delta_4, \text{noise})$ in a nonlinear way. If V_{id} is the only large signal, straight-forward Taylor series expansion gives,

$$D_{out} \approx \delta_0 + (1+\delta_1)V_{id} + \delta_2 V_{id}\text{^}2 + \delta_3 V_{id}\text{^}3 + \ldots + c_1\Delta_1 + c_2\Delta_2 + c_3\Delta_3 + c_4\Delta_4 + (d_1\Delta_1 + d_2\Delta_2 + d_3\Delta_3 + d_4\Delta_4)V_{id}, \ldots$$

In the above expression, the first term δ_0 is the ADC's offset, δ_1 is ADC's gain error, δ_2 produces second order harmonic distortion, δ_3 produces third order harmonic distortion, …, $c_1\Delta_1 + c_2\Delta_2 + c_3\Delta_3$ is due to non-ideal power supply rejection, $c_4\Delta 4$ is due to non-ideal common mode rejection, and $(d_1\Delta_1 + d_2\Delta_2 + d_3\Delta_3 + d_4\Delta_4)V_{id}$ is due to second order inter-modulation between the differential input signal and variations in both power supply and common mode. If there is third order inter-modulation between the input and the various Δ's, a term similar to the last term in the above equation will be included with all d's changed to e's and V_{id} changed to V_{id}^2. By the same pattern, even higher order inter-modulation terms could be

included. Notice that there is no need to include any terms involving small signal quantities of order 2 or higher.

To describe the proposed algorithm, we need the concept of orthogonal signals. Real signals $x_1(t)$, $x_2(t)$, …, $x_k(t)$ are said to be mutually orthogonal over an interval [0, T] if

$$\int_0^T x_i(t)x_j(t)dt = 0 \quad \forall i \neq j,$$
$$\int_0^T |x_i(t)|^2\, dt \neq 0 \quad \forall i.$$

For discrete time signals, the integrals will be replaced by summation over a data record obtained over the given time interval. A set of discrete sinusoidal signals are mutually orthogonal if the data record contains integral but distinct number of periods of each signal.

Since a functional ADC is a stable system, by standard dynamical systems theory, the ADC output to a bounded periodic input will be bounded and periodic with the same period as the input. The multi sinusoidal signals at various ADC terminals can then be viewed as a vector input signal with various sinusoidal components. To apply the dynamical systems theory just mentioned above, we will make sure the vector input is a periodic signal. This is guaranteed by making sure that the frequencies of the various sine components are rationally related.

Under conditions in the last paragraph, the ADC output will be a periodic signal. If the differential input, the common mode input, and the supply variations are all selected to span a different integer number of periods in the data record, all components in the ADC output D_{out} will be mutually orthogonal signals. Their coefficients will be easily computed.

3. The SATOM algorithm

The basic concept of multiple orthogonal excitations explained in the last section will now be developed into a test algorithm for high-resolution delta sigma ADCs. In what follows, a step-by-step procedure will be described for parameter selection, test signal generation, data acquisition, data processing and specification computation. To illustrate the process, some intermediate results will be shown. All results are from actual measurement results, with nothing from simulation.

1) Data record length selection

Data record length M should be selected based on the ADC's sampling frequency and the allowable time. For fast computation of Fourier transform, a power of 2 is recommended. For example, if the ADC's maximum sampling rate is 1 KSPS and we are only allowed about 1 second, then M = 2^10 = 1024 is selected. If we can afford 4 seconds for testing all the AC and DC specifications as shown later, them M = 4096 will be used. More data gives better test coverage and test precision. M can also be selected to be different for bench test vs production test.

2) Multi-excitation frequency selection

Several conditions should be satisfied. As discussed in the previous section, if the vector of input signals is periodic, the theoretical foundation of the algorithm is solid. To satisfy this, we should select frequencies at all input points to be rationally related AND each individual sine wave spans an integer number of periods in the M samples of the data record. Furthermore, from basic signal processing theory, each sine wave should have a minimum of 5 periods in the data record. This can be fairly easily done by selecting the number of periods for each sine source. For example, let J_{in} be an odd integer representing the number of periods of the differential input sine wave in the data record, then the input sine frequency will be $f_{in} = (J_{in}/M)*f_{samp}$. Similarly, we can select J_{AVdd}, J_{AVss}, J_{DVdd}, and J_{ICM}, all to be integers different from J_{in} and different from each other, to define the corresponding input sine wave frequencies. Notice that all integers must be greater than or equal to 5 but less than or equal to M/2 – 5. Also, since the differential input is large signal, it will produce harmonic distortion and inter-modulation tones at higher frequencies. Hence, J_{in} is preferably the smallest among all. Finally, it is important to choose these J's so that the harmonic distortions, inter-modulations, and the five fundamentals all fall in different frequency bins, preferably separated by as much space as possible. It would be more convenient to use a spreadsheet to automatically check for frequency bin collisions.

3) Multi-excitation amplitude selection

The differential input amplitude is typically set at -0.5 dB to -1 dB full scale (FS), or as the data sheet or customer would require for spectral test. The amplitude for AV_{dd}, AV_{ss}, DV_{dd} can be set at 10% nominal values. For a functional ADC, these inputs will only cause small variations in the ADC output that is less than 0.01% full scale, and they do not interfere with the analog input signal. The situation for the common mode input is different, since the common mode input directly adds to the differential mode input. The addition of the common mode sine wave should not cause the overall ADC input signals to go outside their valid ranges. If the ADC's input common mode range is sufficiently large (as is the case with the devices we tested), a convenient choice for the common mode sine amplitude would be around 10% of reference, with the DC common mode set at the middle of its range.

4) Data acquisition

If a precision frequency-synthesizer is conveniently available, it is preferred so that all sine waves are simultaneously coherent with the sampling clock. Alternatively, if an accurate master clock is available, it can be used as reference to all signal generators to attempt to achieve near perfect coherent sampling. Otherwise, simply do the best to achieve coherent sampling with the available resources. With all excitations simultaneously turned on, a set of M samples will be collected. If transient settling is of concern, a waiting period should be given for the transient to die out before taking the first sample. The

collected raw data (digital numbers coming out of the ADC) will be transferred to a computer for processing.

5) Data processing

If perfect simultaneous coherent sampling is achieved, then direct application of the fast Fourier transform (FFT) algorithm is preferred because of its computational efficiency. The mutual orthogonality will ensure that the ADC output response from different excitation sources will not interfere with each other under FFT. The integers selected in step 2 will directly give the frequency bin numbers to look for the corresponding responses.

For ultra precision delta sigma ADCs, achieving perfect coherent sampling is not an easy task, especially when multiple sine sources have to be used. In such cases, an algorithm for non-coherent sampling such as those in [23-25] should be used.

In this paper, since 5 non-synchronized sine wave excitations are simultaneously used, a creative application of non-coherent sampling must be done carefully. We take the general approach of "frequency domain identification, time domain correction, plus residue transformation." Even though mathematically time domain and frequency domain carry exactly the same information, our empirical experience shows that our approach can be 1000s times more efficient in computation time than the time-domain four-parameter-sine-fitting method as suggested in the IEEE standard [1]. The following sequence of plots illustrates the spectral analysis processing steps.

First, the raw data was passed through FFT and the resulting spectrum was shown as the blue curve in Figure 2 below. The major peak near 0 dB is due to the differential analog input. It is slightly non-coherent. A non-coherent identification algorithm was used in the frequency domain to identify the fundamental, which was then removed in the time domain. The residue signal was passed through FFT again and the resulting spectrum was shown as the red curve. The next largest spectral component is clearly non-coherent component and was due to the common mode input signal.

The non-coherent algorithm was applied again to accurately identify the common mode input signal. The identified non-coherent fundamental was then removed in the time domain, and the residue spectrum was show as the black curve in Figure 3.

The largest components in the black spectrum are due to product of the differential input signal and the signals at AV_{dd} and AV_{ss} (the 2nd order inter-modulation). These frequency bins are at $J_{AVdd} \pm J_{in}$ and $J_{AVSS} \pm J_{in}$. The non-coherent algorithm was applied to identify these terms in the frequency domain and to remove them in the time domain. The new residue spectrum was green in Figure 4.

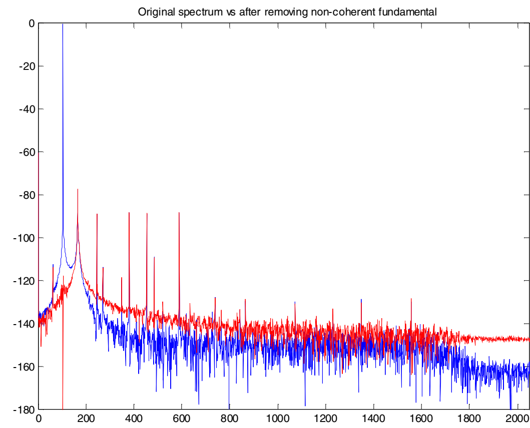

Figure 2. Initial spectrum and spectrum after removing the non-coherent fundamental from the differential input

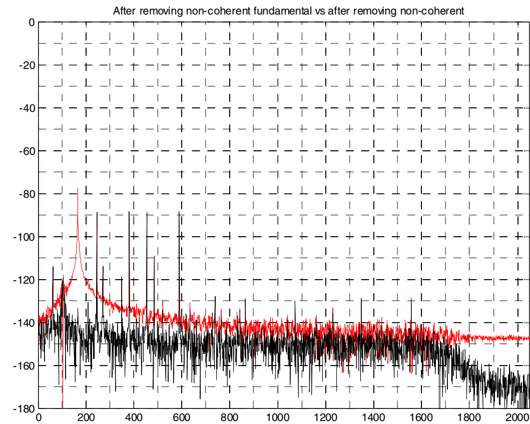

Figure 3. Spectrums before and after removing the non-coherent fundamental from the common mode input

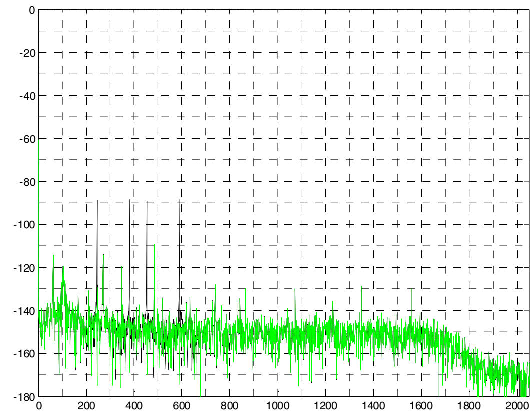

Figure 4. Spectrums before and after removing the 2nd order inter-modulation between V_{id} and AV_{dd}/AV_{ss}

In the green spectrum, it contains the ADC's harmonic distortion components, fundamental components from $AV_{dd}/AV_{ss}/DV_{dd}$, as well as higher order inter-modulations between V_{id} and AV_{dd}/AV_{ss}. Since these are all fairly small, the order in which each component is computed is no longer important. In this illustration, we first identify and remove the higher order inter-modulation components. The residue spectrum was shown as the blue curve in Figure 5.

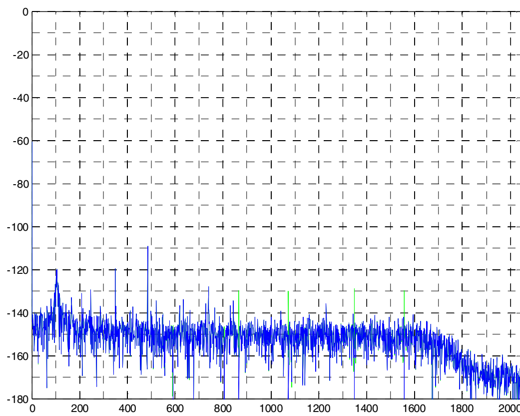

Figure 5. Spectrums before and after removing the higher order inter-modulation between Vid and AV_{dd}/AV_{ss}

In the blue spectrum, we see a little bit of "spectral leakage" around the differential input fundamental frequency bin. This is due to a slight drift in frequency caused by a slight drift in the reference voltage. One possible solution is to exclude the affected bins from computation of total noise. The second approach is to perform anti-drift averaging in the time domain to remove the spectral leakage. With the second approach, the resulting spectrum was shown in Figure 6. Notice that a different vertical scale was used to allow for a little more details. The Vid's harmonic distortion components and the fundamental components due to AV_{dd}, AV_{ss}, and DV_{dd} were still present. The power in these bins could now be used to compute the ADC's specifications.

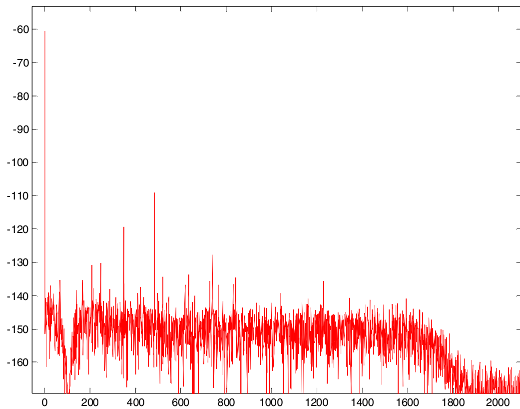

Figure 6. Spectrum after removing leakage due to V_{id} frequency drift

6) Computing AC and DC specifications

From the identified V_{id} fundamental, the ADC's output amplitude and the ADC's gain error can be computed. From the final spectrum's DC component, the ADC's offset voltage can be computed accurately. From the identified powers from the AV_{dd}, AV_{ss}, DV_{dd}, and ICM, the PSR of AV_{dd}, PSR of AV_{ss}, PSR of DV_{dd}, and CMR can be computed. From the V_{id} harmonic distortion component powers, the ADC's total harmonic distortion (THD) and spurious-free dynamic range (SFDR) can be computed for the tested power level. By appropriately excluding certain bins, summing up the total power from the rest bins, and scaling according to the number of bins in the summation, the ADC's zero input noise RMS value, and the ADC's signal noise ratio (SNR) can be computed. Combining with THD information, the ADC's signal to noise plus distortion ratio (SNDR) and equivalent number of bits (ENOB) can be computed.
To compute the ADC's integral nonlinearity (INL) curve, the harmonic distortion components are first scaled according to output amplitude and the order of the distortion term. After proper scaling in the spectrum, the inverse FFT is used to transform it back to an error signal in the time domain. By cross indexing the time domain ADC output codes and the time domain error signal, the ADC's integral nonlinearity error at those observed output codes can be computed. Plotting the error vs code produces the ADC's INL curve.

To summarize, from a total of M data points, the following ADC specifications can be computed accurately:

- offset, gain error, output power
- PSR of AV_{dd}, AV_{ss}, and DV_{dd}, CMR
- noise RMS, SNR, THD, SFDR, SNDR, ENOB
- M-point INL curve, INL in µV, INL in ppm

4. Measurement Results

As described in the last section, SATOM uses a single data record and simultaneously computes many AC and DC test parameters. Among these, linearity (INL) is the one that takes the most amount of time in conventional test. Test accuracy and precision requirements for INL are also among the most stringent. Furthermore, the proposed method uses sinusoidal input and is fundamentally a frequency domain test method. Therefore, there is less concern about SATOM's effectiveness in testing traditional AC test parameters, and the major issue is whether or not it can actually test INL accurately. Because of this, most of our validation efforts will be focused on INL testing, and most of measurement results are intended to demonstrate functionality, accuracy, repeatability, and robustness of SATOM in INL testing. After that, we will provide a set of complete test results of all parameters listed at the end of section 3 for one device, and compare the results against those obtained with conventional methods that require much longer test time.

Extensive measurements were conducted at Texas Instruments. A commercially available high resolution high performance delta sigma ADC was used for validation. The choice of the product carries no significance and is purely based on availability and convenience. To demonstrate the accuracy of the proposed method, we would need good parts, marginal parts, and bad parts. However, to actually find a sufficient number of marginal parts and bad parts may require a significant amount of effort, especially if the part has high yield. Instead, we decided to run the clock rate at significant higher than the maximum spec rate to cause performance

degradation. This will effectively create marginal and bad parts.

The frequencies for the multiple sine waves were selected using a spreadsheet to avoid frequency collisions among harmonic and inter-modulation frequencies. For the given test setup, our ability to achieve coherent sampling is very limited, since we have to use individual stand-alone function generators as excitation sources. Hence, we were forced to use the non-coherent sampling spectral analysis algorithm. The number of samples M used was either 2^10, 2^11, or 2^12. With SATOM, INL values at M points are computed.

The INL of each device was tested with SATOM and was tested again with the conventional method of DC metering. Results for a good part and a bad part were shown in the upper and lower panes of Figure 7 respectively. The horizontal axis represents the interpreted voltage in volts of the ADC output. The vertical axis represents the ADC's integral nonlinearity errors in micro volts. Results from SATOM were in black. 4096 INL points were obtained from the M=4096 data samples. Results from the conventional method were shown in red. Due to the large amount of time required, the conventional method was limited to a 21 point test.

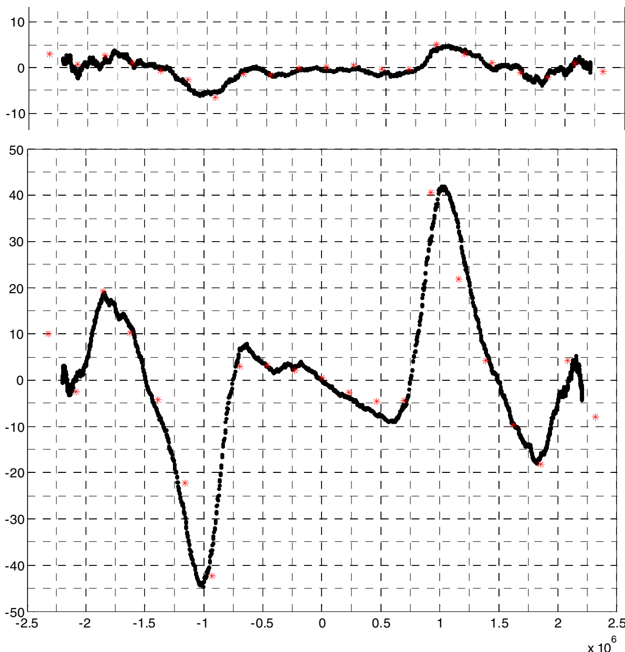

Figure 7. INL curve of a good part (upper) and that of a bad part (lower) tested with SATOM (black) and with conventional DC metering (red)

From Figure 7, it can be clearly seen that the SATOM generated INL results agreed with the conventional results very closely, in both the overall INL value and the inner structure of the INL curve shape. These measurements were repeated for multiple devices and for each device the SATOM method was repeated 25 times to verify repeatability. Due to time consumption, the conventional method was only repeated 8 times for each device. The random variation ranges for both methods were comparable, and were at about 4 μV.

Next, the number of samples in the data record is reduce to M=1024 for the proposed method. The same measurement results from the convention method were used for comparison. Figure 8 below shows the results for one marginal device. The horizontal and vertical axes carry the same meaning as those in Figure 7. As pointed out above, the random uncertainties in the red (conventional) measurement are about 4 μV. The same device was tested 10 times with the proposed method, each using M=1024 samples. Ten blue INL curves were shown in Figure 8. It is clear that at only M=1024 samples, both accuracy and repeatability are at the random uncertainty level of the reference conventional method.

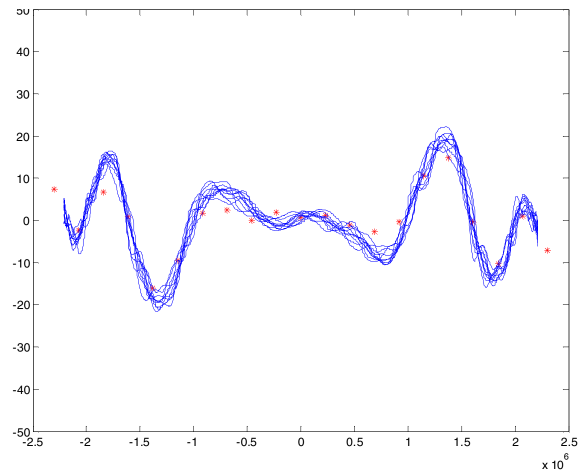

Figure 8. INL plots of a marginal device, measured 10 times with the proposed method (ten 1024-point curves in blue) and compared against conventional method (one 21-point measurement in red)

Figure 9 above shows the results for one bad device. Similar to Figure 8, results from ten repeated tests with the proposed method were shown in blue, each using M=1024 samples. As a reference, the 21-point INL measurement results from the conventional method was shown in red.

In Figure 10 below, the measurement results for a good device were displayed. Again, the ten blue curves were results from ten repeated measurement using the proposed method, each time using M=1024 samples. The red curve is the INL measurement using the conventional approach. From this figure, it can be seen that the match between the new method and the conventional method is excellent. Both accuracy and repeatability are well within the uncertainty band. Also notice that the agreement for the good device is significantly better than for the marginal or bad device. This might be explained by the fact that the bad device was not an actual bad device, it was made bad by over driving the clock rate. At the overly accelerated clock rate, some of the errors may be of dynamic nature, leading to time varying performance.

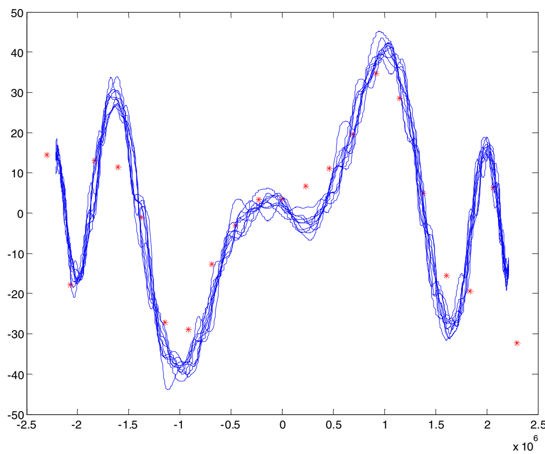

Figure 9. INL plots of a bad device, measured 10 times with the proposed method (ten 1024-point curves in blue) and compared against conventional method (one 21-point measurement in red)

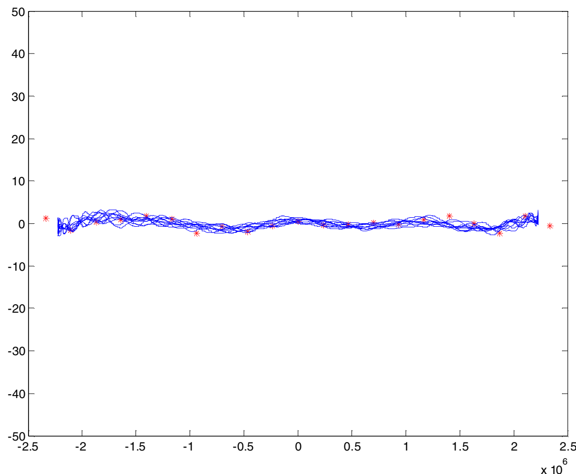

Figure 10. INL plots of a good device, measured 10 times with the proposed method (ten 1024-point curves in blue) and compared against conventional method (one 21-point measurement in red)

The results presented so far have established functionality, accuracy, repeatability, and robustness of the proposed SATOM method in testing the ADC INL performance, which is the most challenging and most time consuming part among all specifications. In Table 1, the complete test results for one device were summarized. The mid column in the table lists the ADC specifications as tested by the proposed method using only M = 1024 samples in the data record. For an ADC running at 1 KSPS, this would only require 1 second of data acquisition time. Total processing time is less than 0.1 second. For comparison, some specifications tested with conventional bench test approaches are listed in column 3, except that the INL was tested with 21 point test.

Notice that test results agree with each other extremely well. The only two numbers that show noticeable differences are AV_{dd} PSR (1.04 dB difference) and DV_{dd} PSR (1.88 dB difference). Since these differences happened at below the -110 dB level, we need to be careful in looking at the dB differences. If we actually convert these into actual power differences, these differences are very close to noise floor.

Table 1. Summary and comparison of test results

Specification	New method	Standard method
ADC Offset	1.0741 mV	1.076 mV
Output Power	-1.07 dB	
V_{indiff} g.e.	-5.98%	-5.98%
V_{indiff} gain	-0.54 dB	
AV_{dd} PSR	-110.96 dB	-112 dB
AV_{ss} PSR	-88.19 dB	-88.5 dB
DV_{dd} PSR	-117.12 dB	-115 dB
V_{icm} reject	-107.17 dB	
Noise RMS	3.97 µV	4 µV
SNR	112.51 dBFS	112.5 dBFS
THD	-109.28 dBFS	-109 dBFS
SFDR	113.35 dBFS	113 dBFS
SNDR	107.59 dBFS	107.3 dBFS
ENOB (SNDR)	17.61 bit	17.6 bit
Max Abs INL	20.51 µV	
Maximum INL	4.36 ppm	4.7 ppm

Because the bench-test setup was put together for easy access and easy modification, instead of for standard, repeated bench tests, the time it took to obtain the results in column 3 was unrealistically long and was in the order of tens of minutes. If the procedure were to be optimized for speed, the time would be reduced to a fraction of that but would still be orders of magnitude longer than the SATOM time of 1 second. Furthermore, in careful characterization test, the INL may need to be tested at 100s of points or even more, rather than 21 points. When this is repeated many many times, the total characterization time would be very significant.

The comparison to bench test is mainly for the purpose of establishing accuracy and robustness of the proposed SATOM approach, since standard bench test is taken as he correct reference. However, the time comparison in the last paragraph should only be taken qualitatively rather than quantitatively. For quantitative test time comparison, we should use actual test time in an optimized production test flow. Fortunately, the 24-bit delta-sigma ADC used in this evaluation is currently in production. The production test time for testing the specifications listed in the table is about 15 seconds with quad-site testing. If the SATOM approach were to be implemented with quad-site testing, the effective test time would be well under 1 second, even if generous allowance for setup time, settling time, and processing time were to be included. This would correspond to a test time reduction of well over 90%.

5. Limitations

The theoretical foundation of the proposed method requires mutually orthogonal excitation signals. For easy

signal generation, we used sinusoidal excitation signals. A sufficient condition is that the various sine waves have frequencies that are rationally related to each other. The common period for all the sine wave is the beat frequency. In order for the sampled data to be orthogonal, the data record length must be an integer multiple of the common period. When this is satisfied, all sine waves are coherently sampled. Therefore, effort must be made to try to achieve simultaneous coherent sampling for all excitation components.

A second limitation is in the number of samples needed for accurate testing. Due to the presence of both harmonic distortion and inter-modulation, more frequency bins are consumed by these distortion bins. Hence, more data points are needed comparing to a standard single tone spectral test. If the ADC is extremely slow, this will still require significant amount of time.

As commented in the algorithm section, when we add the differential mode input and the common mode input, we have to make sure that the resulting ADC input voltages will remain in their valid range. Since the differential signal is already near full range, this may pose difficulties if the input common mode range is not sufficient. When that happens, the CMR should be tested separately.

With an M-point data record, the proposed algorithm computes INL at M different codes. But these M points on the INL curve are not uniformly distributed, with more points crowded at the two ends. This is different from the usual reduce code test. This is certainly different from the traditional INL test.

As described in this paper, SATOM is intended for ultra-precision delta sigma ADC test. It is not intended for pipeline or SAR ADCs. However, the concept can be extended to general ADC test with proper modifications. Nevertheless, for SAR and pipeline ADCs, the algorithm presented in last year's ITC [33] is much better suited.

6. Discussion

The limitation that the proposed algorithm is only intended for application to ultra-precision delta sigma ADCs is not a significant one. In fact the basic concept of SATOM can be extended to all type of ADCs and all types of DACs, and to amplifiers and filters. The concept of orthogonal excitation is a powerful one. The orthogonality minimizes cross interferences and plays a critical role in enabling simultaneous testing of many parameters.

Although the goal of reducing test time at final production test is what drove the algorithm development, but the method applies equally well to characterization test. Since characterization is very thorough involving many repeated tests in various conditions, the new method can significantly cut down the characterization time. Since characterization time is engineering time, its per unit cost is much more significant. Furthermore, faster characterization also leads to faster time to market.

The proposed SATOM method is also extremely well suited for multi-site testing. If quad site testing is used, the same sine input signals can use used to excite all site at the same time. Then the effective data acquisition time will be further reduced by a factor of four. Since the processing time is less than 0.1 second, it is still negligible, especially if pipelining can be done. Comparing this test time for all the parameters listed in Table 1, this can easily represent well over 90% reduction in test time.

7. Conclusions

A new test strategy has been introduced to dramatically reduce test time for precision analog and mixed signal products. The basic concept and the theoretical foundation of the proposed strategy for Simultaneous AC-DC Test with Orthogonal Multi-excitations are explained. In SATOM, a device under test is excited with multiple stimulus signals that are mutually orthogonal and applied at several independent input points to the device. The SATOM algorithm was described in detail, step by step, together with illustrating example showing how intermediate results would look like. Details on how to compute things efficiently are also given. With the given algorithm, a single set of response data is used to simultaneously compute many AC and DC test specifications. This results in a reduction of well over 90% in test time for those specs, with no negative impact on test coverage and test accuracy. Extensive measurement results demonstrated effectiveness, efficiency and robustness of the new method.

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