1.Introduction

If the automobile had followed the same development cycle as the computer, a Rolls-Royce would today cost $100, get one million miles to the gallon and explode once a year

Most of slides come from Semiconductor Manufacturing Technology
by Michael Quirk and Julian Serda

Semiconductor processing

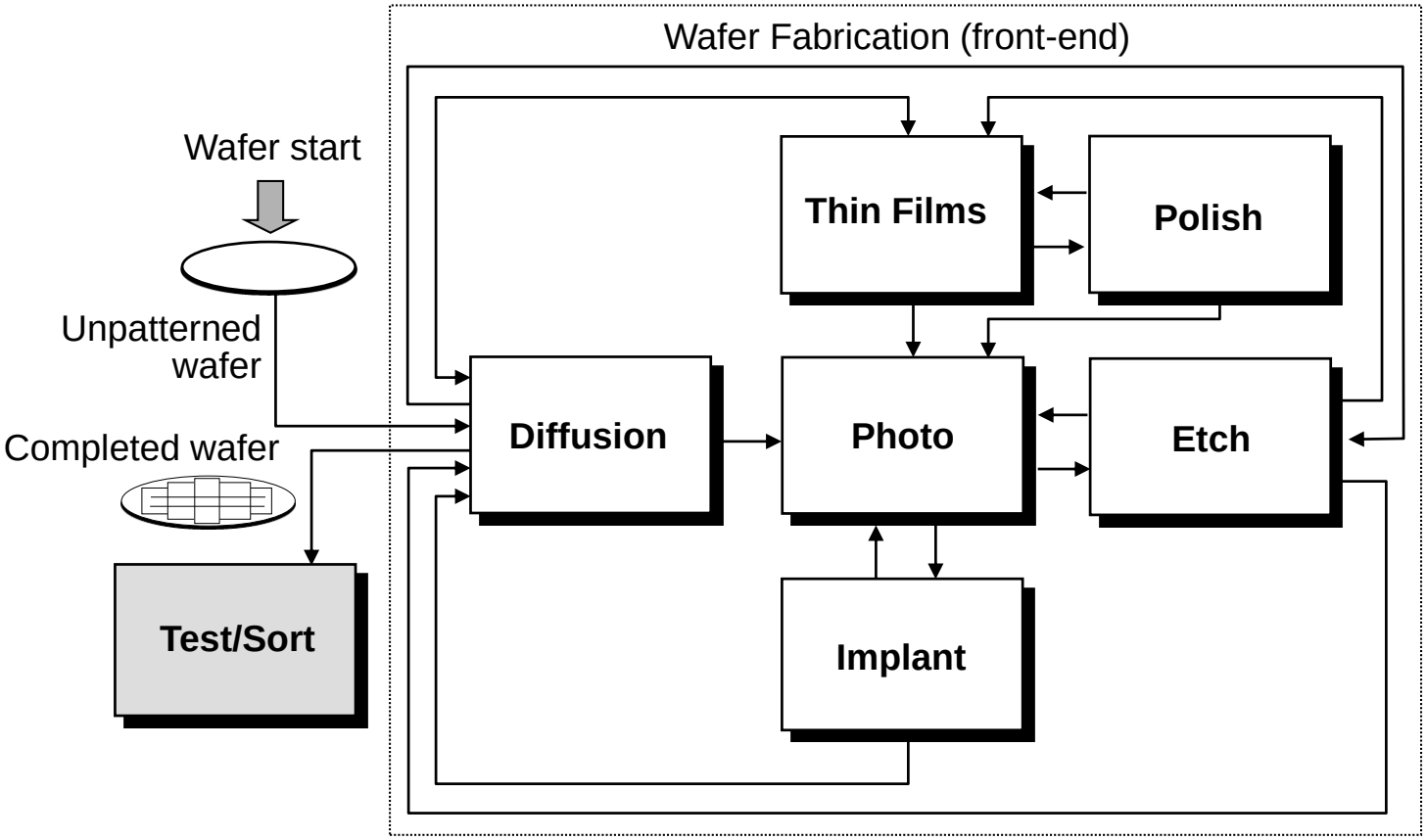
- Semiconductor fabrication
- Layout fundamental
- **Semiconductor testing**
- Semiconductor assembling

Different Electrical Tests for IC Production (From Design Stage to Packaged IC)

Test	Stage of IC Manufacture	Wafer- or Chip-Level	Test Description
IC Design Verification	Pre-Production	Wafer level	Characterize, debug and verify new chip design to insure it meets specifications.
In-Line Parametric Test	Wafer fabrication	Wafer level	Production process verification test performed early in the fabrication cycle (near front-end of line) to monitor process.
Wafer Sort (Probe)	Wafer fabrication	Wafer level	Product functional test to verify each die meets product specifications.
Burn-In Reliability	Packaged IC	Packaged chip level	ICs powered up and tested at elevated temperature to stress product to detect early failures (in some cases, reliability testing is also done at the wafer level during in-line parametric testing).
Final Test	Packaged IC	Packaged chip level	Product functionality test using product specifications.

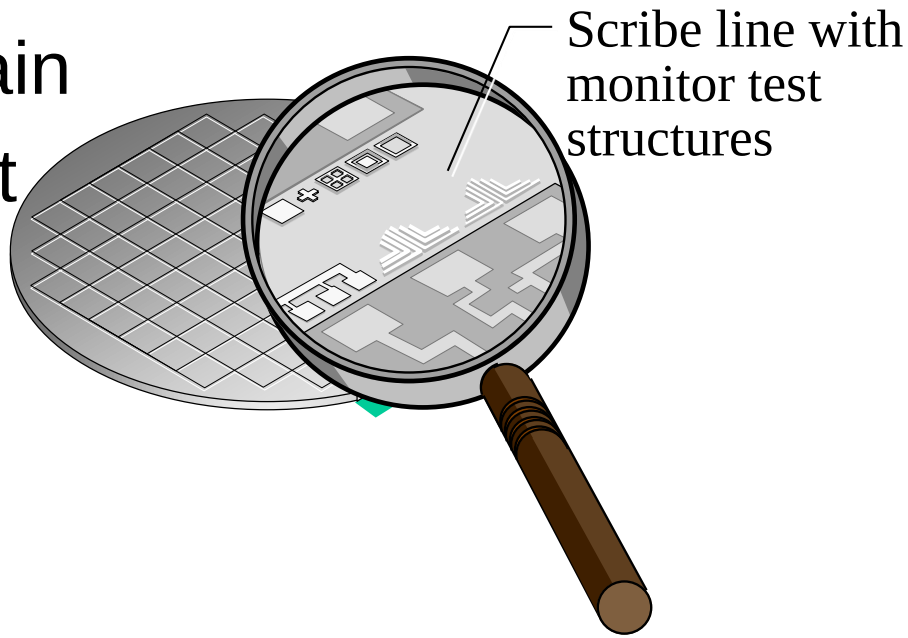
Automated Electrical Tester

Wafer Fab Process Flow with Test



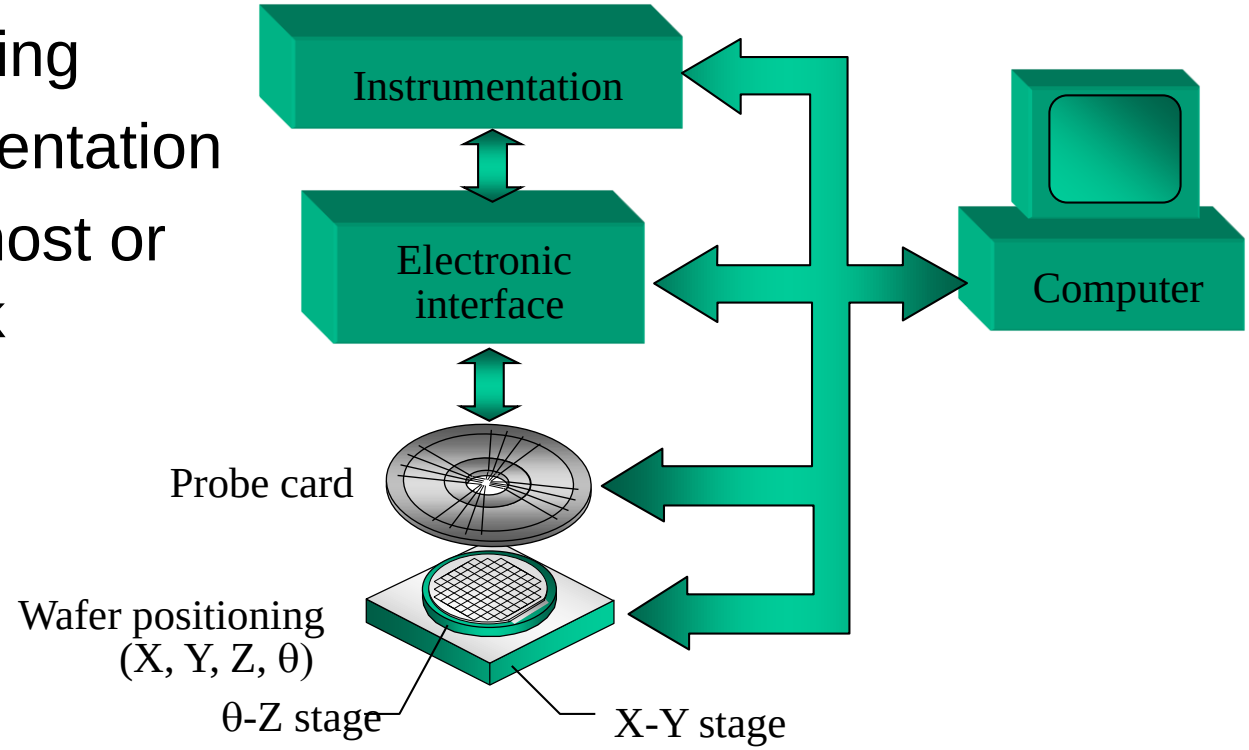
Wafer Test

- In-line Parametric Test (a.k.a. wafer electrical test, WET)
  - In-line test structure
  - In-line test type
  - In-line test data explain
  - In-line test equipment

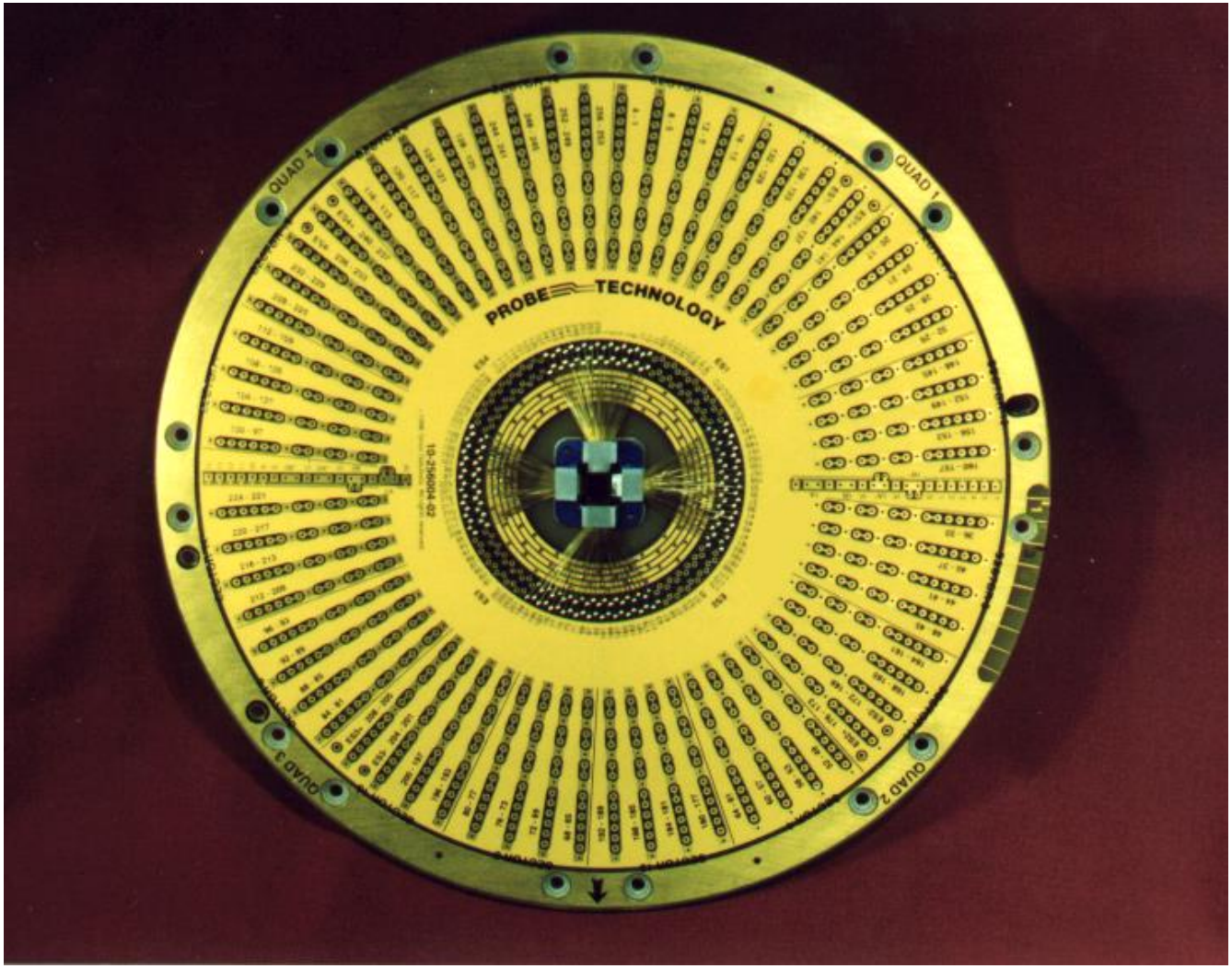


In-line Parametric Test Systems

- Probe card interface
- Wafer positioning
- Tester instrumentation
- Computer as host or server/network



Probe Card for Automatic Tester



Examples of Test Structure

Test Structure	Fault Measurement
Discrete transistors	Leakage current, breakdown voltage, threshold voltage and effective channel length
Various line widths	Critical dimensions
Box in a box	Critical dimensions and overlay registration
Serpentine structure over oxide steps	Continuity and bridging
Resistivity structure	Film thickness
Capacitor array structure	Insulator materials and oxide integrity
Contact or via string	Contact resistance and connections

Data Trends

- The same die location keeps failing a parameter on a wafer.
- The same parameter is consistently failing on different wafers.
- There is excessive variation (e.g., > 10%) in measurement data from wafer to wafer.
- Lot-to-lot failure for the same parameter, indicating a major process problem.

Wafer Sort

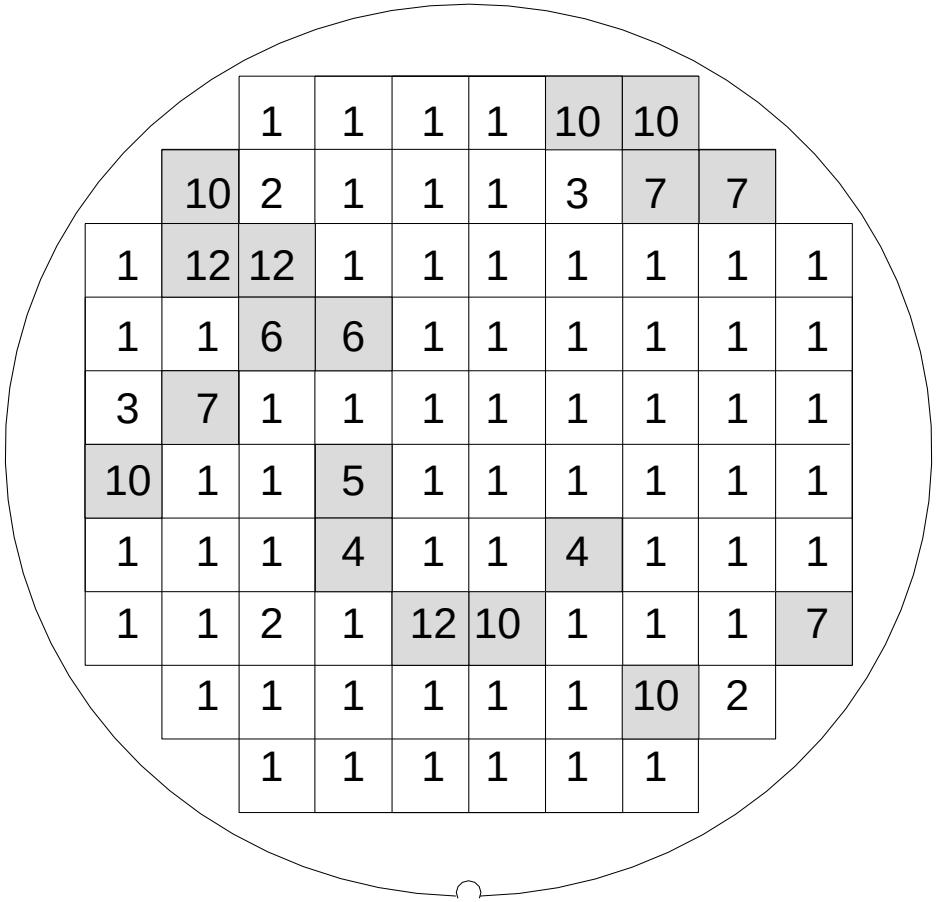
- Wafer Sort (a.k.a. wafer probe)
  - DC testing
  - Output checking
  - Function testing
- The Objectives of Wafer Sort
  - Chip functionality: verify the operation of all chip functions to insure only good chips are sent to the next IC manufacturing stage of assembly and packaging.
  - Chip sorting: sort good chips based on their operating speed performance (this is done by testing at several voltages and varying timing conditions).
  - Fab yield response: Provide important fab yield information to assess and improve the performance of the overall fabrication process.
  - Test coverage: Achieve high test coverage of the internal device nodes at the lowest cost.

Wafer Bin Map with Bin Failures

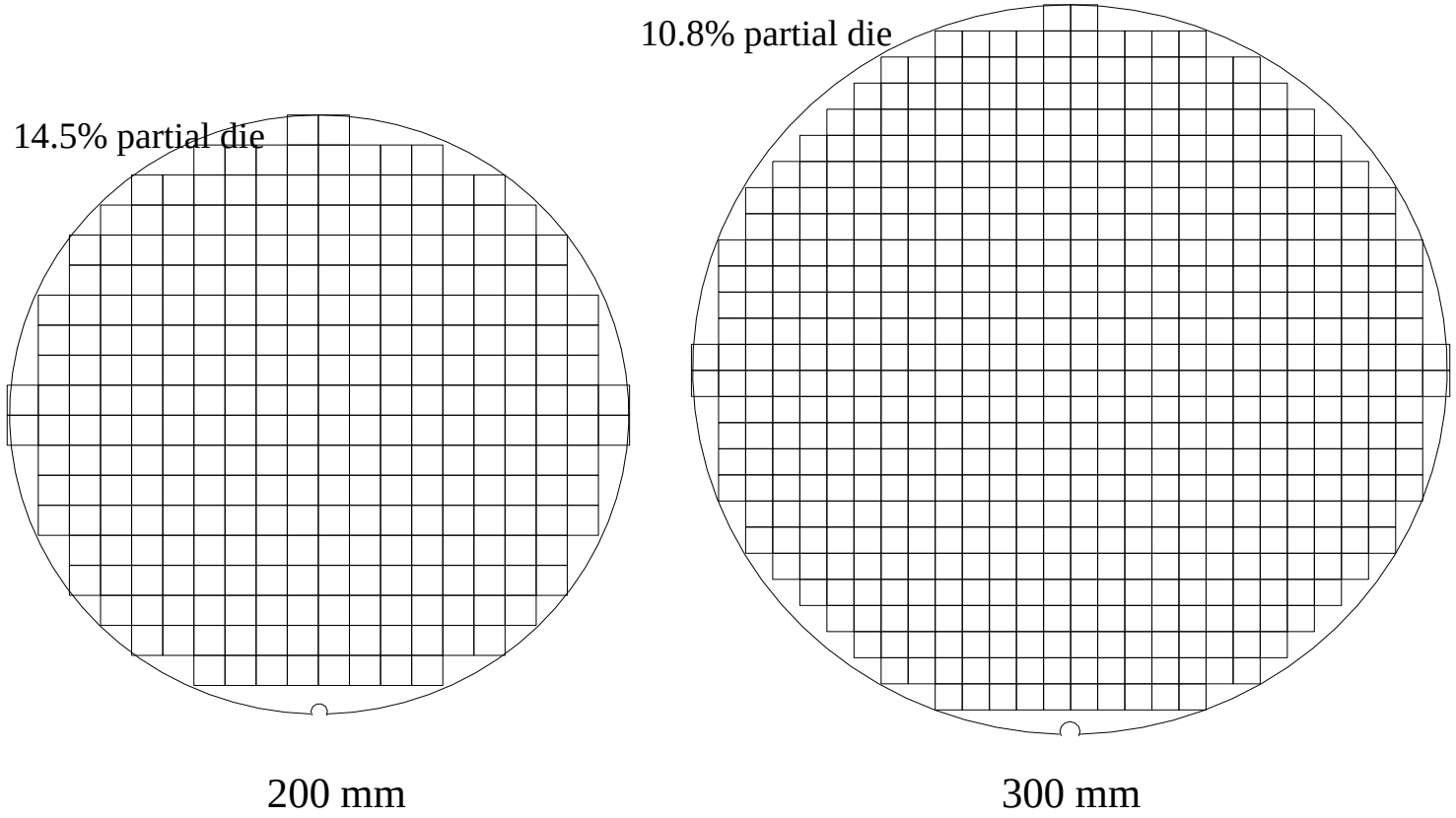
Device:	Example
Lot:	Example
Wafer:	200 mm
Layer:	Hardware Bins
Yield:	79.54%
Good:	70
Total:	88

Good

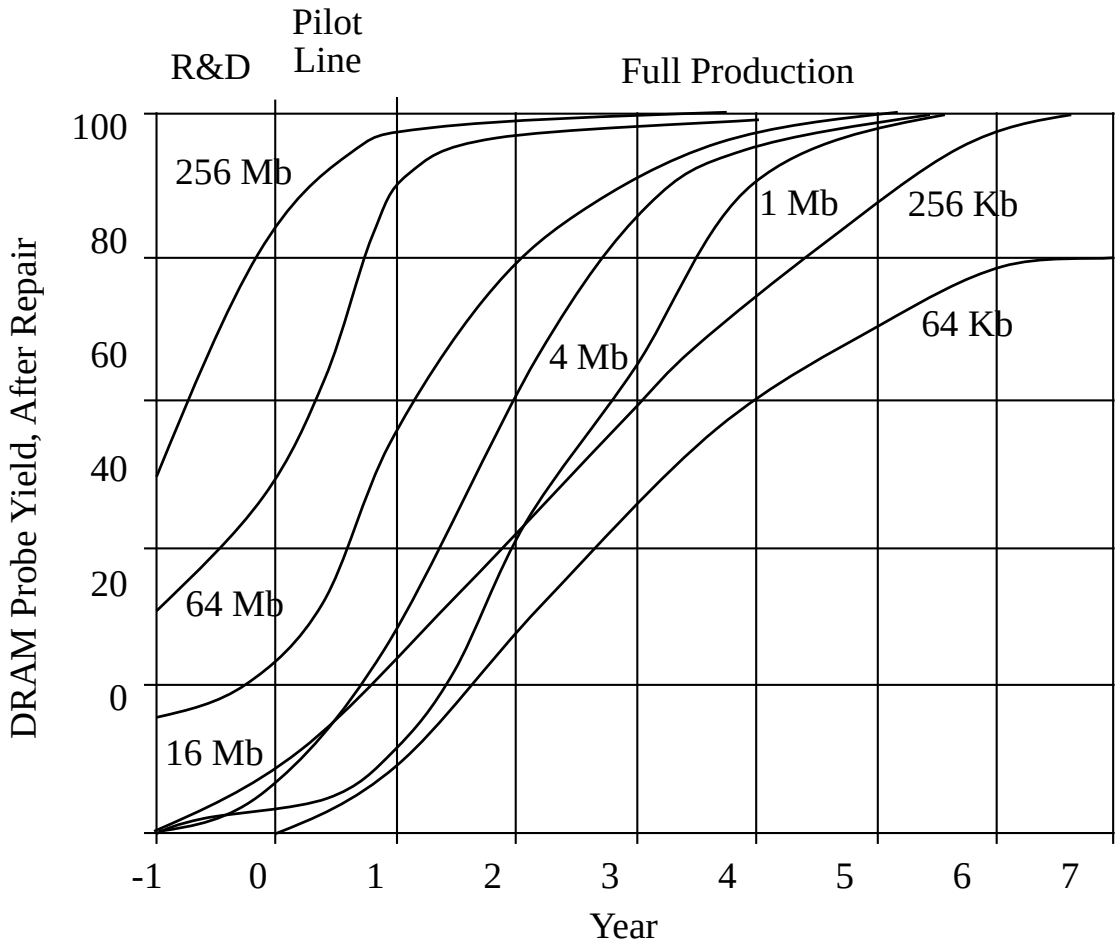
Bad



Reduced Partial Die on Large Wafer



Reduced Time to Product Maturity for DRAM Production



Semiconductor processing

- Semiconductor fabrication
- Layout fundamental
- Semiconductor testing
- **Semiconductor assembling**

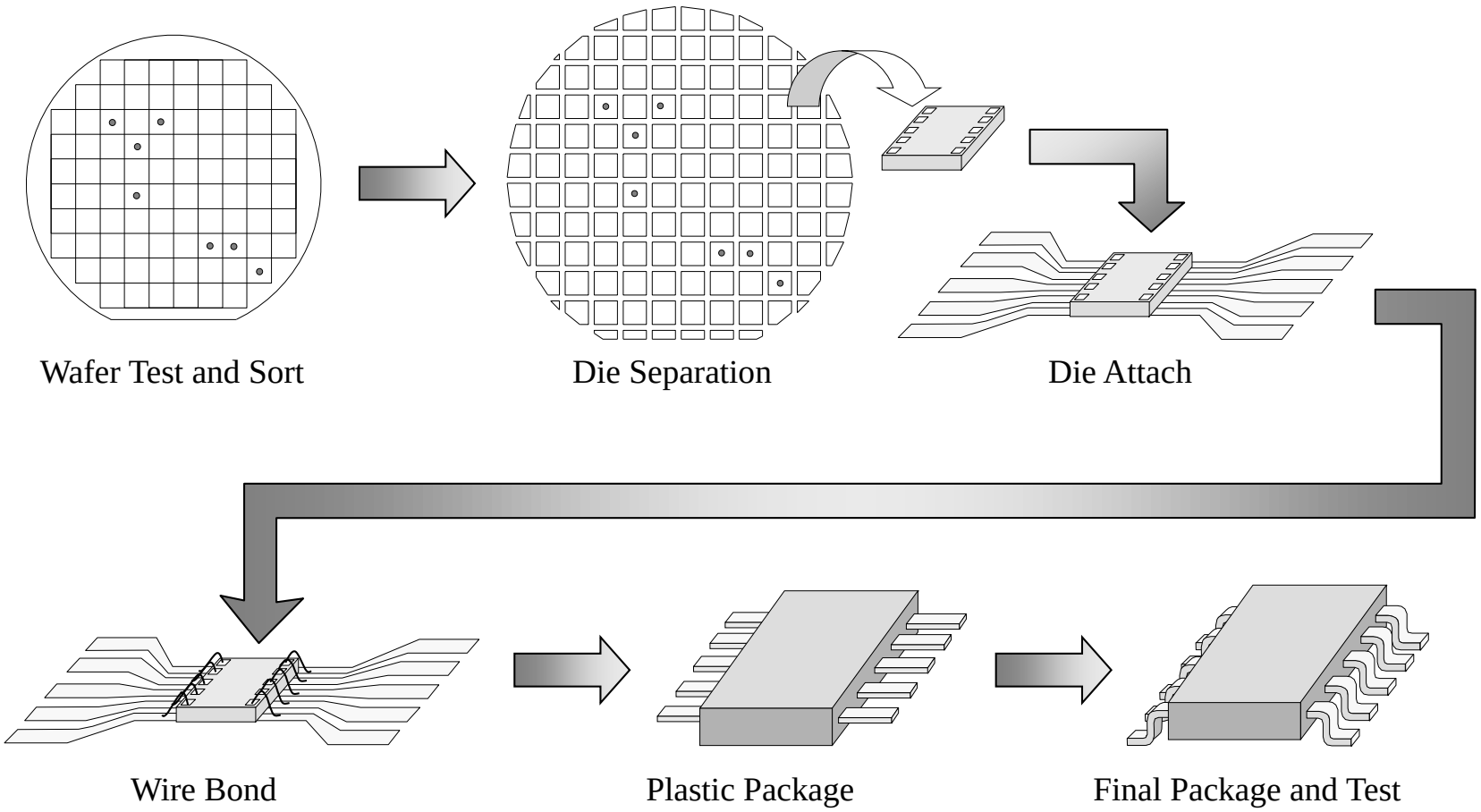
Packaging Requirements

- Electrical: Low parasitics
- Mechanical: Reliable and robust
- Thermal: Efficient heat removal
- Economical: Cheap

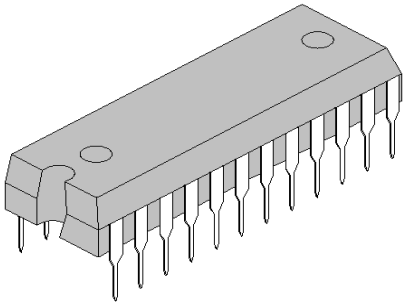
Important Functions of IC Packaging

- Protection from the environment and handling damage.
- Interconnections for signals into and out of the chip.
- Physical support of the chip.
- Heat dissipation.

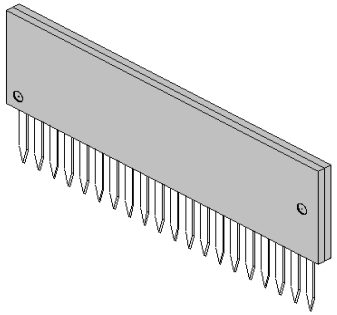
Traditional Assembly and Packaging



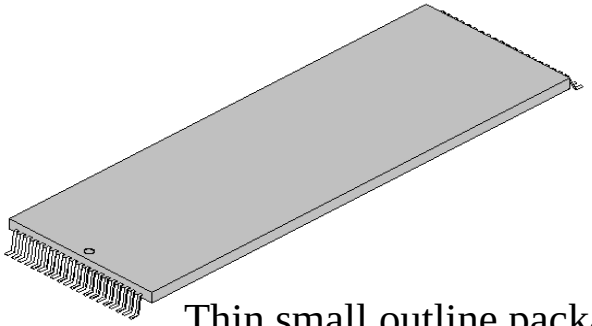
Typical IC Packages



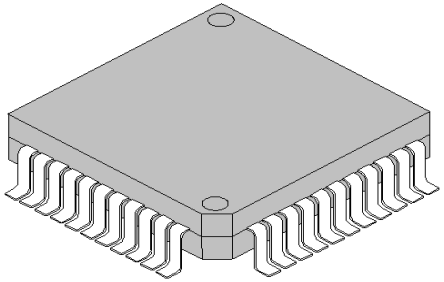
Dual in-line package
(DIP)



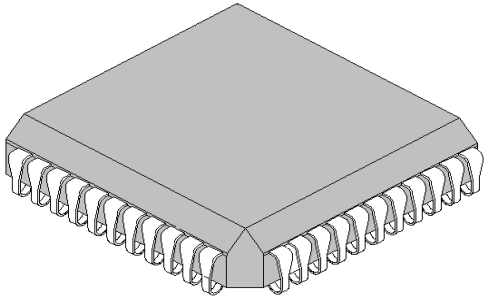
Single in-line package
(SIP)



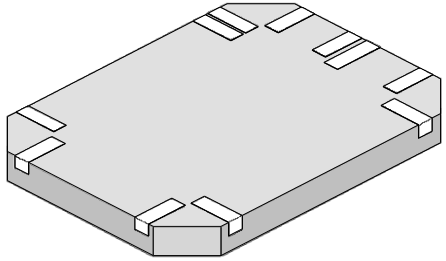
Thin small outline package
(TSOP)



Quad flat pack
(QFP)

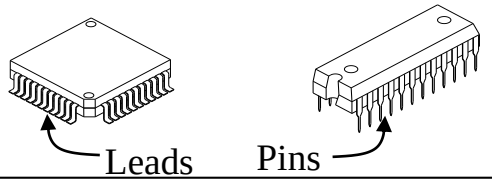
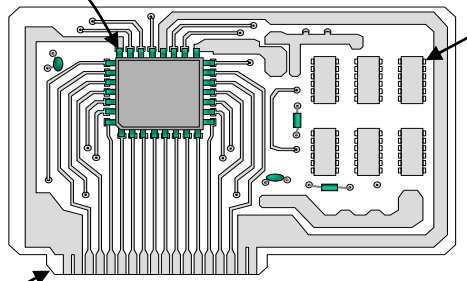
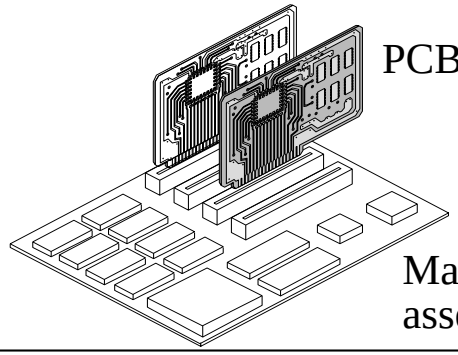


Plastic leaded chip carrier
(PLCC)



Leadless chip carrier
(LCC)

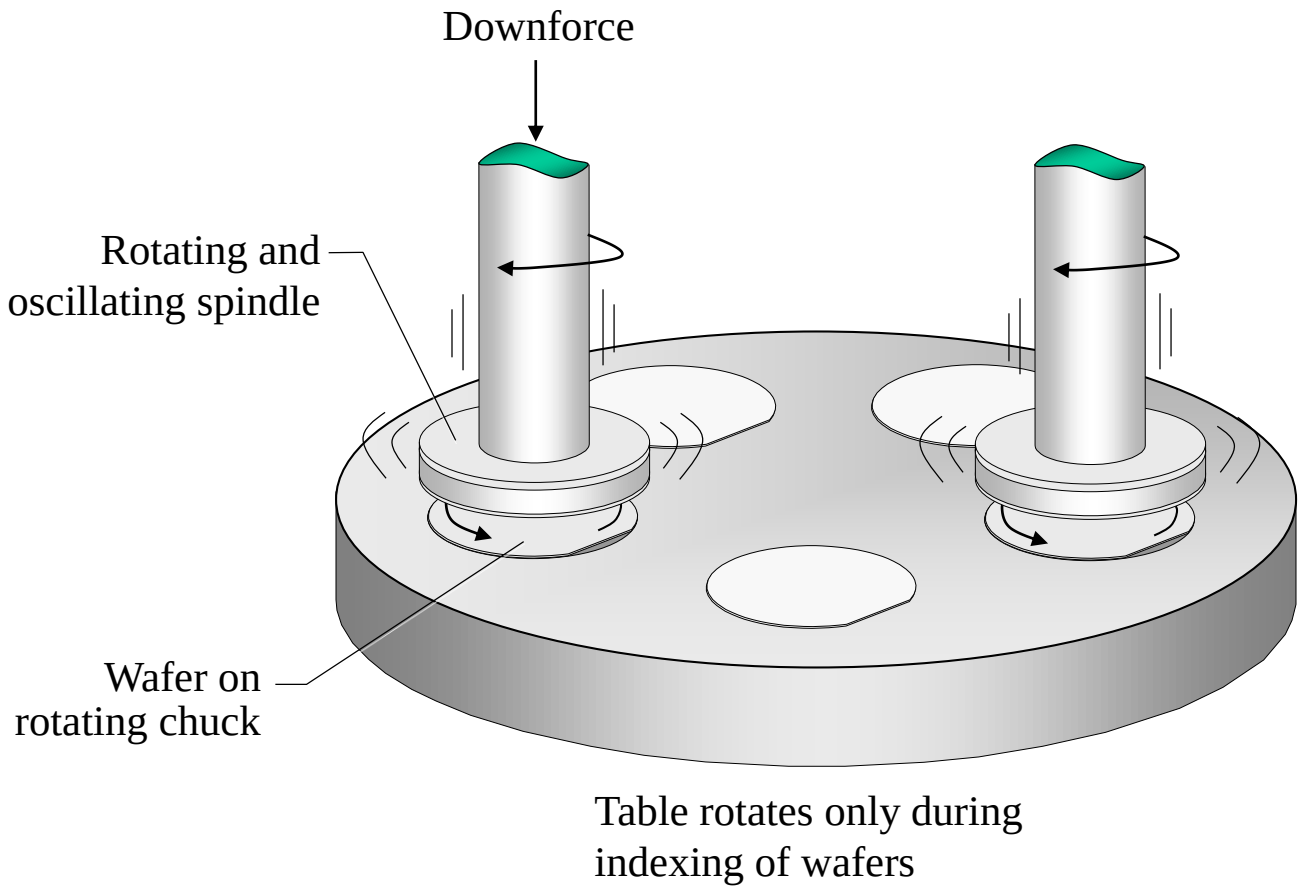
Levels of IC Packaging

First level packaging: IC packaging	Metal leads for mounting onto printed circuit board 
2nd level packaging: Printed circuit board assembly	
Final product assembly: Final assembly of circuit boards into system	

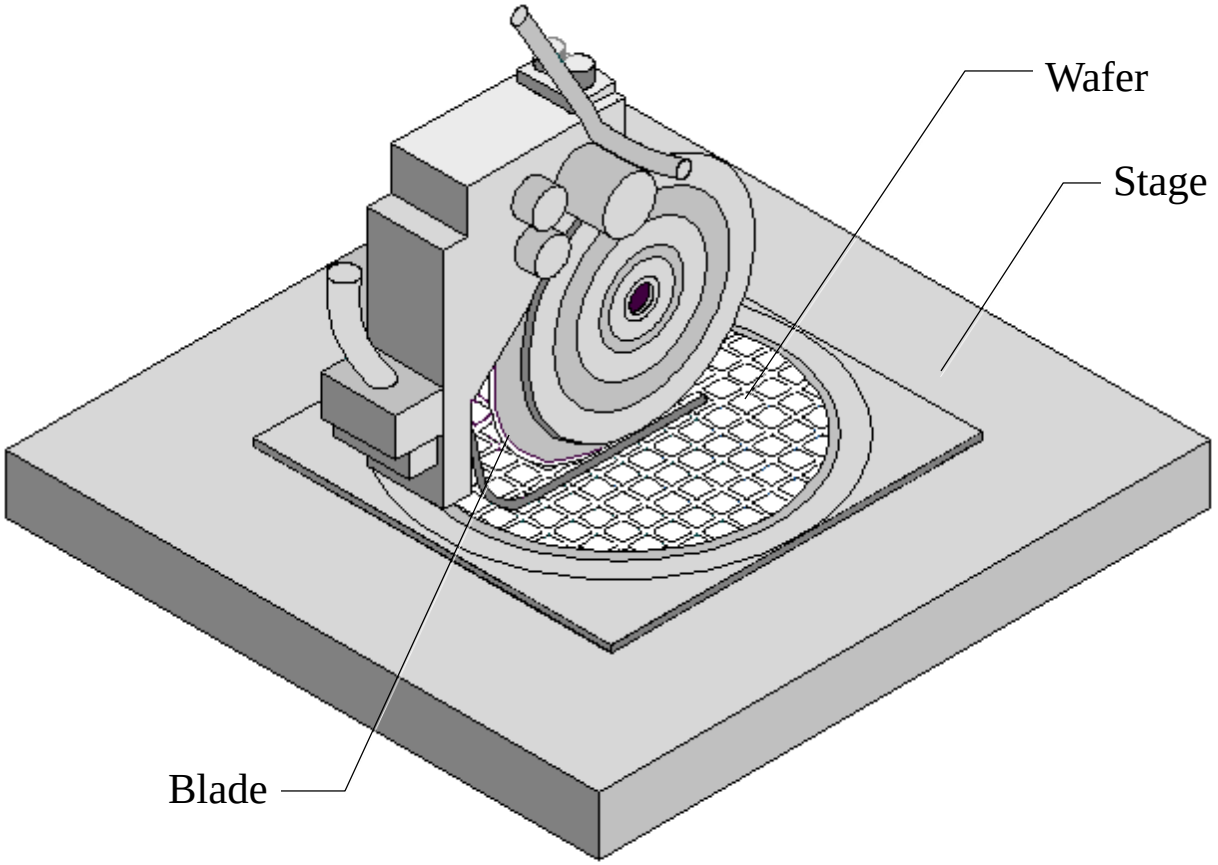
Traditional Assembly

- Wafer preparation (backgrind)
- Die separation
- Die attach
- Wire bonding

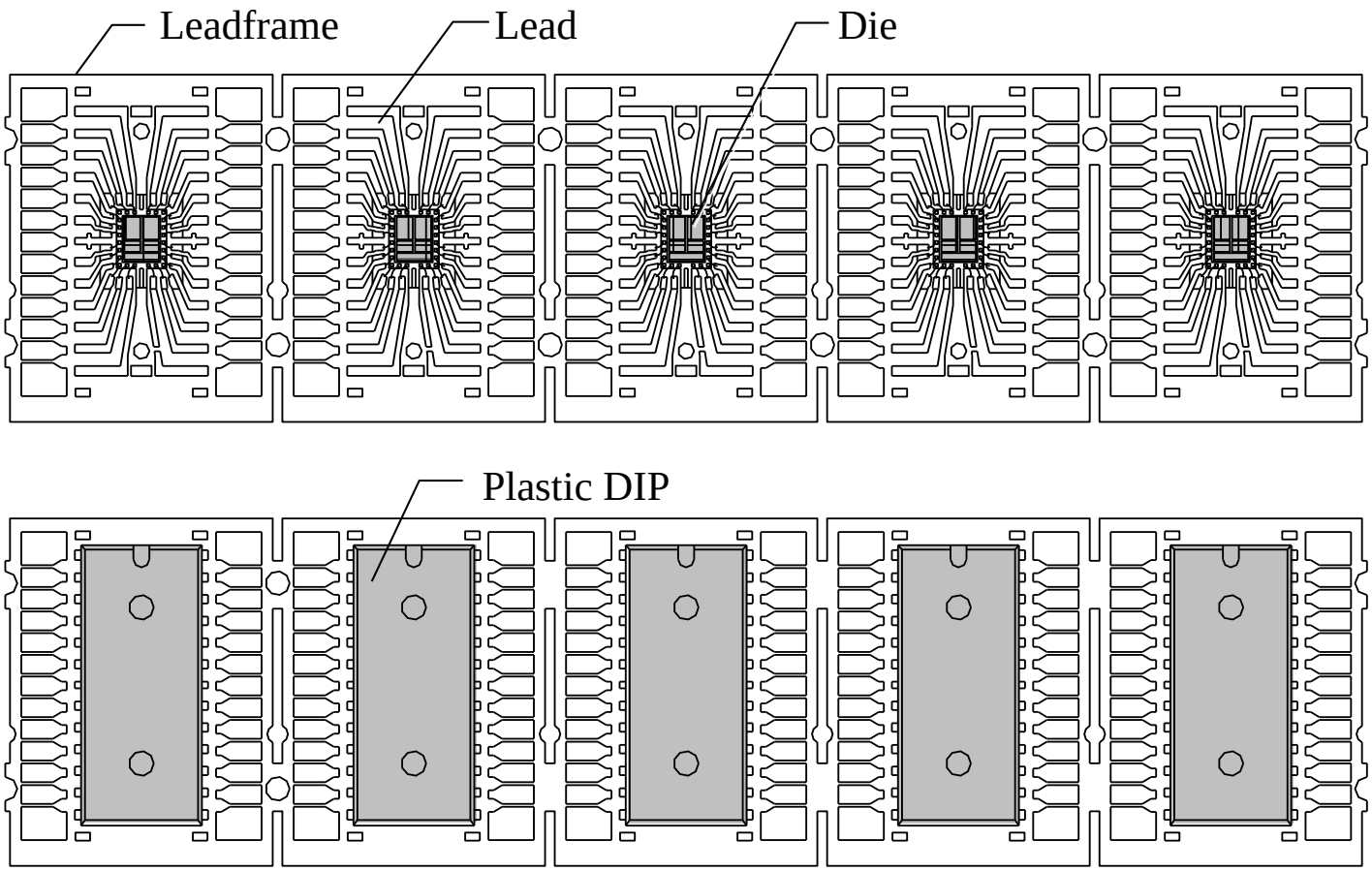
Schematic of the Backgrind Process



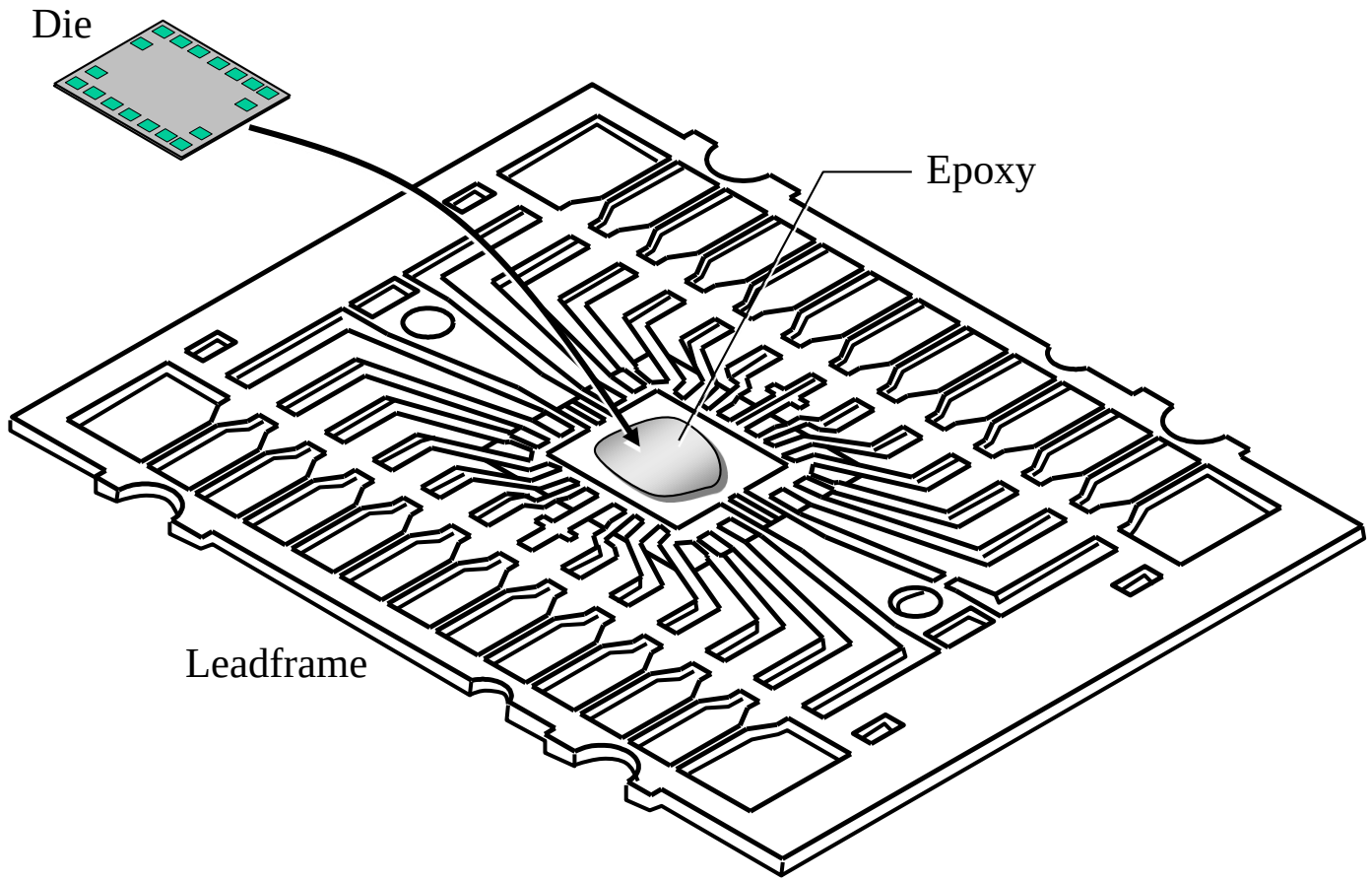
Wafer Saw and Sliced Wafer



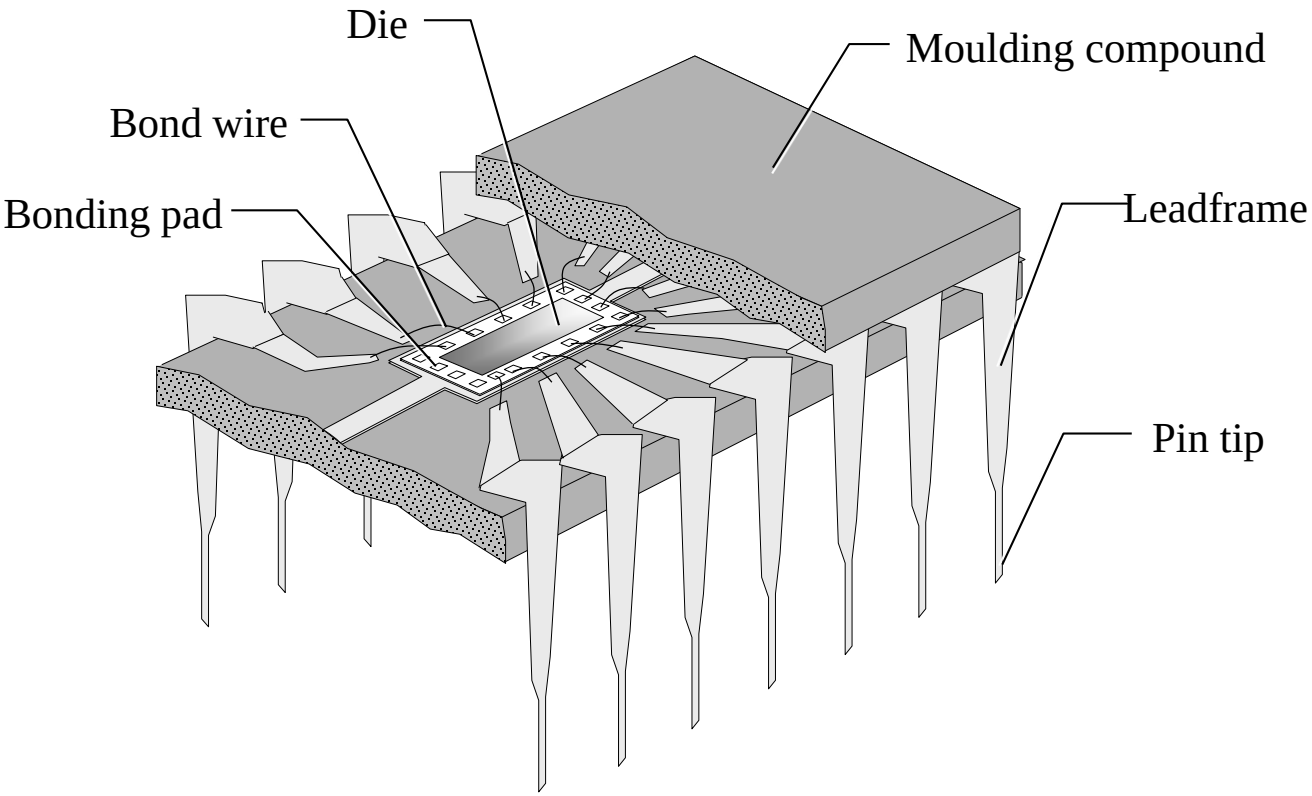
Typical Leadframe for Die Attach



Epoxy Die Attach



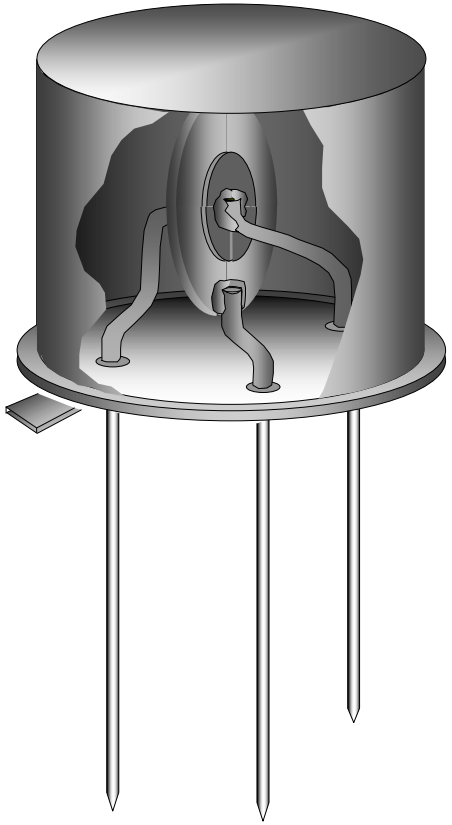
Wires Bonded from Chip Bonding Pads to Leadframe



Wirebonding Chip to Leadframe

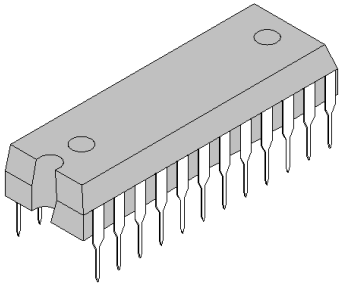
Traditional Packaging

- Plastic Packaging
- Ceramic Packaging
- TO-Style Metal Package(old)

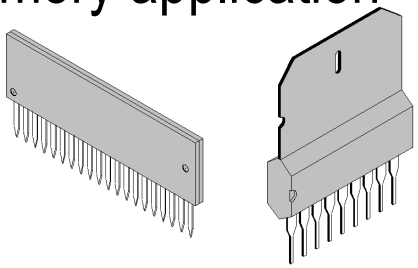


General package mode

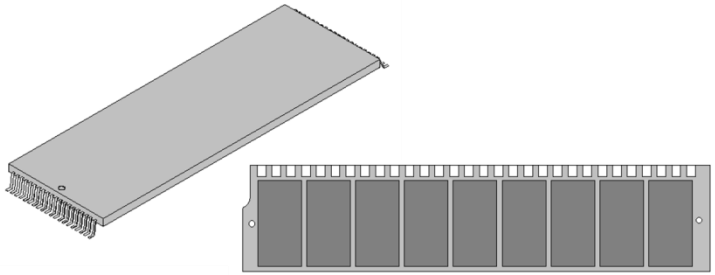
Plastic Dual In-Line Package (DIP) for Pin-In-Hole (PIH)1970s-1980s



Single In-Line Package (SIP), decreasing capacity and cost Memory application

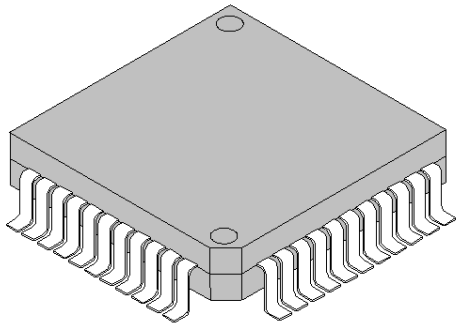


Thin Small Outline Package (TSOP) Memory and smartcard Single In-Line Memory Module (SIMM)

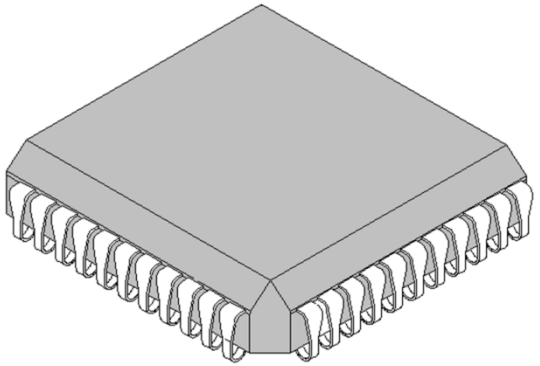


General package mode

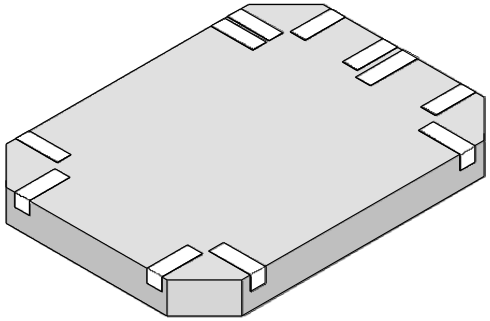
Quad Flatpack (QFP) with Gull Wing Surface Mount Leads



Plastic Leaded Chip Carrier (PLCC) with J-Leads for Surface Mount

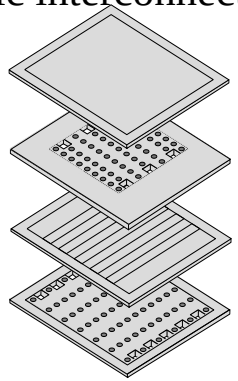


Leadless Chip Carrier (LCC)

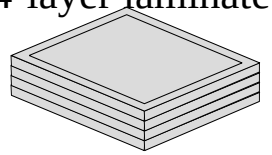


Laminated Refractory Ceramic Process Sequence

Ceramic interconnect layers

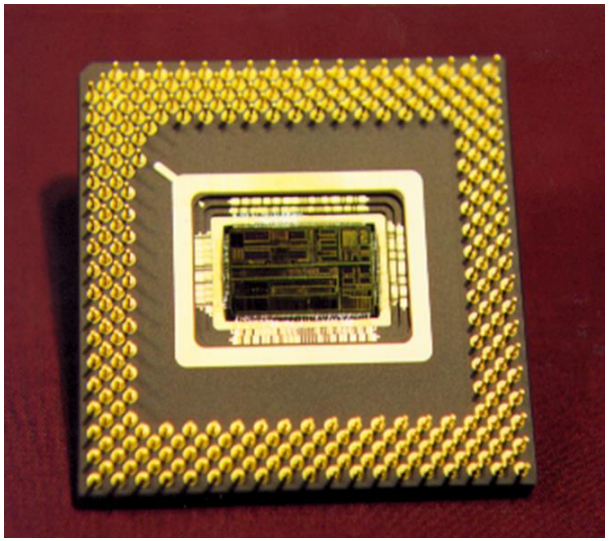


4-layer laminate



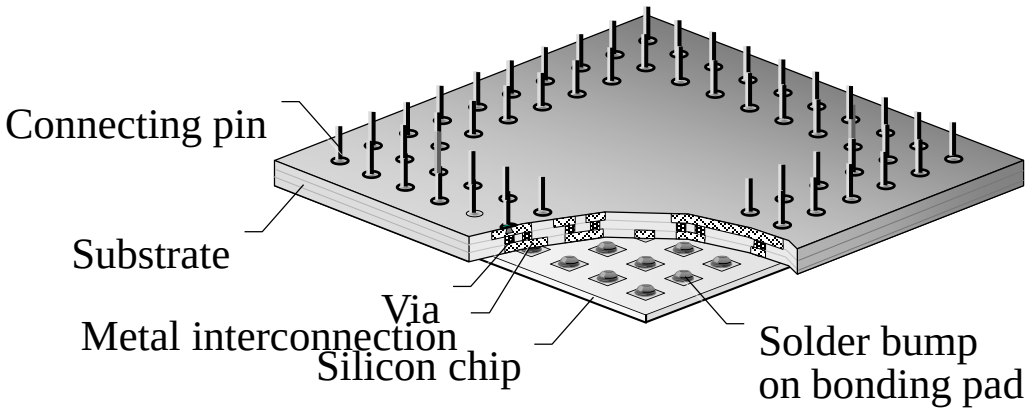
Advanced Packaging

- Flip chip
- Ball grid array (BGA)
- Chip on board (COB)
- Tape automated bonding (TAB)
- Multichip modules (MCM)
- Chip scale packaging (CSP)
- Wafer-level packaging

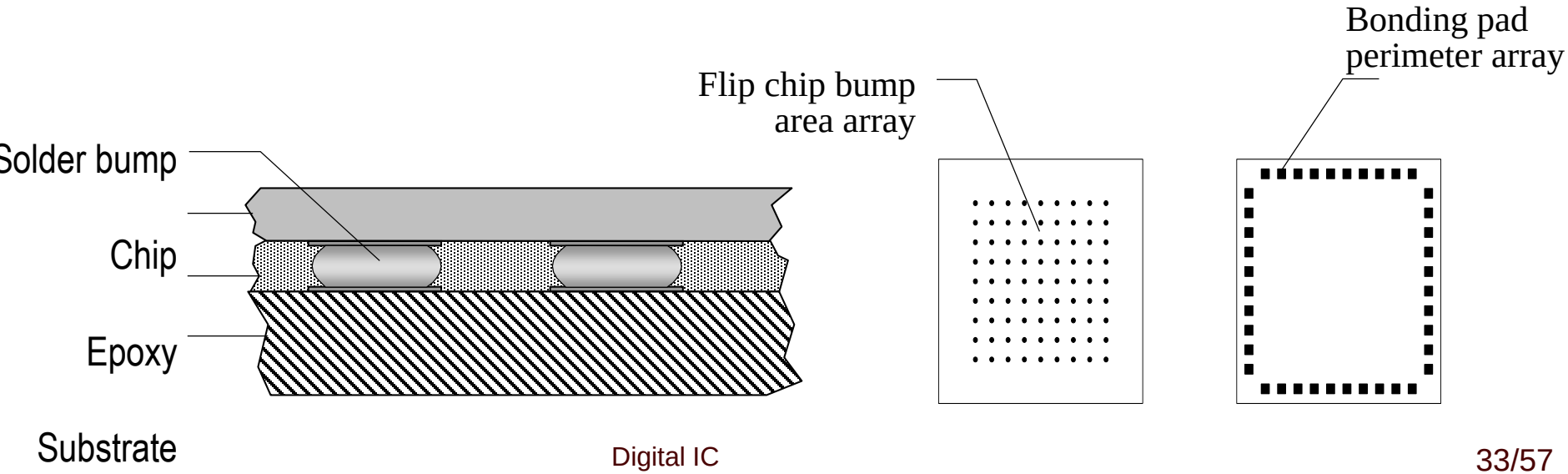


Advanced Packaging

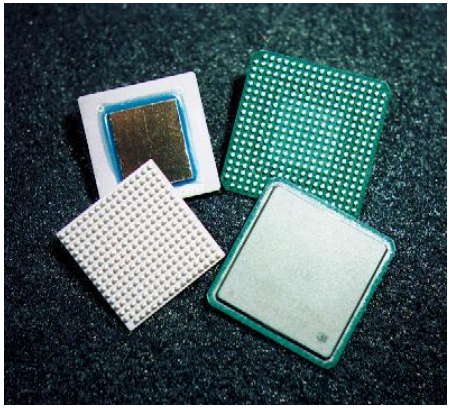
Flip Chip Package

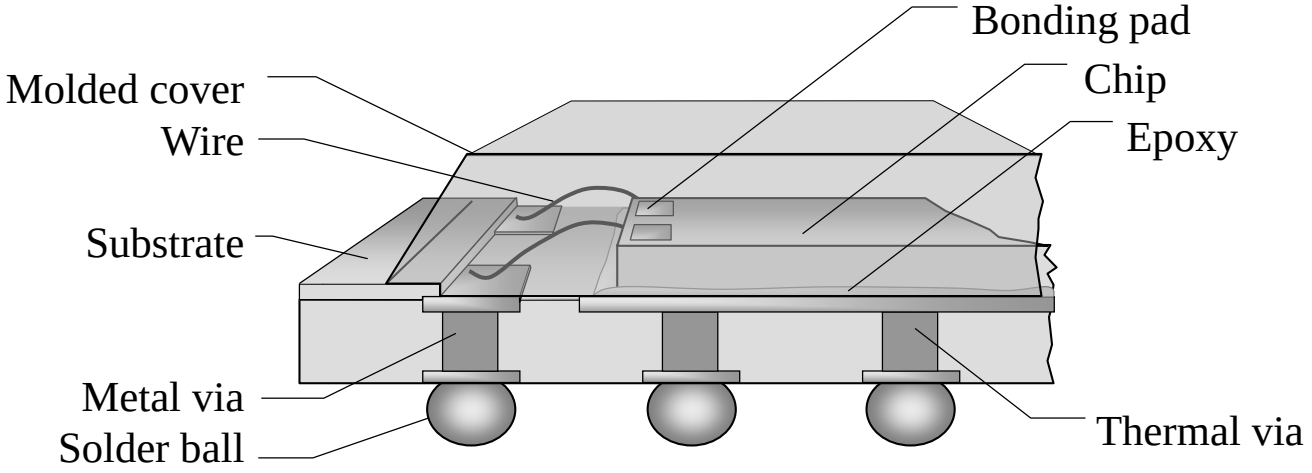


Flip Chip Area Array Solder Bumps Versus Wirebond



Ball Grid Array





Multichip Module (MCM)