Algorithm for Dramatically Improved Efficiency in ADC Linearity Test

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Abstract

For high performance analog and mixed-signal products, production test is a significant contributor to the recurring manufacturing cost. For high resolution ADCs, the cost of build can be dominated by test cost, of which linearity test cost is often the largest component. This paper introduces a new algorithm that dramatically reduces ADC linearity test cost. The algorithm takes a system identification approach using a segmented non-parametric model that captures both linear errors (mismatches, etc.) and truly nonlinear errors (voltage coefficients, etc.). By avoiding the gross inefficiencies inherent in conventional linearity test solutions, the new algorithm is able to reduce the required test data by a factor of over 100. The algorithm works for various types of ADCs, including SARs and pipelines. Simulation results and measurements against the gold standard servo-loop test validate the accuracy of the new solution. Results from multiple case studies involving both good and poor ADCs demonstrate that the new method achieved several times better precision than standard histogram test, while using two orders of magnitude less test data and hence test time.

1. Introduction

The analog-to-digital converter (ADC) is one of the world's largest volume mixed-signal products [1] and accurate testing of high performance ADCs is a well-known important and challenging problem facing the semiconductor industry. A large number of ADC specifications must be tested before the ADC can be passed to the customer. Two groups of specifications impose most of the test challenges. One group is related to the ADC's transfer curve including integral nonlinearity (INL), differential nonlinearity (DNL), offset, and gain error. The other is related to the ADC's spectral performance including total harmonic distortion (THD), spurious free dynamic range (SFDR), signal to noise ratio (SNR), and so on. Linearity test is conventionally tested by the histogram method using either a pure sine wave or a very linear triangular wave as stimulus; whereas spectral performance is tested by the fast Fourier transform (FFT) method using a pure sine wave as input [2].

The challenges and cost in accurate ADC test come from three requirements: 1) fast data capture; 2) precision clock timing; and 3) linear stimulus generation [3]. Many researchers have proposed various techniques to address various aspects of these challenges. In [4-6], new histogram based linearity test algorithms were introduced that dramatically relaxed the linearity requirement for stimulus generation so that 7 or 8 bit linear ramp signals can be used to test high resolution ADCs, achieving test accuracy beyond 16 bits. In [7, 8], computationally efficient algorithms were introduced to relax one of the most stringent precision clock timing requirements: coherent sampling. Both stimulus generation and precision clock timing are requirements on the test equipment or the test interface design. They impose challenges and capital cost at the time of test solution development. Fortunately, this is a one-time cost and can be amortized over all the parts to be tested by the same tester throughout the years. However, test cost associated with data acquisition is recurring for each device manufactured. Therefore test cost due to data acquisition time on the tester is the dominant part of the overall test cost.

Many researchers have proposed methodologies to reduce ADC test time. Adamo, Attivissimo, *et al.* proposed methods to approximately estimate the low frequency contents of an ADC's integral nonlinearity (INL) [9, 10]. Crus Serra, *et al.* attempted to combine large signal spectral testing and small signal ramp test to achieve overall linearity test results [11]. Yu, *et al.* introduced a system identification approach to identify the parameters in a pipeline ADC and then reconstruct the full code linearity information [12]. In [13, 14], the authors incorporated Kalman filtering in the standard histogram method and developed new ADC linearity test algorithms that can reduce the data acquisition time by several times. In [15], Kook, *et al*, attempted to use polynomial fitting and segmented measurements to test high resolution ADCs with low resolution DACs as excitation sources. All of these efforts and similar ones in the literature attempt to reduce linearity test time by limiting the test algorithm's applicability or by sacrificing some aspects of test accuracy. In [16, 17], the authors introduced a new method for testing the ADC's low frequency spectral performance from available linearity test results. This method offers cost savings associated with the data acquisition time for spectral testing without sacrificing test accuracy. In [18], Goyal, *et al,* presented a select code testing method to reduce the test time of SAR ADCs. In [19], design for test (DfT) circuits and modified adaptation algorithms are introduced to reduce the test time associated with calibrating the linear errors in Pipeline ADCs. In [20], Uemori, *et al,* used multi-tone sine wave to reduce the sine histogram test time to close to ramp histogram test time.

In this paper, a new algorithm is introduced for accurate linearity test with dramatically reduced data acquisition. The new method exploits the fact that the number of truly independent error sources contributing to linearity errors is dramatically smaller than the number of code bins to be tested in high resolution ADCs. It also removes the gross noise averaging inefficiency in histogram test in which

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only samples near a particular transition voltage actually contribute to noise averaging for that transition voltage. In the proposed method, all samples on a large segment of the transfer curve contribute to noise averaging. This actually increases the effective number of noise averaging samples by a large factor, even though the total number of samples is reduced by a factor of up to 100s. This effective noise averaging is made possible by creative utilization of the highly accurate input signal, which is disregarded in the conventional test solutions. The knowledge of the input and the fact that the ADC under test is approximately linear allow us to shift many samples to a location where critical estimates need to be made. These three new techniques empower the new algorithm to achieve sufficient test accuracy, enhance measurement precision, and greatly reduce test time and test cost.

The new method is qualitatively different from all existing reduced time test strategies in that accurate INL/DNL test at each and every code is the target. Measurement results for 16 bit SAR ADCs demonstrate that the INL/DNL tested by the new method with 1/4 hit per code on average agrees remarkably well with INL/DNL tested by the gold standard servo loop test, at all 65K code locations.

2. New Algorithm for Efficient ADC Linearity Test

ADC linearity test involves testing possible errors in the ADC's input output transfer curve. Offset and gain errors can be tested quickly without much difficulty. However, full code linearity test requires testing of all transition voltages and the differential nonlinearity (DNL) and integral nonlinearity (INL) associated with these transition voltages. The most prevalent production test method for ADC linearity test is the standard histogram test, using either a sine wave input that has at least 10 times smaller distortion, or a linear ramp input that is at least 10 times more linear, than the ADC under test. Around the order of 100 samples are typically used per ADC output code in order for the histogram method to average down the effect of noise inherently present in any ADC. To achieve the same worst case samples per code, the sine histogram test (SHT) would require $\pi/2$ times the total samples needed by the ramp histogram test (RHT), or about 57% more test data. On the flip side, a sine wave with sufficient purity is significantly easier to generate than a ramp signal with sufficient linearity. Hence, both methods are widely used.

As the resolution of the ADC grows, the number of output codes and therefore the number of INL/DNL to be tested grows exponentially. An n-bit ADC has 2^n output codes, $2^n - 1$ transition voltages, $2^n - 1$ INLs, and $2^n - 2$ DNLs to be tested. If H samples per code is needed for noise averaging, $H*2^n$ samples will be needed in RHT and an additional 57% more needed in SHT. For a 16 bit ADC, with H=64, this would lead to over 4 million samples for RHT and well over 6 million samples for SHT. If the ADC has a sampling rate of 200 KSPS, the data acquisition time alone would be over 20 or 30 seconds long. With multi-site (quad for example) testing, the effective test time will be in the 5 to 9 seconds range. This corresponds to a significant test cost. For slower ADCs, the linearity test time is even worse. Clearly, the number of samples required directly translates into test time which directly translates into test cost. The goal is then to dramatically reduce the number of samples needed for full code linearity test.

Unlike flash ADCs, high resolution ADCs always use architectures for which the number of ADC output codes is orders of magnitude more than the number of analog components used to build the ADC. Cyclic, SAR, two step, pipeline, and sigma delta ADCs are examples of such architectures. For example, a 16 bit SAR ADC has well over 65K output codes and therefore has over 65K INL/DNL's that need to be tested. However, a 16 bit capacitor array based SAR ADC has one comparator, one sample and hold, less than 20 capacitors, and less than 20 switches as its main analog circuit components. The non-idealities (mismatches, voltage coefficients, etc) of these components completely determine all the errors in the input output transfer curve of the ADC. In another word, all the 65K INL/DNL errors are highly correlated and they are all deterministic functions of a much smaller number (less than 100) of independent errors (component size errors, parasitics, voltage coefficients, etc). If the ADC is fully differential, the number of analog components will about double, but the number of independent error sources remains small.

The correlated nature of the INL/DNL errors begs for a model based approach to ADC linearity testing. There have been many attempts at constructing behavioral models of a given architecture with linear and nonlinear relationships based on circuit laws for the purpose of ADC linearity testing. But none of these attempts have led to solutions with acceptable test accuracy, including some of the authors' earlier work. There is an intrinsic reason why these approaches will not work. For any "model-able" error source, a good designer will find a circuit modification, or a calibration, to take that error out. As a result, in a well-designed ADC, all the model-able error sources have been reduced to very low levels. But these small errors and the various secondary error sources still combine to cause INL/DNL errors at levels that would cause ADC rejection at production test. Hence, the true need for production test is to catch these un-model-able errors. Therefore, any model based approach relying on circuit laws is fundamentally limited to only being able to catch large model-able errors and cannot be used as a replacement for production test of well-designed parts.

The proposed algorithm takes a fundamentally different approach. It does not use any circuit model and hardly use any information about the ADC architecture. It takes a perspective from production test, uses a black-box input-output approach, and models the ADC's INL curve with a "segmented non-parametric" model. The segmented non-parametric model will be explained in the next paragraph.

Input output data from the ADC will be used to identify this model. This can be done with dramatically smaller number of samples than typically used in RHT or SHT. Once the model is identified, full code INL/DNL can be computed from the model.

The segmented non-parametric model is explained with the help of figure 1, which contains a zoomed-in portion of an ADC's INL curve. The axes are intentionally not shown since the actual values are of no concern and may even be distracting. Nevertheless, the ADC's output code goes up along the horizontal and the vertical levels reflect the INL values at each code. The red dots are points on the true INL curve of the ADC. The blue dots are points on the tested INL curve using a standard histogram test with a certain amount of input referred noise. The INL curve is broken into many MSB segments according to the MSB (most significant bits) value of the ADC output code. Within each MSB segment, the MSB code does not change. The average value of each MSB segment is marked by the pink horizontal line's level and is denoted by $E(C_{MSB})$, where C_{MSB} is the MSB code value in the MSB segment. For example, for a 16 bit ADC, the whole INL curve may be broken into 64 MSB segments according to the values of the 6 MSB bits. Each segment is then numbered from C_{MSB} = 0, 1, …, 63. This leads to 64 error terms in the segmented non-parametric model of the INL curve E(0), E(1), …, E(63). Of course, the INL curve may be broken into different numbers of segments, such as, 32 segments or 128 segments.

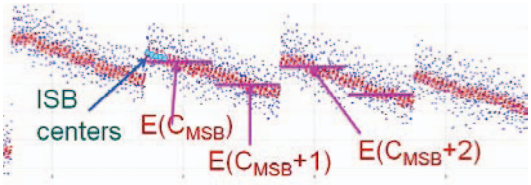

Figure 1 Segmented non-parametric model of ADC INL

It is important to point out that absolutely no assumptions have been made on the ADC. Everything is based on what production test would see. The E(i)'s are allowed to be completely independent of each other, or correlated with each other. They may be due to linear errors (such as mismatch and insufficient gain) or due to nonlinear errors (such as voltage coefficients or code dependent parasitics) or due to a combination of multiple secondary errors. These E(i)'s will be treated like errors in flash ADCs. Any noticeable nonlinear shapes of the ADC INL curve will be captured by these E(i)'s.

Each MSB segment only contains a small portion of the INL curve and no MSB bit will make a transition within any given segment. Suppose the ADC's architecture is such that regardless of which MSB segment, all the lower bits after the MSB bits are converted by the same lower bit ADC. This is the case for all ADC architectures except for a flash ADC. For sigma delta ADCs, the feedback nature makes the lower bits possibly dependent on the MSB values. With this assumption, the proposed algorithm applied to all types of ADCs other than high resolution flash and sigma delta ADCs. Since no one ever builds a high resolution flash ADC and sigma delta ADCs are typically assumed to be linear and not tested for full code INL/DNL, the new algorithm does not impose practical limitations. (In fact, we have run simulation with simulated high resolution flash ADCs and the algorithm works well.)

With the above assumption, the ADC INL curve has a segmented structure. Since each and every MSB segment is the INL curve of the lower bit ADC after the MSB, every segment should have the same shape, nominally. If the ADC's nonlinearity spreads to the lower bit ADC level, each segment's shape may slightly change according to the MSB values. Nevertheless, this nonlinear shape change will be very small, as long as the ADC is approximately linear and is worthy of testing. (This is the second time the "approximately linear" assumption is made. As will be seen from the algorithm, we do have a step to detect if the ADC is "approximately linear" and decide if further test is warranted.) With this, each MSB segment is modeled with the same inner structure, but allowing certain mechanisms to capture the slight gradual shape change from segment to segment.

The inner structure of an MSB segment can be modeled with the same segmented nonparametric model approach. In this manner, an MSB segment is further broken into ISB segments with "I" standing for intermediate. In doing so, we have introduced more error terms in the overall segmented nonparametric model: the average deviations of the ISB segments away from the MSB segment average. Again, these ISB deviations are allowed to have slight gradual changes among different MSB segments.

Although further breaking down may be carried out, our experience indicates that two levels of segmentation are sufficient. If we stop at ISB segmentation, the variations within each ISB segment away from the ISB average values are captured by the LSB code bin width errors (WE). With these, we can then write:

$$INL(C) = E(C_{MSB}) + E_{C_{MSB}}(C_{ISB}) + WE(C_{LSB}).$$

With the above model, it is theoretically possible to test all code bin errors by first identifying all the independent error terms in the model and then using the model to compute the full code INL/DNL. In the ideal noise free case, this can be done using only as many input output samples as the number of error terms in the model, which, for 14, 16, and 18 bit ADCs, is in the 100 to 200 range depending on how the segmentation is done and how much ISB nonlinearity is allowed. In actual testing, noise is inevitable and several 100 times more data will be used to average out the noise.

Just because it is mathematically possible, it does not mean that a practical solution to identify the model can be easily developed or is even possible. First of all, before the ADC

is accurately tested, we do not have true values of INL(C) to plug into the model to identify the E's. Next, during test, we can observe the output code C but we don't know the input value. Thirdly, if we use a smaller number of samples than the number of ADC codes, all the samples are spread around, and therefore no naturally "repeated" measurements of a quantity would be available for noise averaging.

To find solutions to these issues, let us examine the conventional histogram test, reveal its inefficiencies, and use that to motivate new ideas. In Figure 2 below, the conventional histogram test is illustrated. A signal source at least 10 times more accurate than the ADC under test is used to generate the stimulus signal for the ADC. For each sampling time t, the ADC generates an output code C(t) corresponding to the input signal f(t). A total of $H*2^n$ samples will be generated, but immediately these codes will be sorted into 2^n histogram bins. The count value will be kept but the instantaneous values of t, C(t) and f(t) are discarded. These bin counts will be further processed to generate the INL/DNL information.

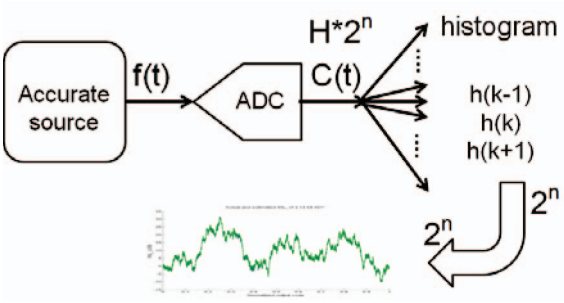

Figure 2 Conventional histogram test of ADC

Clearly, the most accurate quantity in the above set up is the stimulus signal f(t). However, the histogram test algorithm only uses the bin counts and totally disregards the most accurate information available. Also the histogram count in one bin only is used to estimate the DNL for that bin, and provides no help in estimating other quantities. Hence the noise averaging capability of these samples is grossly underutilized.

The first thing we would like to do better is to make use of the accurate input signal. If somehow we can find out the expected output code of a linear ADC that shares the same endpoint fit line as the ADC under test, then this expected linear code can be subtracted from the actual ADC output code to generate an error signal. This can be done for each and every ADC output sample. The error signal reflects the total error made by the ADC due to nonlinearity, noise, and quantization. By doing so we achieve another great benefit: for all those input signal samples that are spread around in one MSB segment, that is, samples sharing the same MSB code but with different lower codes, the process of subtracting the expected linear codes effectively moves them to be all closely scatter around $E(C_{MSB})$. This gives us a great boost in noise averaging capability.

In terms of input output relationships, we can write:

$$C_{exp} - C + noise = E(C_{MSB}) + E_{CMSB}(C_{ISB}) + WE(C_{LSB}).$$

where C_{exp} is the expected output code from a linear ADC with the same endpoint fit line as the ADC under test. These equations can then be used with any identification algorithm in order to estimate the error terms in our segmented nonparametric model. The optimization criteria for the identification algorithm is that the mismatch between the INL(k) predicted by the segmented model at those codes that appear at the actual ADC output and the ADC output error generated by subtracting the expected linear code from the actual code is minimized in some reasonable sense. One possible choice would be the total sum of mismatch squares. The block diagram of the new algorithm is illustrated in Figure 3.

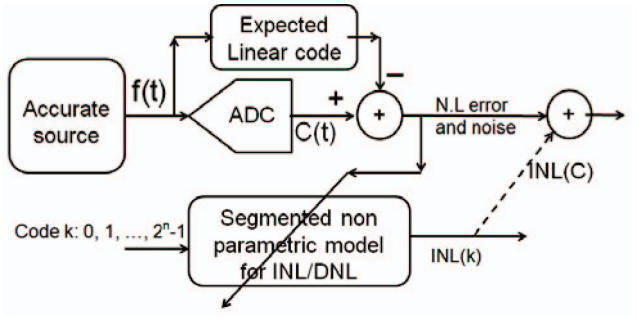

Figure 3 Block diagram of the proposed algorithm for dramatically more efficient ADC linearity test

There is one more unresolved issue: how to generate the expected output code for an input sample that would be produced by a linear ADC sharing the same endpoint fit line as the ADC under test? This turns out to be not so difficult. Suppose we are using a pure sine wave as input for testing. A linear ADC would produce an output code sequence that has no harmonic distortion at all. If this linear ADC shares the same endpoint fit line as the ADC under test, the two ADC's output will have the same offset and the same fundamental component. For an ideal linear ADC, we will let it have no quantization error and no input referred noise. Based on this observation, we can take the actual ADC's output sequence, perform Fourier transform on it (via FFT), extract the DC and fundamental components, and construct the time domain codes. These will be used as the expected linear codes in figure 3.

At this point we can finally summarize the proposed algorithm for ADC linearity test as a flow chart given in figure 4. For computational efficiency of the FFT algorithm, we will always use a power of 2 samples. To ensure that FFT will generate the spectrum accurately without spectral leakage, we will make sure coherent sampling is appropriately maintained.

An important technical detail is to make sure that we only attempt to perform linearity test on "approximately linear" ADCs. This is done by checking the total power of the

error signal after subtracting the expected linear code from the actual ADC output code. If the total error power is significantly worse than the expected total distortion plus noise power, the ADC is very poor and does not warrant further testing. If the error power is at reasonable levels, then we have an "approximately linear" ADC.

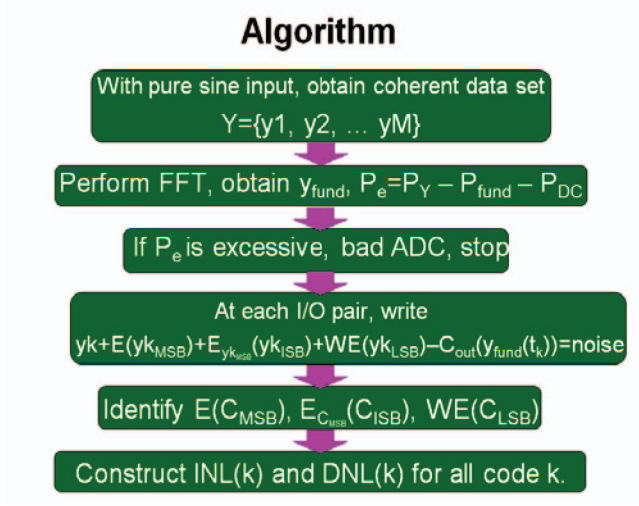

Figure 4 Flow chart of the proposed ADC test algorithm

As can be seen, the total number of samples taken is M which could be significantly smaller than $H*2^n$ and may be even less than 2^n. To find out how small M can be, we need to find out how many terms need to be identified in the segmented nonparametric model. If we count the number of $E(C_{MSB})$'s, $E_{C_{MSB}}(C_{ISB})$'s, and $WE(C_{LSB})$'s for 14 to 18 bit ADCs, the total number K of error terms will come out to be in the 100 to 200 range depending on how the segmentation is done. Without going into details, one can estimate that test uncertainty will have variance given by $Var_{new} = \pi * K * \sigma^2 / 2M$, where σ^2 is the total noise variance in the test system including noise from the source, ADC thermal noise, and quantization noise. The value of σ^2 can be easily computed in the second box in the algorithm flow chart. For example, to drive the noise rms value down by a factor of 8, the total number of samples must satisfy $M > 32\pi*K$. The right hand side is in the 10000 to 20000 range for 14 to 18 bit ADCs. To be safe, we recommend at least double or triple this number. For comparison, the sine histogram test with $H*2^n$ samples will have a test result uncertainty variance given by $Var_{SHT} = \pi * \sigma^2 / 2H$. The ratio of variance improvement is then $Var_{SHT}/Var_{new} = M/KH$. For example, if the new method uses M=2^16 samples with K=160 error terms, and the standard method uses H=64 hits/code with a total of 64*2^16 samples, the variance ratio will be M/KH = 32/5, meaning the test result noise band will be reduced by 2.5 times in the new method. This will be validated by measurement results.

3. Simulation Results

To demonstrate the validity of the proposed method for ADC linearity test, we will present both simulation results and measurement results. Simulation offers a distinctive advantage over measurement in one important aspect: the true INL of an ADC is precisely known in simulation so that the tested INL curves from various methods can be compared with the true INL to obtain test errors.

Extensive simulation studies have been conducted with various ADC architectures, various resolution levels, and various linearity levels. SAR and pipeline ADCs are studied the most since they are the most widely used. SARs are particularly emphasized because of their low power advantage and because of the larger test cost savings since they are much slower than pipeline ADCs. We have also simulated high resolution flash ADCs even though they are not practical. The proposed algorithm worked well with all of these architectures.

Due to space limitation, we will only include some simulation results for a 16 bit two step ADC with a (6 bit, 10 bit) segmentation. Each step is modeled as a flash ADC with string DAC reference whose resistor values are randomly generated. Once the ADC is generated, each and every code transition voltage is found using binary search, similar to the standard servo loop method. From the true transition voltages, the true INL/DNL can be computed.

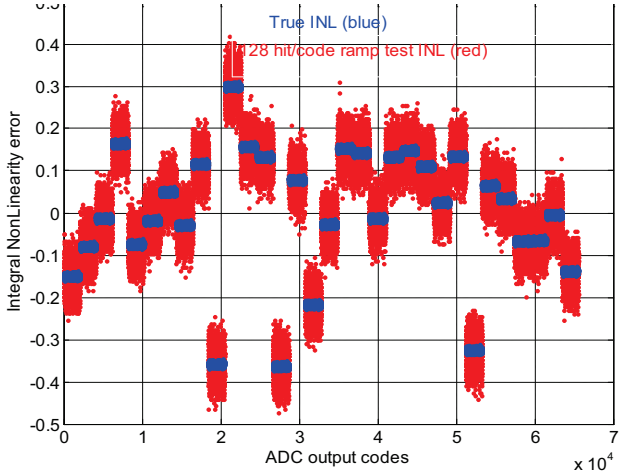

Figure 5 Simulation results comparing the true INL of a 16 bit 2-step ADC against tested INL by the standard ramp histogram test with 128 hits/code and input noise rms value of 0.25 LSB

First, the ADC linearity is tested using the standard histogram method with a perfectly linear slow ramp input taking 128 samples per code. Input referred additive Gaussian noise was added to the ramp signal with a noise rms value of 0.25 LSB. This is in addition to quantization noise. Standard histogram method was used to process the ADC output data to compute the tested INL. Figure 5 shows the results. The blue dots show the true INL errors at each ADC output code, and the red dots show the RHT tested INL errors at the corresponding ADC output code. Note that the maximum difference over 65K codes is about

0.15 LSB. This agrees with the theoretical prediction based on the noise magnitude and the hits per code being used.

Next, the ADC linearity is tested again using the proposed method. In this case, a sinusoidal stimulus is applied to the ADC input. The signal frequency is about 1/10 of the Nyquist frequency of the ADC. An additive Gaussian noise with rms value of 0.25 LSB is also added to the sinusoidal signal. The signal frequency is selected so that coherent sampling is maintained. The sine wave amplitude is slightly less than half of the ADC input range to avoiding clipping, even in the presence of noise.

The proposed method is applied to process the ADC output data. In this example, we used only one time segmentation in the segmented nonparametric model. Hence, we only have MSB segments. Within each MSB segment, all the inner variations are attributed to the LSB. The INL model used in the test algorithm does not know anything about the architecture of the ADC under test. To minimize the number of error terms to be identified, an (8 bit, 8 bit) segmentation is used in the INL model. Notice that this is different from the actual ADC architecture which has a (6 bit, 10 bit) MSB/LSB segmentation. Since we assume that no truly nonlinear error will exist beyond the first 8 MSB, we did not use any terms to account for gradual nonlinear shape changes from segment to segment. As a result, we have 2^8 error terms for the MSB and 2^8 error terms for the LSB, giving a total number of independent error terms K = 2^8 + 2^8 = 512. To achieve the same level of noise averaging effect as the ramp histogram test on the previous page, we should use a total number of samples M = KH = 512 * 128 = 2^16, giving an average of 1 sample per code. But since sine wave input is used in the new method, the effective number of samples is reduced by a factor of $\pi/2$. Based on our theory, the INL test results will have an noise error band around the true INL that is about $(\pi/2)^{0.5}$ = 1.25 times of the noise band seen in figure 5.

The results of the new algorithm are shown in Figure 6. Again the blue dots are the true INL errors and the red dots are the INL values tested by the proposed method. Comparing the results in Figure 5 and Figure 6, we observe that the INL test errors in both methods are at very similar levels. The noise band in figure 6 is indeed slightly larger than that in figure 5, confirming the correct theoretical prediction of the noise averaging capability of the new algorithm. Notice also that in both figure 5 and figure 6, the tested results (the red dots) are crowded around the blue dots, establishing the test accuracy of both the standard histogram test and the proposed test.

To summarize, simulation results have demonstrated that for a 16 bit ADC, the proposed method achieved the same linearity test accuracy as that by the standard ramp histogram method. Similar levels of measurement precision are achieved but the new method used only less than 1% of test data, and hence less than 1% of test time. These results agree extremely well with the theoretical prediction. Since test cost is dominantly due to test time, the proposed method can potentially reduce ADC linearity test cost by a factor more than 100 times.

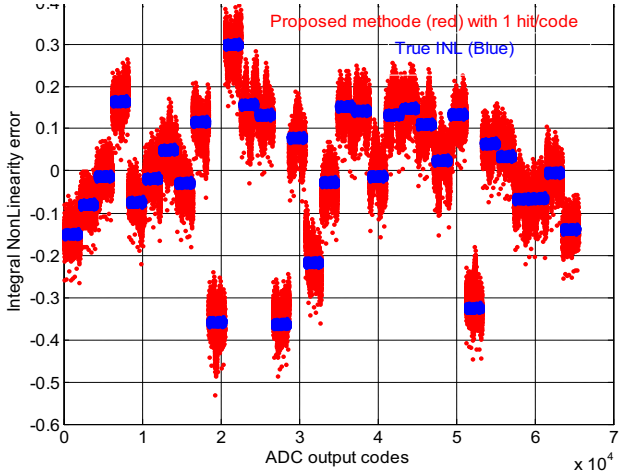

Figure 6 Simulation results comparing the true INL of a 16 bit 2-step ADC against tested INL by the proposed method with an average of only 1 hit/code and input noise rms value of 0.25 LSB

4. Measurement Results

In this section we will present several case studies to further validate the proposed method for accurate ADC linearity testing with greatly reduced test cost. To eliminate any possible concerns about the integrity of, or bias in, the measurement results, measurement data were taken by independent third parties in industry laboratories. We asked our contacts to test a few ADCs with industry standard methods. Both linearity test and spectral performance test were performed. No request regarding the resolution of the ADCs or the type of the ADCs was made. The only preference conveyed was that a mixture of both good and bad ADCs be measured. Raw data from spectral testing were fed to the proposed algorithm. The algorithm did not know the resolution or architecture of the ADCs being tested. Full code INL/DNL test were conducted by using the proposed method and using only the available raw data from spectral test. The tested INL/DNL using the proposed method is then compared against the tested INL/DNL using industry standard method. Due to space limitation, we will only provide measurement results for a few 16 bit SAR ADCs.

In our segmented nonparametric model for the INL curve, we used two time segmentation, with MSB, ISB and LSB groups of codes. We have experimented with various segmentations such as 6-5-5, 6-6-4, 6-4-6, 5-6-5, 7-5-4, etc, with some additional terms accounting for the ISB shape change due to slight nonlinearity in the ISB. In all of these cases, the new INL test method worked about equally well. The total number of terms to be identified is about 160. Based on our theory, this should allow us to further reduce the total number of samples as compared to what was used in simulation in the last section. This will

be verified by the measurement results, but we will do the reduction gradually, staring from 65K samples, to 32K samples, and to 16K samples.

In the first case study, a good 16 bit SAR ADC was used. We compare the INL test results from the new algorithm against those from ramp histogram test. The RHT was carried out on a mixed-signal ATE equipped with 20 bit linear DACs to generate linear triangular wave stimulus signals. 64 hits per code were used, requiring a total of 4.2 million samples. With a sampling rate of 250 KSPS, this corresponds to 16.8 seconds of data acquisition time for the RHT. The RHT tested INL values are represented by the blue dots in Figure 7.

From the spectral test results, the total input referred noise has an rms value of about 0.65 LSB. With 64 hits per code, the RHT INL test results have a measurement uncertainty with rms value of 0.08 LSB, giving a 3 sigma noise band of +– 1/4 LSB.

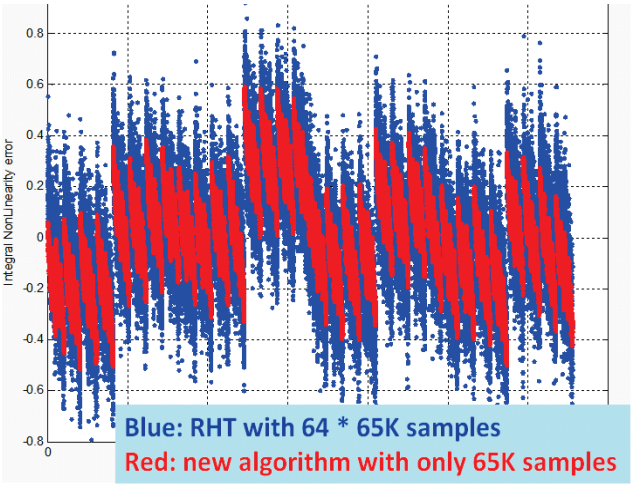

Figure 7. Measurement results comparing the INL of a 16 bit SAR ADC by the ramp histogram method with 64 hits/code against INL by the proposed method using an average of 1 hit/code. True INL is unknown and input referred noise rms is 0.65 LSB.

For comparison, the proposed INL test algorithm is applied to a set of ADC output data coherently sampled from a pure sine wave input with peak to peak values slightly less than the ADC's full input range. A total of 2^16, or 65K, samples were used. After running the new algorithm, the tested INL values were plotted in the same graph in figure 7 as the red dots. Notice how the red curve lies right near the center of the blue curve's noise band. This is a clear indication that both results have the same accuracy, but the red has better precision. From the example numbers used at the end of section two, the test results from the new algorithm has a measurement uncertainty of rms value of 0.03 LSB and a 3 sigma noise band of +– 0.1 LSB. A visual inspection of figure 7 provides a quick confirmation of the theoretical prediction.

As a second case study, a marginally good 16 bit SAR ADC was used. In this case, we compare against sine wave histogram test. The standard linearity test was carried out with 128 samples per code using a total of 2^23 samples. Standard spectral testing was also carried out with 2^15 samples, averaging 0.5 sample per code, with coherent sampling. Since in the ideal coherent sine wave testing, if a code is hit, it will be hit twice, the total data collection of 2^15 samples will only hit fewer than 1/4 of the ADC output codes. Nevertheless, these samples are sufficient for the proposed new algorithm to provide an accurate test of the entire ADC output codes.

The 2^15 raw samples of the ADC output from spectral testing was fed to the proposed algorithm. Both spectral performance and linearity performance were tested in the new algorithm. The total effective input noise, including quantization noise, was determined to have an rms value of 0.63 LSB. The input sine signal's amplitude, frequency, initial phase, and offset were accurately computed. This information was used to determine the expected output value from a linear ADC. The difference between the actual output codes and the expected linear output codes are processed by the new algorithm with the tested INL values shown as the red scatter plot in Figure 8 below.

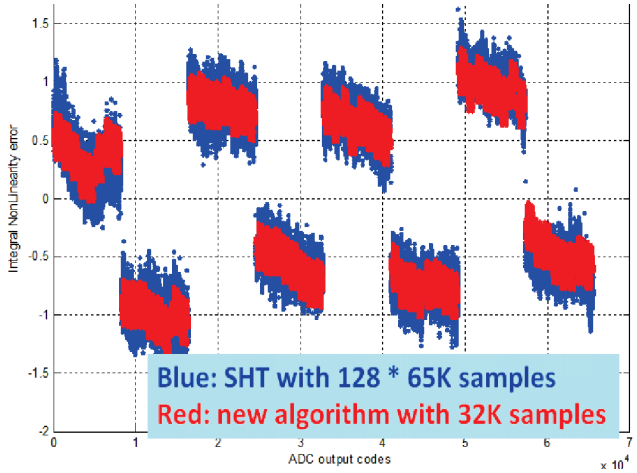

Figure 8 Measurement results comparing the INL of a 16 bit SAR ADC by the standard histogram method with 128 hits/code against INL by the proposed method using spectral test data that has about 0.5 hit/code. True INL is unknown and input referred noise is unknown

For comparison, the tested INL of the same ADC using SHT was also plotted in the same figure as the blue scatter plot. Notice that the SHT used 256 times more data than what were used in the proposed method. Notice again that the red graph lies near the center of the blue graph, indicating that both sets of test results have the same accuracy and the red has a little bit better precision as the red noise band is narrower than the blue. If we follow the theoretical derivation, we would predict that the red noise band is 1.25 times narrower than the blue. A visual

judgment provides a quick confirmation of the theoretical prediction.

In both case studies, a quick visual inspection of the INL plots indicates that the measurement uncertainty bands have widths closely matching the values predicted by theory. The ratio of the noise band width of the new algorithm to that of the standard histogram test also matches the theoretical prediction. However, since these are measurement results, the true measurement uncertainty is unknown. Nevertheless, we can use repeatability of the test results as an estimate of the measurement uncertainty. To this end, the device in the first case study was tested again on a different day using both the new algorithm and the histogram test. Results from the two INL tests using the new algorithm are subtracted and the difference is shown in the top graph of Figure 9. Clearly the difference is mostly limited to within +-0.1 LSB and for a few codes reaches -0.14 LSB. This is very close to the uncertain prediction by the theory. Results from the two histogram tests are also subtracted and the difference is shown in the lower graph of Figure 9. It can be seen, the noise band is about 3 times wider than the top graph. This proves that the new algorithm produced INL test results that are significantly more repeatable while using 64 times less data than the standard histogram test.

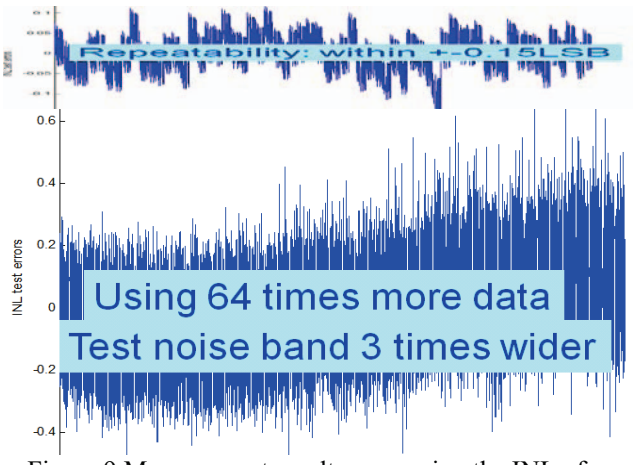

Figure 9 Measurement results comparing the INL of a 16 bit SAR ADC by the standard histogram method with 128 hits/code against INL by the proposed method using spectral test data that has about 0.5 hit/code. True INL is unknown and input referred noise is unknown

Till now, measurement results have shown that with 64 to 256 times less data, the new algorithm was able to produce INL test results that are of similar accuracy to the standard histogram test, but with better or significantly better precision. But accuracy for both methods could be bad simultaneously since true INL is unknown. To establish test accuracy, further case studies were conducted against the gold standard servo loop testing. Due to space limitation, we will present one set of case study results.

Shown below in Figure 10 are both INL plot (top) and DNL plot (bottom) in blue for a 16 bit SAR ADC, as tested by the gold standard servo loop test. Overlaying on the same graphs are the INL plot and DNL plot in red as tested by the proposed new algorithm. The servo loop took over 18 minutes to complete the test, while the new algorithm used only 16K data taking less than 0.1 sec. Note that the match between the two methods is excellent.

In Figure 11, a zoomed-in view is provided for the same INL/DNL plots near output code 1000. They clearly show code-for-code match between the servo-loop test results and the proposed method results. This demonstrates the new algorithm's ability to produce highly accurate test results for full code testing of both INL and DNL with the number of samples as small as 1/4 the number of codes.

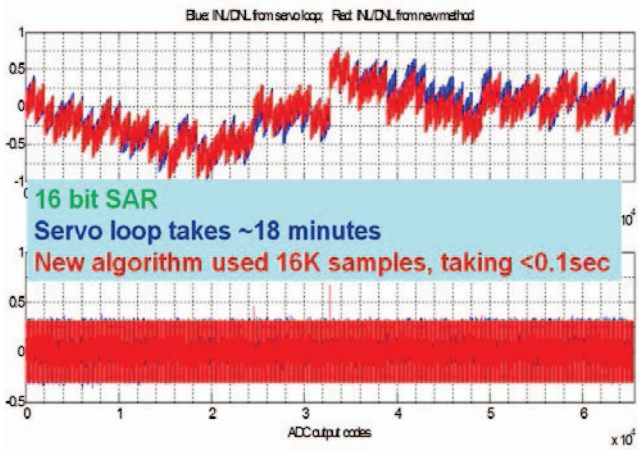

Figure 10 Comparison of tested INL/DNL values of a 16 bit SAR ADC from the new algorithm using only 16K samples against those from the gold standard servo loop test. Though not shown, zoomed-in views demonstrate excellent code-for-code match in both INL and DNL.

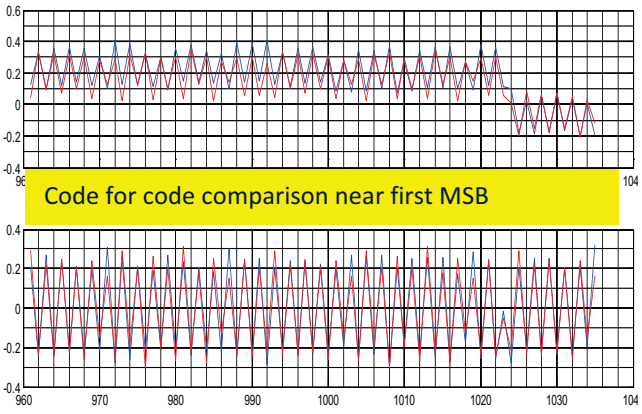

Figure 11 A zoomed-in view of the INL/DNL plot near the first MSB transition, showing excellent code for match

5. Limitations

The proposed method is intended for static linearity test of high resolution ADCs whose architecture naturally

facilitates a segmented structure of its INL/DNL curve. It is not intended for flash ADCs which are low resolution and do not have a segmented structure. It is not intended for delta sigma ADCs which do not have a segmented structure, even though they are high resolution. Even for ADCs with a segmented structure such as pipeline, when the resolution is below 12 bits, the ratio of number of transition voltages to number of error parameters in the model becomes low, and the proposed method does not offer any advantage to histogram test.

Occasionally, some people talk about "high frequency INL" or "dynamic INL/DNL". Regardless the exact meaning, the proposed method is not intended for capturing such errors. Only errors observable with repeatability under low frequency excitations are captured by the proposed method. Isolated code errors (sparkle) that happen at peculiar bit combinations are not identified as transfer curve errors.

The proposed algorithm offers significantly better noise averaging capability as compared to histogram test. However, this superior noise reduction is limited to true noise. For example, if the ADC's last few LSB bits makes systematic errors, they may appear like noise, but they cannot be averaged out. As another example, the so-called quantization noise is actually not noise and by itself cannot be averaged out. For such kind of non-noise errors, additional tricks must be used to either measure and cancel them systematically, or "whiten" then so that they can be averaged out.

6. Discussion

The limitation to higher resolution ADCs is not a significant one since test time for low resolution ADCs is very short and there is no material gain even if it can be reduced. High resolution delta sigma ADCs are never tested for full code INL/DNL. Hence, the new method is not more restrictive than the standard histogram test. However, it would be great if a method can be developed to allow linearity test of delta sigma ADCs beyond the couple handful codes that they are typically tested. The proposed method may have opened up a possible direction toward fuller coverage linearity test for delta sigma ADCs.

Because of the dramatically reduced test time, the new method offers new pathways towards ADC calibration and trimming based on full code INL/DNL test. Such calibration and trimming can be optimized to reduce the after-trimming linearity to the minimum possible level. In contrast, the local measurement based calibration and trimming prevalent in the literature and in industry will inevitably suffer from cumulative errors and lead to less than optimal performance.

Although the goal of reducing test time at final production test is what has driven the algorithm development, but the method applies equally well at characterization test. Since characterization is very thorough involving many repeated tested at various conditions, the new method can significantly cut down the characterization time. Since characterization time is engineering time, its per unit cost is much more significant. Furthermore, faster characterization also leads to faster time to market.

7. Conclusions

In the standard histogram method for ADC linearity test, a large number of samples per code must be used to average down the effect of measurement noise, leading to long test time and high test cost, especially for higher resolution ADCs. The new algorithm presented in this paper uses three highly effective techniques to greatly improve the efficiency in ADC linearity test: 1) taking advantage of a very accurate input signal to generate expected output by a linear ADC, 2) making all samples contribute linearly to noise averaging, 3) exploiting the highly dependent nature of code bin width in high resolution ADCs. These techniques enable efficient identification of a segmented non-parametric model of the ADC INL curve. From the identified model, full code INL/DNL values can be easily computed. This leads to greatly improved noise averaging efficiency, dramatically reduced number of samples required, and dramatically reduced test time and test cost for high resolution ADC linearity test.

In controlled simulation studies where the true ADC nonlinearity and measurement noise are available for comparison, the proposed method shows noise suppression capability far more superior to that of the standard histogram method. Data acquisition time can be reduced by a factor of several hundreds.

Measurement results in multiple case studies demonstrated that the proposed method can achieve similar test accuracy and better test precision than the standard histogram method, using up to 256 times less data acquisition. Comparison against servo loop test demonstrates the test accuracy of the new method.

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