DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT04
Hex inverter

Product specification
File under Integrated Circuits, IC06

September 1993
Hex inverter  

74HC/HCT04

FEATURES

• Output capability: standard
• I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT04 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A. The 74HC/HCT04 provide six inverting buffers.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>TYPICAL</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I_{PHL} / I_{PLH}</td>
<td>propagation delay nA to nY</td>
<td>C_L = 15 pF; V_{CC} = 5 V</td>
<td>7</td>
<td>8 ( \text{ns} )</td>
</tr>
<tr>
<td>C_I</td>
<td>input capacitance</td>
<td></td>
<td>3.5</td>
<td>3.5 ( \text{pF} )</td>
</tr>
<tr>
<td>C_{PD}</td>
<td>power dissipation capacitance per gate</td>
<td>notes 1 and 2</td>
<td>21</td>
<td>24 ( \text{pF} )</td>
</tr>
</tbody>
</table>

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_{D} in \( \mu \text{W} \)):

   \[ P_{D} = C_{PD} \times V_{CC}^2 \times f_{i} + \sum (C_L \times V_{CC}^2 \times f_o) \]

   where:

   - \( f_i \) = input frequency in MHz
   - \( f_o \) = output frequency in MHz
   - \( \sum (C_L \times V_{CC}^2 \times f_o) \) = sum of outputs
   - \( C_L \) = output load capacitance in pF
   - \( V_{CC} \) = supply voltage in V

2. For HC the condition is \( V_I = \text{GND to } V_{CC} \)
   For HCT the condition is \( V_I = \text{GND to } V_{CC} - 1.5 \text{ V} \)

ORDERING INFORMATION

See “74HC/HCT/HCU/HCMOS Logic Package Information”.

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PIN DESCRIPTION

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>SYMBOL</th>
<th>NAME AND FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 3, 5, 9, 11, 13</td>
<td>1A to 6A</td>
<td>data inputs</td>
</tr>
<tr>
<td>2, 4, 6, 8, 10, 12</td>
<td>1Y to 6Y</td>
<td>data outputs</td>
</tr>
<tr>
<td>7</td>
<td>GND</td>
<td>ground (0 V)</td>
</tr>
<tr>
<td>14</td>
<td>VCC</td>
<td>positive supply voltage</td>
</tr>
</tbody>
</table>

Fig.1 Pin configuration.

Fig.2 Logic symbol.

Fig.3 IEC logic symbol.

Fig.4 Functional diagram.

Fig.5 Logic diagram (one inverter).

FUNCTION TABLE

<table>
<thead>
<tr>
<th>INPUT</th>
<th>OUTPUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>nA</td>
<td>nY</td>
</tr>
<tr>
<td>L</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
</tr>
</tbody>
</table>

Notes
1. H = HIGH voltage level
   L = LOW voltage level
Hex inverter 74HC/HCT04

DC CHARACTERISTICS FOR 74HC
For the DC characteristics see “74HC/HCT/HCU/HCMOS Logic Family Specifications”.
Output capability: standard
I\textsubscript{CC} category: SSI

AC CHARACTERISTICS FOR 74HC
GND = 0 V; t\textsubscript{r} = t\textsubscript{f} = 6 ns; C\textsubscript{L} = 50 pF

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>T\textsubscript{amb} (°C)</th>
<th>UNIT</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>+25</td>
<td>–40 to +85</td>
<td>–40 to +125</td>
</tr>
<tr>
<td>\text{min.}</td>
<td>\text{typ.}</td>
<td>\text{max.}</td>
<td>\text{min.}</td>
<td>\text{max.}</td>
</tr>
<tr>
<td>\text{min.}</td>
<td>\text{typ.}</td>
<td>\text{max.}</td>
<td>\text{min.}</td>
<td>\text{max.}</td>
</tr>
<tr>
<td>\text{min.}</td>
<td>\text{typ.}</td>
<td>\text{max.}</td>
<td>\text{min.}</td>
<td>\text{max.}</td>
</tr>
</tbody>
</table>

- \text{t}_{\text{PHL}} / \text{t}_{\text{PLH}} propagation delay
  - nA to nY
  - 25 ns
  - 9 ns
  - 7 ns
  - 105 ns
  - 21 ns
  - 18 ns
  - 130 ns
  - 26 ns
  - 22 ns
  - 2.0
  - 4.5
  - 6.0
  - Fig.6

- \text{t}_{\text{THL}} / \text{t}_{\text{TLH}} output transition time
  - 19 ns
  - 7 ns
  - 6 ns
  - 75 ns
  - 15 ns
  - 13 ns
  - 95 ns
  - 19 ns
  - 16 ns
  - 110 ns
  - 22 ns
  - 19 ns
  - 2.0
  - 4.5
  - 6.0
  - Fig.6
DC CHARACTERISTICS FOR 74HCT
For the DC characteristics see “74HC/HCT/HCU/HCMOS Logic Family Specifications”.
Output capability: standard
I\(\text{CC}\) category: SSI

Note to HCT types
The value of additional quiescent supply current (\(\Delta I\text{CC}\)) for a unit load of 1 is given in the family specifications. To determine \(\Delta I\text{CC}\) per unit, multiply this value by the unit load coefficient shown in the table below.

<table>
<thead>
<tr>
<th>INPUT</th>
<th>UNIT LOAD COEFFICIENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>nA</td>
<td>1.20</td>
</tr>
</tbody>
</table>

AC CHARACTERISTICS FOR 74HC
GND = 0 V; \(t_r = t_f = 6\) ns; \(C_L = 50\) pF

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>(T_{\text{amb}}) (°C)</th>
<th>UNIT</th>
<th>TEST CONDITIONS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>74HCT</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(+25)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\text{min.})</td>
<td></td>
<td>(V_{\text{CC}})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\text{typ.})</td>
<td></td>
<td>WAVEFORMS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\text{max.})</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\text{min.})</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>(\text{max.})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(t_{\text{PHL}}/t_{\text{PLH}})</td>
<td>propagation delay</td>
<td>10</td>
<td>19</td>
<td>24</td>
</tr>
<tr>
<td>(t_{\text{THL}}/t_{\text{TLH}})</td>
<td>output transition</td>
<td>7</td>
<td>15</td>
<td>19</td>
</tr>
<tr>
<td></td>
<td>time</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

AC WAVEFORMS

Fig.6 Waveforms showing the data input (nA) to data output (nY) propagation delays and the output transition times.

PACKAGE OUTLINES
See “74HC/HCT/HCU/HCMOS Logic Package Outlines”.