Nonlinear Circuits and Nonlinear Devices

- Diode
- BJT
- MOSFET
**Thanks for your input!**

<table>
<thead>
<tr>
<th>Question</th>
<th>Mean</th>
<th>Var</th>
<th>Min</th>
<th>Max</th>
</tr>
</thead>
<tbody>
<tr>
<td>How many hours do you spend per week working with lecture material</td>
<td>8.6</td>
<td>3.3</td>
<td>4.5</td>
<td>20.0</td>
</tr>
<tr>
<td>(including time spent in the lecture and HW)</td>
<td></td>
<td></td>
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<tr>
<td>Of those in the first question, how many are spent in group study?</td>
<td>2.5</td>
<td>2.1</td>
<td>0.0</td>
<td>7.0</td>
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<tr>
<td>How many hours per week do you spend working in the lab on laboratory</td>
<td>5.4</td>
<td>3.7</td>
<td>2.5</td>
<td>20.0</td>
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<tr>
<td>experiments</td>
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<tr>
<td>How many additional hours per week do you spend on laboratory</td>
<td>3.1</td>
<td>2.3</td>
<td>0.0</td>
<td>11.0</td>
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<tr>
<td>requirements?</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>What percent of the lectures do you attend?</td>
<td>93.0</td>
<td>15.5</td>
<td>10.0</td>
<td>100.0</td>
</tr>
<tr>
<td>How many hours do you spend reading materials from text or notes</td>
<td>1.4</td>
<td>2.0</td>
<td>0.0</td>
<td>10.0</td>
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<tr>
<td>not associated with solving homework assignments</td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>What was your grade average, before the retake, on the first two exams</td>
<td>58.0</td>
<td>12.3</td>
<td>20.0</td>
<td>82.0</td>
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<tr>
<td>Total Hours</td>
<td>17.1</td>
<td>6.2</td>
<td>8.0</td>
<td>35.0</td>
</tr>
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</table>
MOS Transistors

Review from Last Time:

MOSFET

n-channel

p-channel
In *most* analog applications, the MOSFET is operated in the saturation region.

In *most* digital applications, the MOSFET is operated in either the cutoff or triode regions and changes between these two regions as the boolean variables change from a “0” to a “1”
n-type resistor

If $H$ is small compared to $L$ and $W$, termed a thin-film resistor

\[ R = \rho \frac{L}{WH} \]
If $H$ is small compared to $L$ and $W$, termed a thin-film resistor.
n-Channel MOSFET

- Source
- Drain
- Gate
- Bulk
- L
- W
- L_{\text{EFF}}
- Poly
- n-active
- Gate oxide
- p-sub
- depletion region (electrically induced)
n-Channel MOSFET Operation and Model

“Cutoff” region of operation

\[ I_D = 0 \]
\[ I_G = 0 \]
\[ I_B = 0 \]
n-Channel MOSFET Operation and Model

Critical value of $V_{GS}$ that creates inversion layer termed threshold voltage, $V_T$)

“Triode” region of operation
Inversion layer forms in channel
Inversion layer will support current flow from D to S
Channel behaves as thin-film resistor

$I_D R_{CH} = V_{DS}$
$I_G = 0$
$I_B = 0$
n-Channel MOSFET Operation and Model

Inversion layer disappears near drain

“Saturation” region of operation

Saturation first occurs when $V_{DS} = V_{GS} - V_T$

$I_D = ?$
$I_G = 0$
$I_B = 0$
Transistor Size Comparison with 24AWG Copper Cable
(Drawn to scale)

State of Art transistor dimensions about 200 times smaller (lateral) than 10μ fiber

The gates of about 40000 transistors can be placed on the cross-section of this fiber (maybe only 4000 transistors)
MOS Transistors

Standard square-law model

\[ I_g = 0 \]

\[ I_D = \begin{cases} \frac{\mu C_{ox} W}{L} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS} & V_{GS} < V_T \\ \frac{\mu C_{ox} W}{2L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) & V_{GS} \geq V_T \end{cases} \]

- \( V_{GS} \leq V_T \)  \( V_{DS} \leq V_{GS} - V_T \)  Cutoff
- \( V_{GS} \geq V_T \)  \( V_{DS} > V_{GS} - V_T \)  Saturation

\( \mu C_{ox} \approx 10^{-2} \frac{A}{\sqrt{V^2}} \)

\( \lambda \approx 0.01V^{-1} \)

\( V_T \approx 0.5V \) to \( 3V \)

\( W/L \)  varies by design
MOS Transistors

p-channel MOSFET

\[ V_{GS} \quad V_{DS} \quad I_D \]

\[ I_D = \begin{cases} 
0 & \text{Cutoff} \\
\mu C_{ox} \frac{W}{L} \left( V_{gs} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{gs} < V_T \\
(\mu C_{ox}) \frac{W}{2L} (V_{gs} - V_T)^2 (1 + \lambda V_{DS}) & V_{gs} \leq V_T \quad V_{DS} \geq V_{gs} - V_T \end{cases} \]

\[ V_{GS1} \quad V_{GS2} \quad V_{GS3} \quad V_{GS4} \quad V_{GS5} \quad V_{GS6} \]

Standard square-law model

Cutoff
\[ V_T < 0 \]
\[ I_D \leq 0 \]

Saturation
\[ V_{DS} \leq 0 \]
MOS Transistor Models
simplifications

Switch-level dc model — good enough for predicting basic operation of many digital circuits
MOS Transistor Models
simplifications

\[ I_G = 0 \]
\[ I_D = 0 \quad V_{GS} < V_T \quad \text{Cutoff} \]
\[ V_{DS} = 0 \quad V_{GS} \geq V_T \quad \text{Triode} \]

Equivalent Circuit Models

\[ V_{GS} < V_T \]
\[ V_{GS} > V_T \]

S\(_1\) open for \(V_{GS} < V_T\)
S\(_1\) closed for \(V_{GS} > V_T\)
MOS Transistor Models
simplifications

Switch-level dc model – good enough for predicting basic operation of many digital circuits
MOS Transistor Models
simplifications

- \( I_g = 0 \)
  \( V_{ds} > V_T \)  
  Cutoff

- \( I_d = 0 \)
  \( V_{gs} \leq V_T \)
  Triode

Equivalent Circuit Models

- \( V_{gs} > V_T \)
  \( V_{gs} < V_T \)

- \( S_1 \) open for \( V_{gs} > V_T \)
  \( S_1 \) closed for \( V_{gs} < V_T \)
MOS Transistor Models simplifications

**Better Switch-level dc model** — good enough for predicting basic operation of many digital circuits and can be used to predict speed performance if parasitic capacitances are added

\[ I_D = \begin{cases} 0 & \text{if } V_{GS} < V_T \\ \frac{V_{DS}}{R_{FET}} & \text{if } V_{GS} \geq V_T \end{cases} \]

\[ R_{FET} \approx \frac{1}{V_{GS} - V_T} \left( \frac{L}{\mu C_{ox} W} \right) \]
MOS Transistor Models
simplifications

\[ I_D = \begin{cases} 0 & V_{GS} < V_T \\ \frac{V_{DS}}{R_{FET}} & V_{GS} \geq V_T \end{cases} \]

- **Cutoff**
- **Triode**

\[ R_{FET} \approx \frac{1}{V_{GS} - V_T} \left( \frac{L}{\mu C_{ox} W} \right) \]

- \( S_1 \) closed for \( V_{GS} > V_T \)
- \( S_1 \) open for \( V_{GS} < V_T \)
MOS Transistor Models

Voltage Variable Resistor (VVR) operation

\[ R_{FET} \approx \frac{1}{V_{GS} - V_T} \left( \frac{L}{\mu C_{OX} W} \right) \]

\[ I_D = \begin{cases} 0 & V_{GS} < V_T \quad \text{Cutoff} \\ \frac{V_{DS}}{R_{FET}} & V_{GS} \geq V_T \quad \text{Triode} \end{cases} \]

**VVR Application** — \textit{dc} gate to source voltage can be used to control the resistance

\textit{Widespread applications in analog circuits and computer-control of electronic circuits}
MOS Transistor Models
Voltage Variable Resistor (VVR) operation

Analog application of MOSFET in triode region

\[ R_{\text{FET}} \approx \frac{1}{V_{\text{GS}} - V_{\text{T}}} \left( \frac{L}{\mu C_{\text{OX}} W} \right) \]
Voltage Variable Resistor

Applications include Automatic Gain Control (AGC)
Voltage Variable Resistor

Applications include Automatic Gain Control (AGC)
MOS Transistor Models

simplifications

Saturation Region Model – used for many analog applications

$$I_D = \left( \frac{\mu C_{ox} W}{2L} \right) (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

Saturation

Can often assume $\lambda = 0$
MOS Transistor Models
simplifications

Saturation Region Model – good enough for many analog applications

\[ I_D = \left( \frac{\mu C_{ox} W}{2L} \right) (V_{GS} - V_T)^2 \]

With \( \lambda = 0 \)

Saturation Region Model – good enough for many analog applications
MOS Transistor Models
simplifications

Saturation Region Model — good enough for many analog applications
MOS Transistor Models (Summary)
MOS Transistor Models (Summary)

\[ I_D = \left( \frac{\mu C_w W}{2L} \right) (V_G - V_T) \left( 1 + \lambda V_D \right) \]

- \( S_1 \) open for \( V_{GS} < V_T \)
- \( S_1 \) closed for \( V_{GS} > V_T \)

- \( S_1 \) closed for \( V_{GS} > V_T \)
- \( S_1 \) open \( V_{GS} < V_T \)
MOS Transistor Applications (Digital Circuits)

Assume “1” $\sim V_H = V_{DD} > V_T$

Assume “0” $\sim V_L = 0V < V_T$

MOSFET Model

$I_G = 0$

$I_D = 0 \quad V_{GS} < V_T \quad \text{Cutoff}$

$V_{DS} = 0 \quad V_{GS} \geq V_T \quad \text{Triode}$

Assume $V_T \sim V_{DD}/5$
MOS Transistor Applications  
(Digital Circuits)

\[ V_{DD} \]
\[ Y \]
\[ M_1 \]

Assume “1” \( \sim \) \( V_H = V_{DD} > V_T \)

Assume “0” \( \sim \) \( V_L = 0V < V_T \)

\[ I_D = 0 \quad V_{gs} < V_T \quad \text{Cutoff} \]
\[ V_{ds} = 0 \quad V_{gs} \geq V_T \quad \text{Triode} \]

Assume \( V_T \sim V_{DD}/5 \)

If “1” \( \sim \) \( X = V_{DD} \), \( V_{DS} = 0V \) so \( Y = 0V \) \( \sim \) “0”

If “0” \( \sim \) \( X = 0V \), \( I_D = 0A \) so \( Y = V_{DD} - I_D R = V_{DD} \) \( \sim \) “1”

So this circuit performs as a Boolean inverter

Assume “0” \( \sim \) \( V_L < V_T \)

Assume “1” \( \sim \) \( V_H > V_T \)

<table>
<thead>
<tr>
<th>X</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
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</tbody>
</table>

Truth Table
MOS Transistor Applications
(Digital Circuits)

Assume “1” \( V_H = V_{DD} > V_T \)
Assume “0” \( V_L = 0V < V_T \)

\begin{align*}
I_g &= 0 \\
I_D &= 0 \quad V_{GS} < V_T \quad \text{Cutoff} \\
V_{DS} &= 0 \quad V_{GS} \geq V_T \quad \text{Triode}
\end{align*}

Assume \( V_T \approx V_{DD}/5 \)
MOS Transistor Applications
(Digital Circuits)

Assume “1” ~ $V_H = V_{dd} > V_T$

Assume “0” ~ $V_L = 0V < V_T$

$I_d = 0 \quad V_{gs} < V_T$  \quad \text{Cutoff}

$V_{ds} = 0 \quad V_{gs} \geq V_T$  \quad \text{Triode}

Assume $V_T \sim V_{dd}/5$

If “1” ~ A = $V_{dd}$, “1” ~ B = $V_{dd}$, $V_{ds1}=V_{ds2}=0V$  so $Y = 0V \sim “0”$

If “1” ~ A = $V_{dd}$, “0” ~ B = 0V, $V_{ds1} = 0V$  \hspace{1em} (and $I_{d2}=0A$) \hspace{1em} so $Y = 0V \sim “0”$

If “0” ~ A = 0V, “1” ~ B = $V_{dd}$, $V_{ds2} = 0V$  \hspace{1em} (and $I_{d1}=0A$) \hspace{1em} so $Y = 0V \sim “0”$

If “0” ~ A = 0V, “0” ~ B = 0V, $I_{d2} = 0A$  \hspace{1em} and $I_{d1}=0A$ \hspace{1em} so $I_R=0A$, thus

\[ Y = V_{dd} = I_R R = V_{dd} \sim “1” \]
MOS Transistor Applications
(Digital Circuits)

If “1”~ A = V_DD, “1”~ B = V_DD, V_DS1 = V_DS2 = 0V so Y = 0V ~ “0”

If “1”~ A = V_DD, “0”~ B = 0V, V_DS1 = 0V (and I_D2 = 0A) so Y = 0V ~ “0”

If “0”~ A = 0V, “1”~ B = V_DD, V_DS2 = 0V (and I_D1 = 0A) so Y = 0V ~ “0”

If “0”~ A = 0V, “0”~ B = 0V, I_D2 = 0A and I_D1 = 0A so I_R = 0A, thus

Y = V_DD = I_R R = V_DD ~ “1”

2-input NOR Gate
MOS Transistor Applications
(Digital Circuits)

Assume “1” ~ $V_H = V_{DD} > V_T$

Assume “0” ~ $V_L = 0V < V_T$

$I_d = 0$  \hspace{1cm} $V_{gs} < V_T$  \hspace{1cm} Cutoff

$V_{ds} = 0$  \hspace{1cm} $V_{gs} \geq V_T$  \hspace{1cm} Triode

Assume $V_T \sim V_{DD}/5$

If “1” ~ $A = V_{DD}$, “1” ~ $B = V_{DD}$, $V_{DS1} = V_{DS2} = 0V$ so $Y = 0V \sim "0"$

If “1” ~ $A = V_{DD}$, “0” ~ $B = 0V$, $V_{DS1} = 0V$ and $I_{d2} = 0A$ so $I_R = 0A$ thus

$Y = V_{DD} - I_R R = V_{DD} \sim "1"

If “0” ~ $A = 0V$, “1” ~ $B = V_{DD}$, $V_{DS2} = 0V$ and $I_{d1} = 0A$ so $I_R = 0A$ thus

$Y = V_{DD} - I_R R = V_{DD} \sim "1"

If “0” ~ $A = 0V$, “0” ~ $B = 0V$, $I_{d1} = 0A$ and $I_{d2} = 0A$ so $I_R = 0A$ thus

$Y = V_{DD} - I_R R = V_{DD} \sim "1"$
MOS Transistor Applications (Digital Circuits)

If \( 1 \sim A = V_{DD}, \quad 1 \sim B = V_{DD}, \quad V_{DS1} = V_{DS2} = 0V \) so \( Y = 0V \sim \text{"0"} \)

If \( 1 \sim A = V_{DD}, \quad 0 \sim B = 0V, \quad V_{DS1} = 0V \) and \( I_{D2} = 0A \) so \( I_R = 0A \) thus \( Y = V_{DD} - I_R R = V_{DD} \sim \text{"1"} \)

If \( 0 \sim A = 0V, \quad 1 \sim B = V_{DD}, \quad V_{DS2} = 0V \) and \( I_{D1} = 0A \) so \( I_R = 0A \) thus \( Y = V_{DD} - I_R R = V_{DD} \sim \text{"1"} \)

If \( 0 \sim A = 0V, \quad 0 \sim B = 0V, \quad I_{D1} = 0A \) and \( I_{D2} = 0A \) so \( I_R = 0A \) thus \( Y = V_{DD} - I_R R = V_{DD} \sim \text{"1"} \)

2-input NAND Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
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<tr>
<td>0</td>
<td>1</td>
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<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Truth Table
MOS Transistor Applications
(Digital Circuits)

- Can be extended to arbitrary number of inputs
- But the resistor is not practically available in most processes and static power dissipation is too high