EE 330
Exam 1
Fall 2007

Students may bring one piece of paper with notes on two sides or two sheets with notes on one side to this exam. On the exam, there are a set of short questions and 5 problems. The points allocated to each question are as indicated. Each problem is worth 16 points. All work and answers are to appear on this exam sheet. Attach additional sheets only if you run out of room on the examination itself.

If references semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters: \( \mu_n C_{OX} = 100 \mu A/\sqrt{\text{ }}, \mu_p C_{OX} = \mu_n C_{OX}/3\), \( V_{TNO} = 1 \text{ V}, \ V_{TP0} = -1 \text{ V}\), \( C_{OX} = 2fF/\mu^2\), \( \lambda = 0\), and \( \gamma = 0\). If any other detailed information about a CMOS process is needed beyond, consult the process information attached at the end of this exam.

Questions

1. (2 pts) The International Technology Roadmap for Semiconductors (ITRS) makes predictions on challenges and trends in the semiconductor industry. What is the ITRS projecting for the supply voltage of digital ICs in 10 years?

2. (2 pts) The acronym LVS is used to discuss an important operation in the design flow of an integrated circuit. What tool is this referring to?

3. (2 pts) If the breakdown voltage of SiO\(_2\) is 10 MV/cm, what fraction of the breakdown voltage would a gate oxide that is 60 A thick experience if a gate-source voltage of 2.5 V is applied?

4. (2 pts) One of the co-inventors of the transistor formed a company in the San Francisco Bay area to make transistors. This is one of the major reasons that the “Silicon Valley” is now in that area. Who was that person?
5. (2pts) The CMOS process, although more costly, replaced the much simpler NMOS process in the mid 80’s and has been the dominant process in the semiconductor industry ever since. What is the major reason the CMOS process replaced the NMOS process?

6. (2pts) Why are the design rules for a contact opening specified “exactly” whereas almost all other design rules are given in terms of the minimum allowable feature size?

7. (2pts) Design rules are often given in terms of a parameter $\lambda$ rather than in terms of the actual dimensions. What is the reason the $\lambda$-based design rules are so widely used?

8. (2pts) What is the major advantage of using a dry etch rather than a wet etch when an etching processing step is required?

9. (2pts) What is the major reason Shallow Trench Isolation (STI) rather than Local Oxidation (LOCOS) is becoming more preferred for providing electrical isolation of MOS devices?

10. (2pts) Several models that have been introduced for the MOS transistor are appended at the end of this exam. What are the process parameters for the extended square-law model of the device?
Problem 1   Assume the hard yield for an integrated circuit that implements a given function with a die of area A is 60% and the cost per good die is $4.50. Assume the same function could be obtained by splitting the circuit into two parts each requiring a die of area A/2 and then using two of these smaller die to implement the same function. How would the cost for a two good small die solution compare to that of the single die solution? Be quantitative.
Problem 2 Assume the MOSFET in the circuit shown has $W=2\mu$ and $L=10\mu$. Determine the voltage $V_{\text{OUT}}$ (remember the model parameters are given on the first page of this exam).
Problem 3    The layout of a simple circuit in an n-well bulk CMOS process is shown below. Assume the substrate is connected to 0V.

a) Sketch a cross-sectional view of the die that will be formed with this layout along the AA’ section line
b) Determine the capacitance from the gate to substrate of the transistor.
c) Determine the maximum voltage $V_X$ that will keep the transistor operating in the triode region.

Use the process parameters listed on the last page of this exam to solve this problem.
Problem 4  Assume the two diodes in the circuit shown are matched. This circuit is useful as a temperature sensor providing an output voltage $V_{\text{OUT}}$ that is linearly dependent upon temperature $T$, i.e., $V_{\text{OUT}} = \theta T$ where $T$ is in °K. Determine the coefficient $\theta$. (The diode equation under forward bias is given at the bottom of this page should you find it of use)

Diode equation under forward bias

$$I_d = I_s e^{\frac{V_d}{V_t}}$$

where

$$I_s = J_{sx} A \left[ T^m e^{\frac{-V_{so}}{V_t}} \right]$$
Problem 5

a) Design a circuit at the transistor level using complex logic gates that implements the Boolean function \( F = \overline{A}B + CB \). Assume you have available inputs \( A, B \) and \( C \) and that a static CMOS inverter is to be used if the compliments of any input variables are needed.

b) Quantitatively compare the number of transistors and the number of levels of logic for the complex logic gate implementation of part a) to that which would be required to implement the same function using static CMOS NAND and NOR gates.
Some Models for the MOS Transistor

**Basic Switch-Level Model**

\[ I_G = 0 \quad I_B = 0 \]

\[ I_c = 0 \quad \text{if } V_c \text{ is low} \]

\[ V_c = 0 \quad \text{if } V_c \text{ is high} \]

**Extended Switch-Level Model**

\[ I_G = 0 \quad I_B = 0 \]

Switch open for \( V_{GS} \) = small

Switch closed for \( V_{GS} \) = large

**Basic Square-Law Model**

\[ I_G = 0 \quad I_B = 0 \]

\[
I_c = \begin{cases} 
0 & V_{gs} \leq V_t \\
\mu C_{ox} \frac{W}{L} \left( V_{gs} - V_T - \frac{V_{gs} - V_T}{2} \right) V_{ds} & V_{gs} > V_T, \ V_{gs} < V_{gs} - V_T \\
\mu C_{ox} \frac{W}{2L} (V_{gs} - V_T)^2 & V_{gs} > V_T, \ V_{gs} \geq V_{gs} - V_T 
\end{cases}
\]

**Extended Square-Law Model**

\[ I_G = 0 \quad I_B = 0 \]

\[
I_c = \begin{cases} 
0 & V_{gs} \leq V_t \\
\frac{\theta}{\theta_i} \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)^2 V_{gs} & V_{gs} \geq V_T, \ V_{gs} < \theta_i (V_{gs} - V_T)^2 \\
\theta \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)^2 (1 + \lambda V_{gs}) & V_{gs} \geq V_T, \ V_{gs} \geq \theta_i (V_{gs} - V_T)^2 
\end{cases}
\]

\[ V_T = V_{TO} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right) \]

**Basic Short Channel Model**

\[ I_G = 0 \quad I_B = 0 \]

\[
I_c = \begin{cases} 
0 & V_{gs} \leq V_t \\
\frac{\theta}{\theta_i} \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)^2 V_{gs} & V_{gs} \geq V_T, \ V_{gs} < \theta_i (V_{gs} - V_T)^2 \\
\theta \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)^2 (1 + \lambda V_{gs}) & V_{gs} \geq V_T, \ V_{gs} \geq \theta_i (V_{gs} - V_T)^2 
\end{cases}
\]

\[ V_T = V_{TO} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right) \]
## Transistor Parameters

### Minimum
- W/L: 3.0/0.6
- Vth: 0.78 V, -0.93 V
- Idss: 439 μA/μm, -238 μA/μm
- Vth: 0.69 V, -0.90 V
- Vpt: 10.0 V, -10.0 V

### Short
- W/L: 20.0/0.6
- Idss: 439 μA/μm, -238 μA/μm
- Vth: 0.69 V, -0.90 V
- Vpt: 10.0 V, -10.0 V

### Wide
- W/L: 20.0/0.6
- Ids0: < 2.5 pA/μm, < 2.5 pA/μm

### Large
- W/L: 50/50
- Vth: 0.70 V, -0.95 V
- Vjbkd: 11.4 V, -11.7 V
- Ijlk: < 50.0 pA, < 50.0 pA
- Gamma: 0.50 V^0.5, 0.58 V^0.5
- K' (Uo*Cox/2): 56.9 μA/V^2, -18.4 μA/V^2
- Low-field Mobility: 474.57 cm^2/V*s, 153.46 cm^2/V*s

**Comments:** XL_AMI_C5F

## Fox Transistors

### GATE
- Vth: Poly > 15.0 V, -15.0 V

## Process Parameters

### Sheet Resistance
- N+ Activ: 82.7 Ω/sq, 103.2 Ω/sq, 21.7 Ω/sq
- P+ Activ: 21.7 Ω/sq
- Poly: 984 Ω/sq
- POLY2_HR: 39.7 Ω/sq
- POLY2: 0.09 Ω/sq
- MTL1: 0.09 Ω/sq
- MTL2: 0.09 Ω/sq

### Contact Resistance
- N+ Activ: 56.2 Ω, 118.4 Ω, 14.6 Ω
- P+ Activ: 24.0 Ω
- Poly: 24.0 Ω
- Poly2: 0.78 Ω

### Gate Oxide Thickness
- 144 Å

**Comments:** N\POLY is N-well under polysilicon.

## Capacitance Parameters

### Area
- Substrate: 429 aF/μm^2, 721 aF/μm^2
- N+ Active: 82 aF/μm^2
- P+ Active: 32 aF/μm^2, 17 aF/μm^2, 10 aF/μm^2, 40 aF/μm^2
- N_Well: 32 aF/μm^2

**Comments:**

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