EE 330
Exam 1
Spring 2007

Students may bring one piece of paper with notes on one side to this exam. On the exam, there are a set of short questions and 5 problems. The points allocated to each question are as indicated. Each problem is worth 16 points. All work and answers are to appear on this exam sheet. Attach additional sheets only if you run out of room on the examination itself.

If detailed information about a CMOS process is needed beyond what is specified in any problem on any question, consult the process information attached at the end of this exam. If any other process parameters are needed, specify clearly what process parameter is needed and specify a typical value for that parameter.

Questions

1. (2pts) What is the minimum gate length in a state of the art CMOS process today?

2. (4pts) How many silicon atoms are in a crystal of silicon that is in the shape of a cube 10μ on a side?

3. (2pts) What is the difference between sheet resistance and resistivity?

4. (4 pts) What is the maximum die area that can be used if the hard yield is to be 80% and the defect density is 1.5/cm²?
5. (2pts) State Moore’s Law

6. (2pts) One of the pioneers of the semiconductor industry was from Iowa. Identify who this was and name one of the companies he co-founded.

7. (2pts) There are multiple logic design styles that are regularly used. Three have been discussed so far in this course. Give two of these three?

8. (2pts) What is the major advantage of using a dry etch rather than a wet etch when an etching processing step is required?
Problem 1 Assume op amps are to be made in a CMOS process with 12 inch wafers that cost $2600 each. If the die for the op amps is square of 400μ on a side, what is the manufacturing cost for the silicon that goes into the op amp? You may assume the hard yield and the soft yields are very high.
Problem 2 The switch-level model of a MOSFET developed early in the course is shown. Later a square-law model of the MOSFET was established. Although the basic operation of the MOSFET was not discussed when the switch-level model was introduced and as such, the resistor $R_{SW}$ was assumed to be a given value, now that the square-law model is available, the value of the $R_{SW}$ can be determined from the model parameters and the square-law model. Assuming the switch $S_1$ is “ON” when the MOSFET is operating in the triode region with small $V_{DS}$ and with a controlling voltage of $V_{GS} = 5V$, determine $R_{SW}$ from the square law model if the length of the transistor is 1µ and the width of the transistor 8µ. The square-law model and the model parameters are given below.

Square Law Model:

$$I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{OX} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T
\end{cases}$$

Model parameters: $\mu C_{OX} = 100 \mu A V^{-2}$, $V_T = 1V$
Problem 3

An interconnect 400μ long and 1μ wide is used to drive a load resistor of $R_L=10K\Omega$. A long interconnect actually forms a long distributed delay line but can be is often modeled as a lumped circuit. Different lumped circuit models are used but for the purpose of this interconnect, the lumped circuit model shown below is quite useful where in this model, the resistance between the two ends of the interconnect is $2R_X$ and the capacitance from the interconnect to the substrate is $C_X$.

![Lumped Circuit Model](image)

a) Determine the lumped interconnect model if Poly 1 is used for the interconnect

b) Repeat if Metal 1 is used for the interconnect

c) (extra credit) Determine the rise time at the output $V_{OUT}$ if a 1V step is applied at the input and if the interconnect is Poly 1
Problem 4    If the current in a diode changes by +/- 1 decade above and below 1mA, what is the corresponding change in the diode voltage. Assume the diode has a junction area of 1000μ² and a saturation current density of J_s= 1fAμ²
Problem 5

a) Design a circuit using complex logic gates that implements the Boolean function \( F = \overline{AB} + C \). Assume you have available inputs \( A, B \) and \( C \) and that a static CMOS inverter is to be used if the compliments of any input variables are needed.

b) Give a stick diagram implementation of this complex logic gate. You may use your own convention for designating layers (different colors of ink, solid, dashed or dotted lines, etc. but whatever you use, give the appropriate designation).
## Transistor Parameters

<table>
<thead>
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<th>Parameter</th>
<th>Minimum</th>
<th>Wide</th>
<th>Large</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>W/L</strong></td>
<td>3.0/0.6</td>
<td>20.0/0.6</td>
<td>50/50</td>
</tr>
<tr>
<td><strong>Vth</strong></td>
<td>0.78</td>
<td>0.69</td>
<td>0.70</td>
</tr>
<tr>
<td><strong>Idss</strong></td>
<td>439 uA/µm</td>
<td>238 uA/µm</td>
<td>&lt;2.5 pA/µm</td>
</tr>
<tr>
<td><strong>Vth</strong></td>
<td>-0.93</td>
<td>-0.90</td>
<td>-0.95</td>
</tr>
<tr>
<td><strong>Vpt</strong></td>
<td>10.0</td>
<td>-10.0</td>
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### Comments:
- **XL_AMI_C5F**
- **FOX Transistors**
- **Process Parameters**
- **Capacitance Parameters**

## Comments:
- **N\POLY** is N-well under polysilicon.