Instructions: This is a 50 minute exam. Students may bring 3 pages of notes (front and back) to this exam. There are 10 questions and 5 problems. The points allocated to each question and each problem are as indicated. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If references to semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters: $\mu_n C_{OX} = 100 \mu A/\mu^2$, $\mu_p C_{OX} = \mu_n C_{OX}/3$, $V_{TNO} = 0.5 V$, $V_{TPO} = -0.5 V$, $C_{OX} = 2 \text{fF}/\mu^2$, $\lambda = 0$, and $\gamma = 0$. If reference to a bipolar process is made, assume this process has key process parameters $J_S = 10^{-15} A/\mu^2$, $\beta = 100$ and $V_{AF} = \infty$. Specify clearly what process parameters you are using in any solution requiring process parameters. Also attached to this exam is a table discussed in class that relates to the basic amplifier configurations.

1. (2pts) Why do we often characterize the input impedance, output impedance, and open loop voltage gain of amplifier structures?

2. (2pts) How does $g_m$ vary with $I_{DQ}$ in a MOS Transistor?

3. (2pts) The following structure has cropped up so many times in circuits that have been analyzed that it has a special name associated with it. What is this circuit configuration called?
4. (2pts) When biased at the same current levels, why does the BJT have a larger transconductance than the MOSFET?

5. (2pts) When we initially analyzed the amplifier shown below, assuming the transistor is operating in the forward active region and the current source $I_{xx}$ is ideal, we calculated an infinite voltage gain but on further analysis it was observed that the gain is not actually infinite and that the reason that the calculation showed an infinite gain was because we neglected a small signal model parameter that was not negligible in this circuit. What parameter was neglected that caused the gain to become infinite?

![Amplifier Diagram]

6. (2pts) What do we mean when we say a circuit is unilateral?

7. (2pts) What is a cascode amplifier?

8. (2pts) How does the $g_m$ of a BJT vary with bias current?
9. (2pts)  What is the difference between a current source and a current sink?

10. (2 pts)  What is the purpose of biasing an amplifier circuit?
**Problem 1** (16 Pts.) Assume the capacitors are large in the following circuit.

a) Determine the input impedance

b) Determine the quiescent output voltage

c) Obtain an expression for the small-signal voltage gain in terms of the components in the circuit and the small-signal model parameters for the devices

d) Obtain the output voltage \( V_{\text{OUT}}(t) \) if \( v_{\text{IN}} = 0.2 \sin(1000t) \)
Problem 2 (16 Pts.) Assume the voltages $V_{EE}$ and $V_{SS}$ are set so that $V_{DQ}=V_{CQ}=5\text{V}$. Numerically determine the small signal voltage gain of the circuit shown.
Problem 3 (16 Pts.) Assume $\beta=50$ for the two BJT transistors and the threshold voltage of the MOSFET is -1V. Determine the voltage $V_{OUT}$. 
**Problem 4** (16 Pts) Assume the capacitors in the following circuit are large.

a) Determine $W$ so that $V_{CQ} = 4V$.

b) Determine the small signal voltage gain from the input to the output indicated in terms of the small signal model parameters of the devices.
Problem 5 (16 Pts) Assume the capacitors in the following amplifier are large. Also assume the transistors are biased to that all BJTs are operating in the Forward Active region and all MOSFETs are operating in the saturation region.

a) Draw the small-signal equivalent circuit
b) Obtain an expression for the small-signal voltage gain in terms of the small-signal model parameters and the resistors in the circuit
### TRANSISTOR PARAMETERS

**W/L** | **N-CHANNEL P-CHANNEL** | **UNITS**
---|---|---
MINIMUM | 3.0/0.6 | 0.78 | -0.93 volts
SHORT | 20.0/0.6 | 439 | -238 uA/um
Vth | 0.69 | -0.90 volts
Vpt | 10.0 | -10.0 volts
WIDE | 20.0/0.6 | < 2.5 | < 2.5 pA/um
LARGE | 50/50 | 0.70 | -0.95 volts
Vth | 11.4 | -11.7 volts
Ijlk | <50.0 | <50.0 pA
Gamma | 0.50 | 0.58 V^0.5
K' (Uo*Cox/2) | 56.9 | -18.4 uA/V^2
Low-field Mobility | 474.57 | 153.46 cm^2/V*s

**COMMENTS: XL_AMI_C5F**

### FOX TRANSISTORS

**GATE** | **N+ACTIVE** | **P+ACTIVE** | **UNITS**
---|---|---|---
Vth | Poly | >15.0 | <-15.0 volts

### PROCESS PARAMETERS

**N+ACTV** | **P+ACTV** | **POLY** | **PLY2 HR** | **POLY2** | **MTL1** | **MTL2** | **UNITS**
---|---|---|---|---|---|---|---
Sheet Resistance | 82.7 | 103.2 | 21.7 | 984 | 39.7 | 0.09 | 0.09 ohms/sq
Contact Resistance | 56.2 | 118.4 | 14.6 | 24.0 | 0.78 | ohms
Gate Oxide Thickness | 144 | angstrom

**PROCESS PARAMETERS**

**MTL3** | **N\PLY** | **N WELL** | **UNITS**
---|---|---|---
Sheet Resistance | 0.05 | 824 | 815 | ohms/sq
Contact Resistance | 0.78 | ohms

**COMMENTS: N\POLY is N-well under polysilicon.**

### CAPACITANCE PARAMETERS

**N+ACTV** | **P+ACTV** | **POLY** | **POLY2** | **M1** | **M2** | **M3** | **N_WELL** | **UNITS**
---|---|---|---|---|---|---|---|---
Area (substrate) | 429 | 721 | 82 | 32 | 17 | 10 | 40 | aF/um^2
Area (N+active) | 2401 | | 36 | 16 | 12 | | | aF/um^2
Area (P+active) | 2308 | | | | | | | aF/um^2
Area (poly) | 864 | 61 | 17 | 9 | | | | aF/um^2
Area (poly2) | 53 | | | | | | | aF/um^2
Area (metal1) | 34 | 13 | | | | | | aF/um^2
Area (metal2) | 32 | | | | | | | aF/um^2
Fringe (substrate) | 311 | 256 | 74 | 58 | 39 | | | aF/um
Fringe (poly) | 53 | 40 | 28 | | | | | aF/um
Fringe (metal1) | 55 | 32 | | | | | | aF/um
Fringe (metal2) | 48 | | | | | | | aF/um
Overlap (N+active) | 206 | | | | | | | aF/um
Overlap (P+active) | 278 | | | | | | | aF/um
## Basic Amplifier Gain Table

<table>
<thead>
<tr>
<th>A&lt;sub&gt;V&lt;/sub&gt;</th>
<th>CE/CS</th>
<th>CC/CD</th>
<th>CB/CG</th>
<th>CEwRE/CSwRS</th>
</tr>
</thead>
<tbody>
<tr>
<td>BJT</td>
<td>MOS</td>
<td>BJT</td>
<td>MOS</td>
<td>BJT</td>
</tr>
</tbody>
</table>

- **A<sub>V</sub>**
  - BJT: \(-\frac{\beta V_I}{I_{CQ}} + \frac{g_m R_C}{V_I}\)
  - MOS: \(-\frac{2 \beta V_B}{Q V_E} + \frac{g_m R_C}{V_I}\)
  - CB/CG: \(-\frac{\beta V_I}{I_{CQ}} + \frac{2 \beta V_B}{Q V_E} + \frac{R_C}{R_E}\)
  - CEwRE/CSwRS: \(-\frac{R_C}{R_E}\)

- **R<sub>in</sub>**
  - BJT: \(\frac{R_I}{\beta V_I + \beta R_E}\)
  - MOS: \(\frac{R_I}{\beta V_I + \beta R_E}\)
  - CB/CG: \(\frac{R_I}{\beta V_I + \beta R_E}\)
  - CEwRE/CSwRS: \(\frac{R_I}{\beta V_I + \beta R_E}\)

- **R<sub>out</sub>**
  - BJT: \(R_C\)
  - MOS: \(R_C\)
  - CB/CG: \(R_C\)
  - CEwRE/CSwRS: \(R_C\)

### Dc and small-signal equivalent elements

- **dc Voltage Source**
  - Element: \(V_{dc}\)
  - dc equivalent: \(V_{dc}\)

- **ac Voltage Source**
  - Element: \(V_{ac}\)
  - dc equivalent: \(V_{ac}\)

- **dc Current Source**
  - Element: \(I_{dc}\)
  - dc equivalent: \(I_{dc}\)

- **ac Current Source**
  - Element: \(I_{ac}\)
  - dc equivalent: \(I_{ac}\)

- **Resistor**
  - Element: \(R\)
  - dc equivalent: \(R\)