Instructions: This is a 50 minute exam. Students may bring 3 page of notes (front and back) to this exam. There are 10 questions and 5 problems. There is also an optional extra credit problem. The points allocated to each question and each problem are as indicated. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If references to semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters: \( \mu_n C_{OX} = 100 \mu A/v^2 \), \( \mu_p C_{OX} = \mu_n C_{OX}/3 \), \( V_{TNO} = 0.5V \), \( V_{TPG} = -0.5V \), \( C_{OX} = 2fF/\mu^2 \), \( \lambda = 0 \), and \( \gamma = 0 \). If reference to a bipolar process is made, assume this process has key process parameters \( J_S = 10^{-15}A/\mu^2 \), \( \beta = 100 \) and \( V_{AF} = \infty \). Specify clearly what process parameters you are using in any solution requiring process parameters. Also attached to this exam is a table discussed in class that relates to the basic amplifier configurations.

1. (2pts) Why is the Q-point of a common source amplifier often placed near the middle of the load line?

2. (2pts) In terms of the small-signal model parameters, give the small-signal equivalent circuit of a diode-connected n-channel MOSFET

3. (2pts) In the Common Gate amplifier, why is the input on the source rather than on the drain?

4. (2pts) The cascode configuration is actually a cascade of two basic amplifier stages. In a bipolar process, what type of basic amplifier is the first stage of the cascode configuration?
5. (2pts) Part way through the design of an integrated circuit, the system was represented as an interconnection of a number of multiple-input NOR gates. At what level (Behavioral, Structural, or Physical) in the design hierarchy was the designer at with this interconnection of gates?

6. (2pts) There are many different desirable characteristics of a logic family but one is generally viewed as more important than all of the rest. Which is the most important?

7. (2pts) What is a standard cell library?

8. (2pts) Resistors and capacitors are widely used for biasing discrete bipolar amplifiers. What circuit element is most widely used in biasing integrated MOS integrated circuits?

9. (2pts) Consider a MOS transistor and a BJT transistor biased at the same current levels with the MOS device operating in the saturation region and the BJT operating in the forward active region. Circle the appropriate letter to indicate which of the following is true.
   a) The output impedance of the MOS transistor is much larger than that of the BJT
   b) The output impedance of the MOS transistor and the BJT are comparable
   c) The output impedance of the MOS transistor is much smaller than that of the BJT

10. (2 pts) Which of the basic bipolar amplifier structures has a low input impedance and a high output impedance?
Problem 1 (16 Pts.) Assume the capacitor in the following circuit is large.

a) Determine $W$ so that the quiescent drain voltage is 0V.

b) Parametrically determine the small-signal voltage gain in terms of the small-signal model parameters of the transistor and the resistors $R_1$ and $R_2$.

c) Numerically determine the small-signal voltage gain if the quiescent drain voltage is 0V.
Problem 2 (16 Pts.) Determine the voltage $V_{OUT}$.
**Problem 3** (16 Pts.) Assume the MOSFET and the BJT are biased to operate in the saturation region and the forward active region respectively. Obtain the amplifier two-port model for the following circuit in terms of the small signal model parameters of $Q_1$ and $M_2$. 
Problem 4 (16 Pts) Assume the capacitors in the following amplifier are large. Also assume the transistors are biased to that all BJT's are operating in the Forward Active region and all MOSFETs are operating in the saturation region.

a) Draw the small-signal equivalent circuit
b) Obtain an expression for the small-signal voltage gain in terms of the small-signal model parameters and the resistors in the circuit

\[ V_{OUT} = ? \]
\[ L = 1 \mu \]
\[ R_2 \]
\[ R_5 \]
\[ 10K \]
\[ R_1 \]
\[ W = ? \]
\[ L = 1 \mu \]
\[ M_1 \]
\[ Q_2 \]
\[ 10K \]
\[ Q_3 \]
\[ C_1 \]
\[ R_3 \]
\[ R_4 \]
\[ C_2 \]
\[ R_6 \]
\[ R_7 \]
\[ M_4 \]
\[ V_{IN} \]
\[ V_{OUT} \]
Problem 5 (16 Pts)  Assume the nonlinear three-terminal device in the circuit shown below is characterized by the equations

\[ I_1 = V_1 e^{2V_1} \]
\[ I_2 = 10V_1 + V_2 V_1^2 \]

a) Determine the small signal model in terms of \( V_{1Q} \) and \( V_{2Q} \).
b) Determine the Q-point for the circuit given below
c) Determine the small-signal voltage gain for the circuit given below
d) Give the total output voltage for the circuit given below if \( V_{IN} = 0.0002 \sin 500t \)
Problem 6 (15 pts extra credit) The detective problem! Assume you were told that the circuit shown in the shaded rectangle was part of a hardware Trojan embedded in a large IC and that the value for W/L and the resistor R are needed to fully understand how the Trojan works. Since the circuit was embedded, it was not possible to see what was inside the integrated circuit so a client decided to make electrical measurements to determine W/L and R. So, power was supplied with an 8V and -2V supply as indicated and the first thing that was measured was the dc power dissipation when the small signal input was 0. The power dissipation was 1mW. Then the small signal voltage gain was measured; it was -6. When a third measurement was attempted, the circuit self-destructed into a pile of “dust” so no additional measurements could be made. Determine R and W/L from the limited measurements that were made before the circuit self-destructed. Assume you know the circuit was fabricated in the process that has model parameters listed on the first page of this exam.
TRANSISTOR PARAMETERS W/L N-CHANNEL P-CHANNEL UNITS

<table>
<thead>
<tr>
<th>MINIMUM</th>
<th>3.0/0.6</th>
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<tbody>
<tr>
<td>Vth</td>
<td>0.78</td>
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<tr>
<td>SHORT</td>
<td>20.0/0.6</td>
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<tr>
<td>Idss</td>
<td>439</td>
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<tr>
<td>Vth</td>
<td>0.69</td>
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<tr>
<td>Vpt</td>
<td>10.0</td>
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<tr>
<td>WIDE</td>
<td>20.0/0.6</td>
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<tr>
<td>Ids0</td>
<td>&lt; 2.5</td>
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<tr>
<td>LARGE</td>
<td>50/50</td>
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<tr>
<td>Vth</td>
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<tr>
<td>Vjbkd</td>
<td>11.4</td>
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<tr>
<td>Ijlk</td>
<td>&lt;50.0</td>
</tr>
<tr>
<td>Gamma</td>
<td>0.50</td>
</tr>
<tr>
<td>K' (Uo*Cox/2)</td>
<td>56.9</td>
</tr>
<tr>
<td>Low-field Mobility</td>
<td>474.57</td>
</tr>
</tbody>
</table>

COMMENTS: XL_AMI_C5F

FOX TRANSISTORS GATE N+ACTIVE P+ACTIVE UNITS

| Vth | Poly | >15.0 | <-15.0 | volts |

PROCESS PARAMETERS N+ACTV P+ACTV POLY PLY2_HR POLY2 MTL1 MTL2 UNITS

| Sheet Resistance | 82.7 | 103.2 | 21.7 | 984 | 39.7 | 0.09 | 0.09 | ohms/sq |
| Contact Resistance | 56.2 | 118.4 | 14.6 | 24.0 | 0.78 | ohms |
| Gate Oxide Thickness | 144 | angstrom |

PROCESS PARAMETERS MTL3 N\PLY N_WELL UNITS

| Sheet Resistance | 0.05 | 824 | 815 | ohms/sq |
| Contact Resistance | 0.78 | ohms |

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS N+ACTV P+ACTV POLY POLY2 M1 M2 M3 N_WELL UNITS

| Area (substrate) | 429 | 721 | 82 | 32 | 17 | 10 | 40 | aF/um^2 |
| Area (N+active) | 2401 | 16 | 12 | aF/um^2 |
| Area (P+active) | 2308 | aF/um^2 |
| Area (poly) | 864 | 61 | 17 | 9 | aF/um^2 |
| Area (poly2) | 53 | aF/um^2 |
| Area (metal1) | 34 | 13 | aF/um^2 |
| Area (metal2) | 32 | aF/um^2 |
| Fringe (substrate) | 311 | 256 | 74 | 58 | 39 | aF/um |
| Fringe (poly) | 53 | 40 | 28 | aF/um |
| Fringe (metal1) | 55 | 32 | aF/um |
| Fringe (metal2) | 48 | aF/um |
| Overlap (N+active) | 206 | aF/um |
| Overlap (P+active) | 278 | aF/um |
Basic Amplifier Gain Table

<table>
<thead>
<tr>
<th></th>
<th>CE/CS</th>
<th>CC/CD</th>
<th>CB/CG</th>
<th>CEwRE/CSwRS</th>
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<tbody>
<tr>
<td><strong>A_v</strong></td>
<td>$-\frac{g_m R_C}{V_I}$</td>
<td>$-\frac{2\beta R_D}{V_{EB}}$</td>
<td>$\frac{2\beta R_E}{V_{EB}}$</td>
<td>$-\frac{R_C}{R_E}$</td>
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<tr>
<td><strong>r_{in}</strong></td>
<td>$r_m + \beta R_E$</td>
<td>$r_m + \beta R_E$</td>
<td>$r_m + \beta R_E$</td>
<td>$r_m + \beta R_E$</td>
</tr>
<tr>
<td><strong>R_{out}</strong></td>
<td>$R_C$</td>
<td>$g_m^{-1}$</td>
<td>$R_C$</td>
<td>$R_C$</td>
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Dc and small-signal equivalent elements

<table>
<thead>
<tr>
<th>Element</th>
<th>dce equivalent</th>
<th>sse equivalent</th>
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<tbody>
<tr>
<td>dc Voltage Source</td>
<td>$V_{dc}$</td>
<td>$V_{dc}$</td>
</tr>
<tr>
<td>ac Voltage Source</td>
<td>$V_{ac}$</td>
<td>$V_{ac}$</td>
</tr>
<tr>
<td>dc Current Source</td>
<td>$I_{dc}$</td>
<td>$I_{dc}$</td>
</tr>
<tr>
<td>ac Current Source</td>
<td>$I_{ac}$</td>
<td>$I_{ac}$</td>
</tr>
<tr>
<td>Resistor</td>
<td>$R$</td>
<td>$R$</td>
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