EE 330 Name_ _ _ _ _ _ _ _ _ _ _ _ _ _ _

Final Exam

Spring 2020

Due Wed May 6 at noon as upload in Canvas

Instructions: There are 10 questions and 8 problems. Two points allocated to each question and the problems are worth 10 points each. Please solve problems in the space provided on this exam. Attach extra sheets only if you run out of space in solving a specific problem. There is also one extra credit problem worth 10 additional points if solved correctly. This is listed as Problem Extra Credit.

If references to semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters; $\mu_n C_{OX}=350\mu A/V^2$, $\mu_p C_{OX}=70\mu A/V^2$,$V_{TNO}=0.5V$, $V_{TPO}= - 0.5V$, $C_{OX}=8fF/\mu^2$, $\lambda = 0.01V^{-1}$, and $\gamma = 0$. If reference to a bipolar process is made, assume this process has key process parameters for an npn transistor of $J_S=10^{-15}A/\mu^2$, $\beta_n=100$ and $V_{AFn} = \infty$ and those for a pnp transistor are $J_S=10^{-15}A/\mu^2$, $\beta_p=20$ and $V_{AFp} = \infty$. If any other process parameters are needed, use the process parameters associated with the process described in the attachments to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters.

Even though this is an open-book open-notes exam, several tables that may be of use are appended at the end of the exam should they be of use to you.

1. (2 pts) A vertical bipolar npn transistor can be viewed as a three-layer stack of doped semiconductor regions where the upper and lower layers are doped with n-type impurities and the middle layer is doped with p-type impurities where the doping density of one of the n-type regions is much larger than the other. Does the higher doping density n-type region correspond to the collector or the emitter of the transistor?

2. (2 pts) Though coupling and bypass capacitors are widely used when biasing discrete amplifier circuits, they are seldom used when biasing integrated amplifiers. Why are capacitors seldom used when biasing integrated amplifiers?

3. (2 pts) Explain what will happen if n-channel devices placed in PU network and p-channel devices placed in PD network.

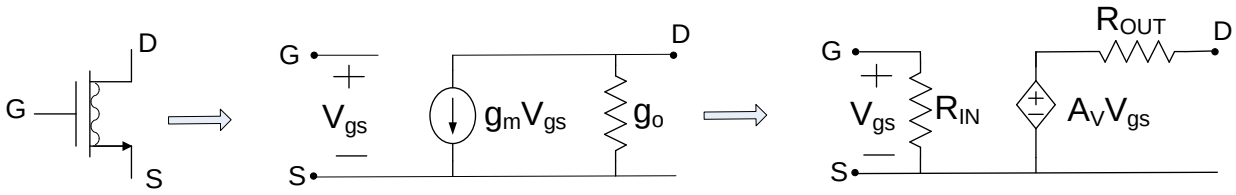
4. (2 pts) Which of the basic bipolar amplifiers has a very low input impedance?

5. (2 pts) Though CMOS logic is more practical in most applications, there are two major advantages of using nMOS logic rather than CMOS logic in some situations. Give one of them.

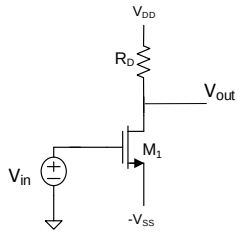
6. (2 pts) Dynamic logic is somewhat more complicated than static CMOS or ratio logic yet there can be a significant benefit from using dynamic logic in some applications. What is the major advantage dynamic logic offers in some applications?

7. (2 pts) The small-signal of the MOSFET that was derived from the square-law equation was characterized in terms of the small-signal parameters g_m and g_o as shown in the middle of the figure below. It can also be equivalently expressed in terms of the amplifier parameters as shown on the right. Express R_{IN}, A_V, and R_{OUT} in terms of the small-signal parameters g_m and g_o.

R_{IN} =_____ A_V =_____ R_{OUT} =_____



7. (2 pts) It was observed that the small parasitic capacitances in a MOS transistor affected the high frequency performance of amplifier circuits. For the common source amplifier shown, C_{DB}, the drain-bulk capacitance, caused the high frequency gain to drop. But one other parasitic capacitor prevented that gain from going to 0 at high frequencies. What parasitic capacitance prevented the high frequency gain from going to 0?



8. (2pts) Which region of operation in the Bipolar transistor corresponds to the triode region of operation in the MOS transistor?

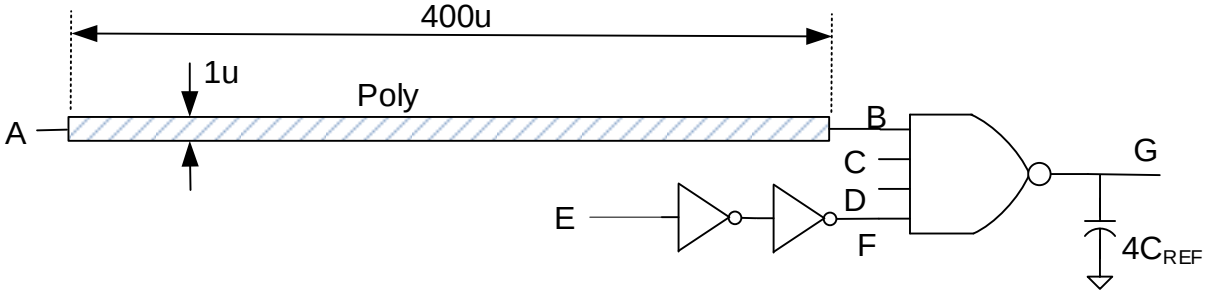
9. (2 pts) What region of operation were the two transistors of a CMOS inverter operating in when the analytical expression for the trip point of the inverter was derived?

10. (2 pts) A MOS transistor with W/L=50μ/1μ and a Bipolar transistor with emitter area of $50\mu^2$ are both biased to operate with a quiescent current of 1mA. Quantitatively compare the small signal trasconductance gain of these two devices.

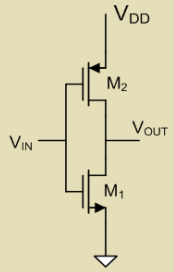
Problem 1 (10 pts) Assume Poly has a sheet resistance of 50Ω/□ and a capacitance density to substrate of $800aF/\mu m^2$. Assume all gates are sized for equal worst-case rise and fall times with OD=1. A reference inverter in this process is shown below. Assume the C and D inputs are both a Boolean 1.

a) If a low to high input transition occurs simultaneously on the A and E inputs, will the B input or the F input rise first? (Be quantitative in your comparison)

b) If the inputs A, C, and D are Boolean 1, calculate the propagation delay ($t_{HL}+t_{LH}$) from E to G.



Reference Inverter



Assume $\mu_n/\mu_p=3$

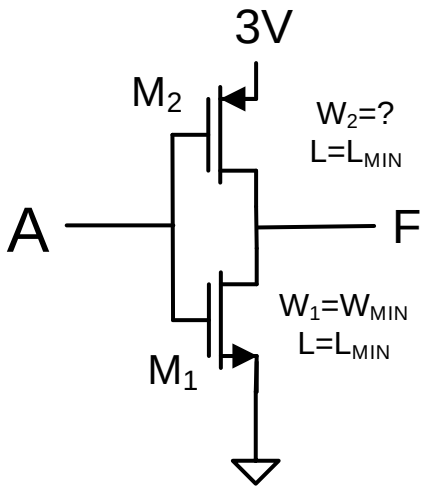
$W_n=W_{MIN}$, $W_p=3W_{MIN}$

$L_n=L_p=L_{MIN}$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

Problem 2 (10 pts) Consider the inverter shown below designed in a process $V_{THn}=-V_{THp}=0.8V$, $\mu_n C_{OX}=100\mu A/V^2$, $C_{OX}=2fF/\mu m^2$, $\mu_n/\mu_p=3$ and $L_{MIN}=W_{MIN}=0.4\mu m$.

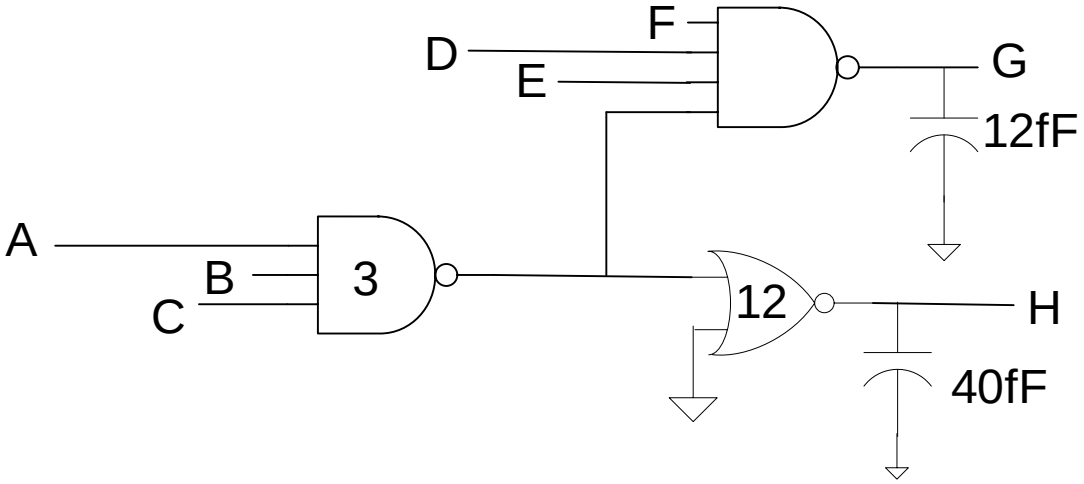
a) Determine W_2 so that the trip point of the logic circuit is at 1.5V
b) Derive the switch-level model for this inverter (including C_{IN}, R_{PU} and R_{PD})



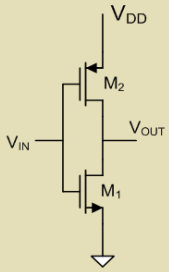
Problem 3 (10 pts) A simple logic circuit that is to be implemented in a standard CMOS process is shown below along with a reference inverter for this process.

a) Give the circuit schematic for the 3-input NAND gate including device sizing so that OD=3. Assume $W_{MIN}=L_{MIN}=0.5\mu m$.

b) Depending upon how the A,B,and C inputs change, the low-high output transition time for the 3-input NAND gate may change. Give the slowest and the fastest t_{LH} for the output of the 3-input NAND gate.



Reference Inverter



Assume $\mu_n/\mu_p=3$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

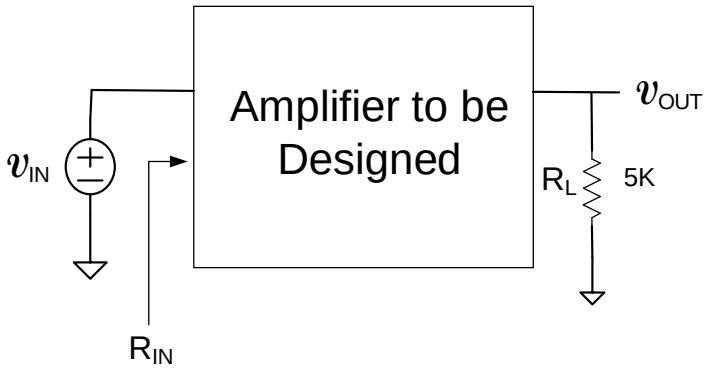
$L_n=L_p=L_{MIN}$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

Problem 4 (10 pts) Design an amplifier with the following properties:

- v_{IN} has one terminal referenced to ground
- A_V=16
- R_{IN}>20K
- R_L=5K has one terminal connected to ground (RL is the load resistor)

You may use any number of MOS and bipolar transistors, any number of dc voltage or current sources, and any number of capacitors. Specify the value of all components and include any necessary biasing for your amplifier

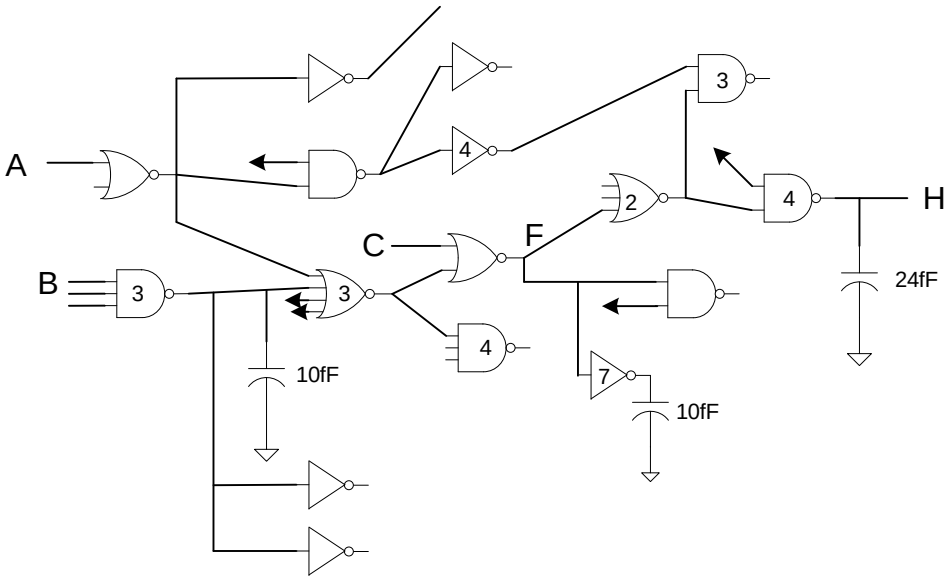


Problem 5 (10 pts) A segment of a logic block is shown below. Assume the lengths of all devices are L_{MIN}. Assume all gates are sized for equal worst-case rise and fall times. Gates with an overdrive factor that is different than 1 are as indicated by a number on the gate. Assume that the process in which these gates are fabricated is characterized by a minimum length reference inverter with

$$t_{REF}=20ps,\ C_{REF}=4fF,\ R_{PDREF}=2.5K$$

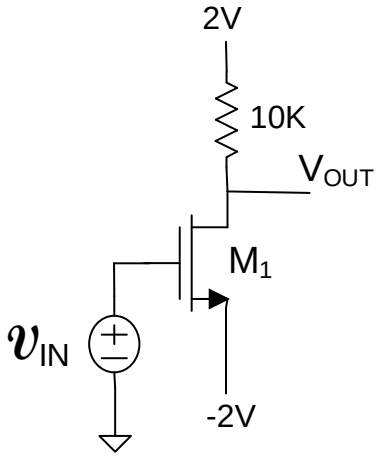
a) Determine the worst-case propagation delay from A to F

b) Repeat part a) if all gates are minimum sized.



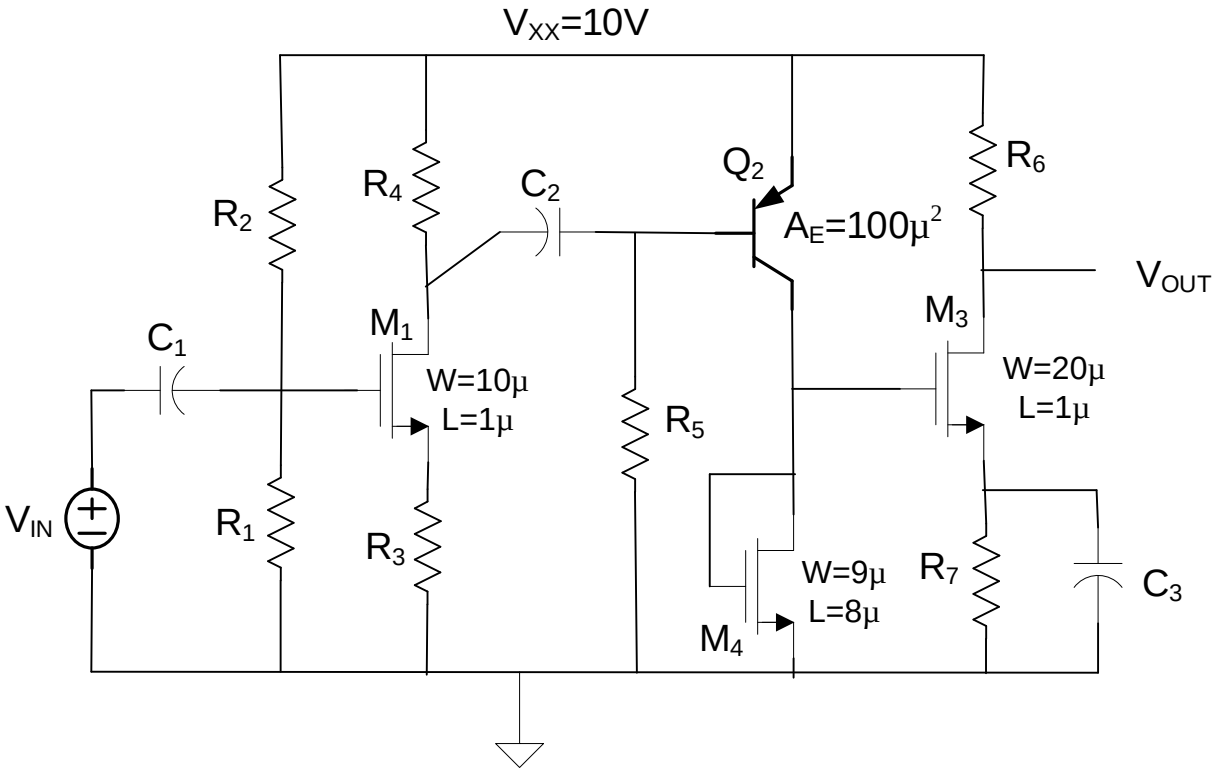
Problem 6 (10 pts) Consider the circuit shown below where v_{IN} is a small-signal input.

a) Determine W and L so that the quiescent output voltage is 1V.
b) Determine the small-signal voltage gain at the Q-point determined in part a) in terms of the small-signal model parameters of M_1
c) Numerically determine the small-signal voltage gain



Problem 7 (10 pts) Consider the amplifier block shown below. Assume all MOS transistors are operating in the saturation region and the BJT is operating in the forward active region. Assume the capacitors are all large.

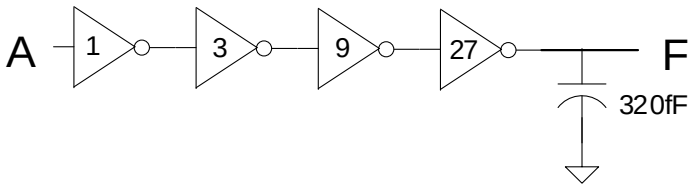
a) Draw the small-signal equivalent circuit of this amplifier
b) Determine the small-signal voltage gain in terms of the small-signal model parameters of the transistors and the components in the circuit
c) Determine the input impedance in terms of the model parameters of the transistors and the components in the circuit



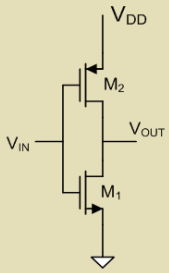
Problem 8 (10 pts) A four-stage pad driver is shown below. The inverters are sized for equal-worst-case rise/fall times with overdrive factors as indicated. A reference inverter for the process is also shown where V_{DD}=3V.

a) Determine the propagation delay of the signal from A to F.

b) Determine the dynamic power dissipation in the third stage (the stage with OD=9) if the input A is a 40MHz 3 Vp-p square wave.



Reference Inverter



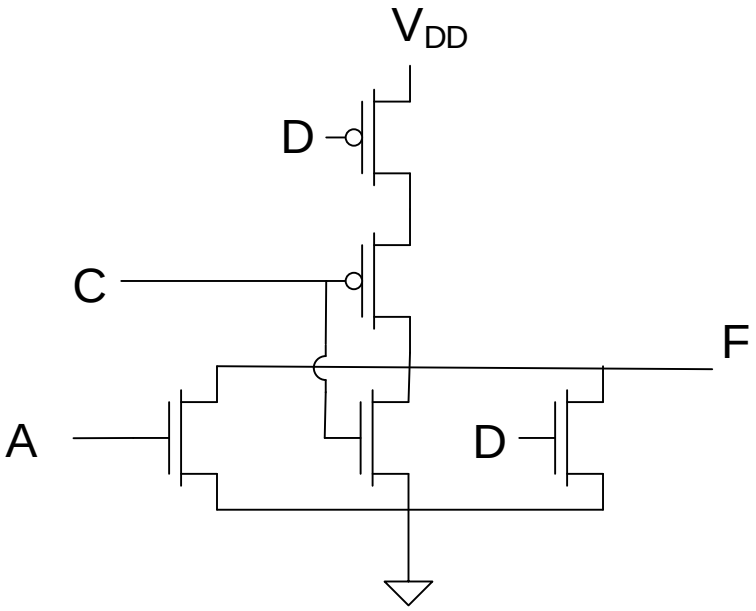
Assume $\mu_n/\mu_p=3$

$W_n=W_{MIN}$, $W_p=3W_{MIN}$

$L_n=L_p=L_{MIN}$

In 0.5u proc t_{REF}=20ps, C_{REF}=4fF, R_{PDREF}=2.5K

Problem Extra Credit (10 pts – Extra Credit) The following circuit has been proposed as a logic circuit. Will it work? If so, give the truth table. If not, explain why.



MOSIS WAFER ACCEPTANCE TESTS

RUN: T68B (MM_NON-EPI) VENDOR:
TSMC TECHNOLOGY: SCN018 FEATURE SIZE: 0.18 microns

COMMENTS: DSCN6M018_TSMC

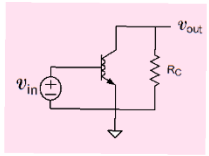
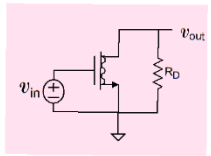
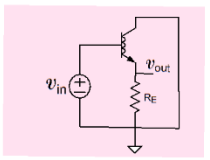
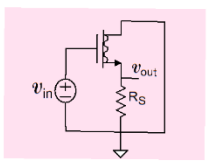
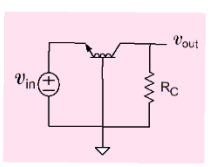
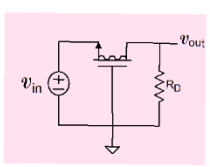
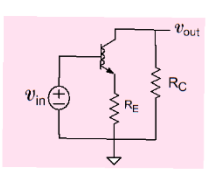
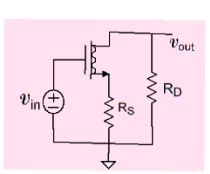
TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	0.27/0.18			
Vth		0.50	-0.51	volts
SHORT	20.0/0.18			
Idss		547	-250	uA/um
Vth		0.51	-0.51	volts
Vpt		4.8	-5.6	volts
WIDE	20.0/0.18			
Ids0		14.4	-4.7	pA/um
LARGE	50/50			
Vth		0.43	-0.42	volts
Vjbkd		3.1	-4.3	volts
Ijlk		<50.0	<50.0	pA
K' (Uo*Cox/2)		175.4	-35.6	uA/V^2
Low-field Mobility		416.52	84.54	cm^2/V*s

PROCESS PARAMETERS	N+	P+	POLY	N+BLK	PLY+BLK	M1	M2	UNITS
Sheet Resistance	6.7	7.8	8.0	59.7	313.6	0.08	0.08	ohms/sq
Contact Resistance	10.6	11.0	10.0				4.79	ohms
Gate Oxide Thickness	41							angstrom

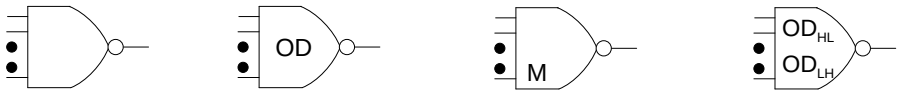
PROCESS PARAMETERS	M3	POLY_HRI	M4	M5	M6	N_W	UNITS
Sheet Resistance	0.08		0.08	0.08	0.03	930	ohms/sq
Contact Resistance	9.24		14.05	18.39	20.69		ohms

CAPACITANCE PARAMETERS	N+	P+	POLY	M1	M2	M3	M4	M5	M6	R_W	D_N_W	M5P	N_W	UNITS
Area (substrate)	942	1163	106	34	14	9	6	5	3		123		125	aF/um^2
Area (N+active)			8484	55	20	13	11	9	8					aF/um^2
Area (P+active)			8232											aF/um^2
Area (poly)				66	17	10	7	5	4					aF/um^2
Area (metal1)					37	14	9	6	5					aF/um^2
Area (metal2)						35	14	9	6					aF/um^2
Area (metal3)							37	14	9					aF/um^2
Area (metal4)								36	14					aF/um^2
Area (metal5)									34			984		aF/um^2
Area (r well)	920													aF/um^2
Area (d well)										582				aF/um^2
Area (no well)	137													aF/um^2
Fringe (substrate)	212	235	41	35	29	21	14							aF/um
Fringe (poly)			70	39	29	23	20	17						aF/um
Fringe (metal1)				52	34		22	19						aF/um
Fringe (metal2)					48	35	27	22						aF/um
Fringe (metal3)						53	34	27						aF/um
Fringe (metal4)							58	35						aF/um
Fringe (metal5)								55						aF/um
Overlap (N+active)		895												aF/um
Overlap (P+active)		737												aF/um

Basic Amplifier Gain Table

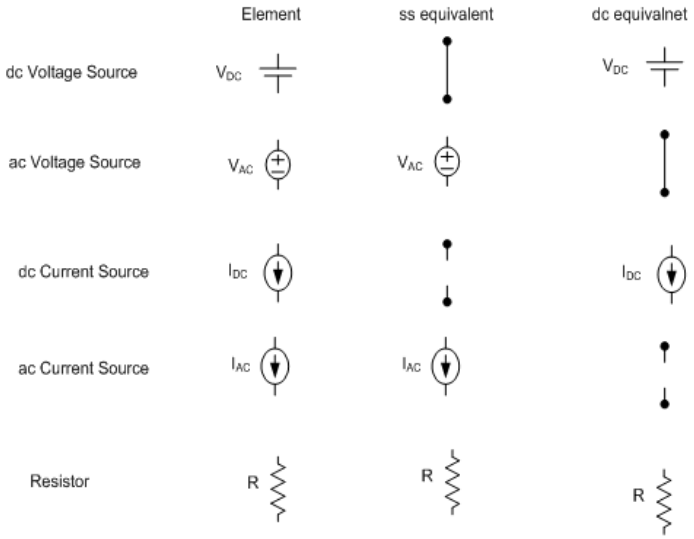
	CE/CS		CC/CD		CB/CG		CEwRE/CSwRS	
	BJT	MOS	BJT	MOS	BJT	MOS	BJT	MOS
								
A_V	$-g_mR_C$		$\frac{g_m}{g_m+g_E}$		g_mR_C		$-\frac{R_C}{R_E}$	
	$-\frac{I_{CQ}R_C}{V_t}$	$-\frac{2I_{DQ}R_D}{V_{EB}}$	$\frac{I_{CQ}R_E}{I_{CQ}R_E+V_t}$	$\frac{2I_{DQ}R_E}{2I_{DQ}R_E+V_{EB}}$	$\frac{I_{CQ}R_C}{V_t}$	$\frac{2I_{DQ}R_C}{V_{EB}}$		
R_{in}	r_π		$r_\pi+\beta R_E$		g_m^{-1}		$r_\pi+\beta R_E$	
	$\frac{\beta V_t}{I_{CQ}}$	∞	$\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$	∞	$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2I_{DQ}}$	$\beta\left(\frac{V_t}{I_{CQ}}+R_E\right)$	∞
R_{out}	R_C		g_m^{-1}		R_C		R_C	
			$\frac{V_t}{I_{CQ}}$	$\frac{V_{EB}}{2I_{DQ}}$				

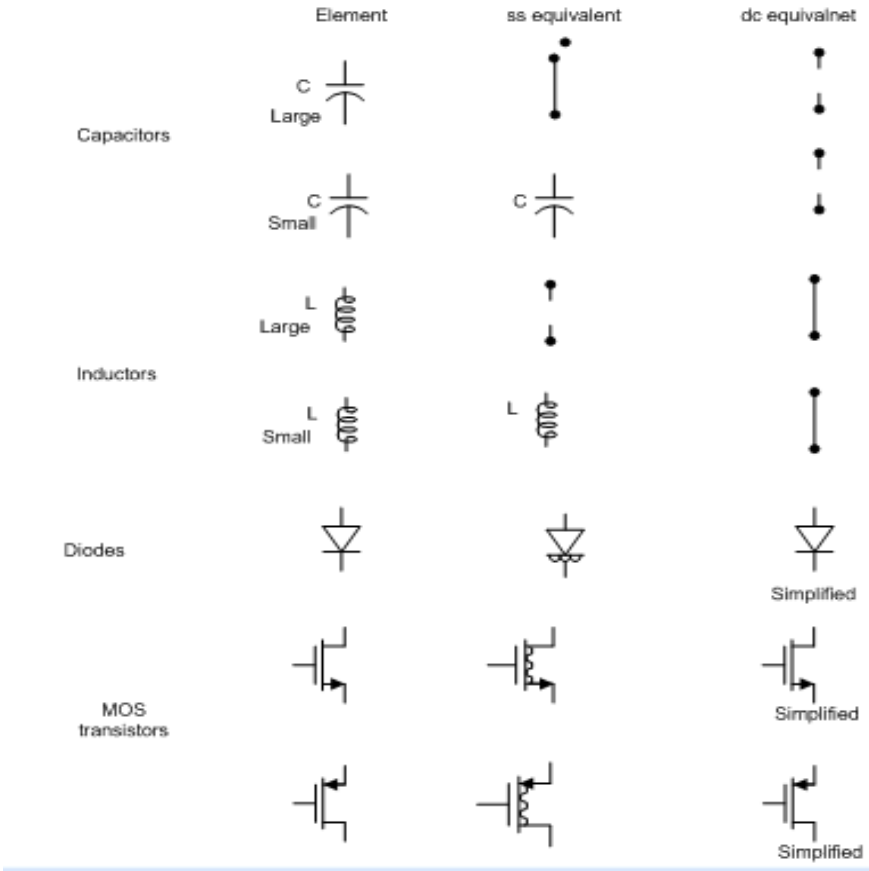
Propagation Delay in Logic Circuits with OD and Asymetry

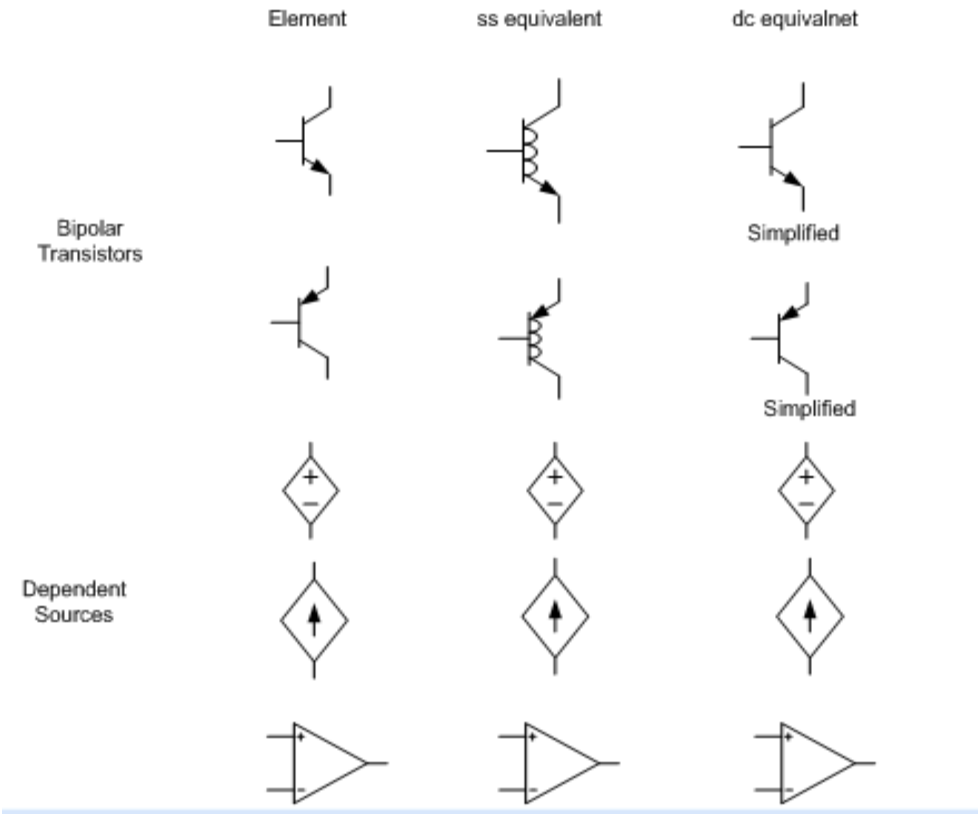


	Equal Rise/Fall	Equal Rise/Fall (with OD)	Minimum Sized	Asymmetric OD (OD_{HL}, OD_{LH})
C_{IN}/C_{REF}				
Inverter	1	OD	1/2	$\frac{OD_{HL}+3 \bullet OD_{LH}}{4}$
NOR	$\frac{3k+1}{4}$	$\frac{3k+1}{4} \bullet OD$	1/2	$\frac{OD_{HL}+3k \bullet OD_{LH}}{4}$
NAND	$\frac{3+k}{4}$	$\frac{3+k}{4} \bullet OD$	1/2	$\frac{k \bullet OD_{HL}+3 \bullet OD_{LH}}{4}$
Overdrive				
Inverter				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/3	OD_{LH}
NOR				
HL	1	OD	1	OD_{HL}
LH	1	OD	1/(3k)	OD_{LH}
NAND				
HL	1	OD	1/k	OD_{HL}
LH	1	OD	1/3	OD_{LH}
t_{PROP}/t_{REF}	$\sum_{k=1}^{n} F_{i(k+1)}$	$\sum_{k=1}^{n} \frac{F_{i(k+1)}}{OD_k}$	$\frac{1}{2}\sum_{k=1}^{n} F_{i(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$	$\frac{1}{2}\sum_{k=1}^{n} F_{i(k+1)}\left(\frac{1}{OD_{HLk}}+\frac{1}{OD_{LHk}}\right)$

Dc and small-signal equivalent elements




Element
ss equivalent
dc equivalnet
Capacitors
C
Large
C
Small
C
Inductors
L
Large
L
Small
L
Diodes
Simplified
MOS
transistors
Simplified
Simplified


Element
ss equivalent
dc equivalnet
Bipolar
Transistors
Simplified
Simplified
Dependent
Sources