Problem 1  The layout of a two-transistor MOS circuit is shown along with the connection of these transistors into a circuit. Assume the circuit is fabricated in the 0.5u AMI process described on the MOSIS WEB page and the process is characterized by the Parametric Test Results for the T17Z process run. Assume that the grid lines are all 0.3u apart.

a) Draw a circuit schematic for the resultant circuit

b) Determine the high-frequency small signal model for the lower device if Vxx and V_{YY} are determined so that I_{Z} = 300uA and V_{OQ}=2V (you may assume that all MOS devices are operating in the saturation region).
Problem 2 
Obtain $g_m$ and $g_0$ for the MOSFET shown. Assume the device is fabricated in a process with $\mu \lambda = 100 \mu A/V^2$, $V_T = 0.75 V$, $\lambda = 0.01 V^{-1}$, $\gamma = 0$ and $\phi = 0.6 V$.

Problem 3 
Capacitors are often made by stacking two conducting layers and using the insulator between the layers as a dielectric. There are several ways to make a capacitor following this approach and both the required area and performance is affected by how this is achieved.

a) Design a Poly-Poly capacitor in the 0.5u AMI process (T17Z process run) that has a nominal capacitance of 600fF. What is the area required for this capacitor?

b) Design a Metal 1-Metal 2 capacitor in the 0.5u AMI process (T17Z process run) that has a nominal capacitance of 600fF. What is the area required for this capacitor? How does that compare (i.e. what percent difference) to that required for the Poly-Poly capacitor?

c) Several layers can be stacked to increase the capacitance density by electrically connecting the resultant capacitors in parallel (alternating conducting layers are connected to form a node). Design a stacked Poly 1, Poly 2, Metal 1, Metal 2, Metal 3 capacitor in the 0.5u AMI process (T17Z process run) that has a nominal capacitance of 600fF. What is the area required for this capacitor? How does that compare (i.e. what percent difference) to that required for the Poly-Poly capacitor?

d) Sometimes the gate oxide capacitance of a transistor is used to form a capacitor. These capacitors are often termed MOSFET capacitors with one plate being the gate and the other plate being the source which is connected to the drain. The capacitance density of these capacitors is $C_{OX}$. Although there is a requirement that such capacitors have a dc voltage in excess of $V_T$ across them to form the inversion layer in the channel, many applications already have this bias. Design a MOSFET capacitor in the 0.5u AMI process (T17Z
process run) that has a nominal capacitance of 600fF. What is the area required for this capacitor? How does that compare (i.e. what percent difference) to that required for the Poly-Poly capacitor?

e) Design a stacked MOSFET, Poly1, Poly2, Metal 1, Metal 2, Metal 3 capacitor in the 0.5u AMI process (T17Z process run) that has a nominal capacitance of 600fF. What is the area required for this capacitor? How does that compare (i.e. what percent difference) to that required for the Poly-Poly capacitor?

Problem 4 Obtain the small signal equivalent circuit for the following circuit. Assume all capacitors are large, all inductors are large, and all transistors are operating in the saturation region. You do not need to solve the circuit. Determine the small signal model for the device at the operating point $V_1 = 2V$, $V_2 = 0.25V$.

Problem 5 The quiescent output voltage in the amplifier shown is to be between 1V and 3V. Size the transistor to maximize the voltage gain. Assume the device is fabricated in a process with $\mu C_{OX} = 100uA/V^2$, $V_T = 0.75V$, $\lambda = 0.5V^{-1}$, $\gamma = 0$ and $\phi = 0.6V$. 