EE 330
Assignment 13
Spring 2017
Since there will be an in-class exam on Friday April 14, this assignment will not be collected or graded.

If references to a semiconductor processes are needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters: \( \mu_nC_{OX}=100\mu A/V^2 \), \( \mu_pC_{OX}=\mu_nC_{OX}/3 \), \( V_{TNO}=0.5V \), \( V_{TPO}=-0.5V \), \( C_{OX}=2fF/\mu^2 \), \( L_{MIN}=W_{MIN}=0.5\mu \), and \( V_{DD}=3.5V \) and a bipolar process is available with model parameters \( J_s=10^{-14}A/\mu^2 \), \( \beta_n=100 \) and \( \beta_p=40 \). The output conductance of the BJT and the MOSFET are characterized, respectively, by \( V_{AF}=100V \) and \( \lambda=.01V^{-1} \).

**Problem 1**  
Assume the biasing voltages have been selected so that the quiescent output voltage is 3V and that all transistors are operating in the forward active region. Determine the small-signal voltage gain. Assume \( A_{E1}=A_{E2}=A_{E3}=100\mu^2 \).

![Diagram of a circuit with labels Q1, Q2, VCC=6V, VOUT, VN=VSS, VSS, VOUT, VCC=6V, Q3, VZZ, VCC=6V, Q4.](attachment:diagram.png)

**Problem 2**  
Assume the biasing voltages have been selected so that the quiescent output voltage is 3V and that all transistors are operating in the forward active region. Determine the small-signal voltage gain. Assume \( A_{E1}=A_{E2}=A_{E3}=A_{E4}=100\mu^2 \).

![Diagram of a circuit with labels Q1, Q2, VCC=6V, VOUT, VN=VSS, VSS, VOUT, VCC=6V, Q3, VZZ, VCC=6V, Q4.](attachment:diagram.png)

**Problem 3**  
If a DC input voltage of 1uV is placed in series with \( V_{IN} \) in the previous circuit, how much change in the output voltage from the quiescent value of 1V can be expected? Comment on the implications of this observation.

![Diagram of a circuit with labels Q1, Q2, VXX, VIN, VSS, VOUT, VYY, VCC=6V, Q3, VZZ, Q4.](attachment:diagram.png)
**Problem 4**  A standard CMOS inverter is shown below. If the devices are sized so that $W_1=W_2=1\mu$, $L_1=L_2=1\mu$, determine the trip point if $V_{DD}=3.5V$.

![CMOS Inverter Diagram](image)

**Problem 5**  What percent deviation in the trip point voltage for the circuit of Problem 4 will occur if the magnitude of the n-channel threshold voltage decreases by 20% and the magnitude of the p-channel threshold voltage increases by 20% from the nominal value?

**Problem 6**  Give all of the two-input Boolean functions and identify which of those are useful or are actually used.

**Problem 7**  A physical layer implementation of a circuit at the layout level is shown below where blue denotes metal, red polysilicon, and green n-active, yellow p-active, brown n-well and black contacts. Assume the upper metal rail is a VDD pin, the lower metal rail is ground, the middle left metal is Boolean input A, and the middle right metal is Boolean output B.

a) Give a physical layer view of this layout at the circuit schematic level. Assume the contact sizes are $2\lambda \times 2\lambda$.

b) Give a structural layer view of this layout at the gate level.

![Physical Layer Layout](image)

**Problem 8**  The small-signal equivalent circuit of a common emitter amplifier is shown below. If the emitter area of the BJT is $100\mu^2$ and the load resistor $R_L$ is 2K, bias this circuit so that the quiescent output voltage is 5V and the DC voltage across $R_L$ is also 5V while maintaining the same small signal gain that this circuit has. You have one dc power supply available of any value you choose and any number of resistors and capacitors.

![Common Emitter Amplifier Diagram](image)
**Problem 9**  Consider the following circuit.

a) Determine an analytical expression that relates $I_{OUT}$ to $I_{IN}$

b) With a computer simulation, plot the relationship between $I_{OUT}$ and $I_{IN}$ as $I_{IN}$ is varied between -40µA and +40uA.

![Circuit Diagram]

**Problem 10**  A Boolean System is supposed to have an output $F$ that is high when the Boolean inputs $A$ and $B$ are high or when the inputs $C$ and $D$ are high and $E$ is low or when the input $A$ is low and the input $E$ is high.

a) Give a behavioral description of this system in terms of the input/output variables $A,B,C,D,E,$ and $F$.

b) Write Verilog code describing this system at the behavioral level

c) Give a gate-level structural description of this system if the only gates that are NOR gates with any number of inputs

d) Write Verilog code describing this system at the gate level

e) Give a transistor-level physical description of this system. You may use any logic style you are familiar with. You need not size the devices

**Problem 11** Give two distinct structural implementations at the gate level of a system with the following Behavioral Description: The output $F$ is high when $A$ is high and $B$ is high or when $C$ is low and $B$ is low. Otherwise the $F$ output is low.