EE 330

Homework 2 Solutions Fall 2022

1)

DRC stands for Design Rule Checking and ensures that all the dimensional tolerances involved within a given process are followed within a layout. For example, if two metal1 interconnects are placed too close to each other, DRC would find that the two interconnects are less than minimally spaced. This tool does not check that correct connections are made, just that the layout meets dimensional rules and manufacturing tolerances.

LVS stands for Layout VS Schematic and ensures that all electrical connections made within a given layout are identical to electrical connections made within a given schematic. For example, if an NMOS gate is tied to an input A in the layout but is tied to an input B within the schematic, the LVS tool would find that the NMOS gate is tied to a different input between the schematic and the layout. This tool does not check that any dimensional rules or manufacturing tolerances are met, just that connections between the layout and schematic are correct.

2)

Wafer area = $\pi r^2 = \pi(22.5cm)^2 = 1590.43cm^2$

Dies/Wafer (ignoring edge cases) = $\frac{1590.43cm^2}{0.5cm^2} = 3180.86 \sim 3180 \frac{dies}{wafer}$

Ideal cost per die = $\frac{\$3000}{3180\ dies} = \$0.94$

Yield = $\frac{Ideal\ cost\ per\ die}{Cost\ per\ die} = \frac{\$0.94}{\$3.00} = 31.33\%$

3)

Die area = $(side\ length)^2 = (6mm)^2 = (0.6cm)^2 = 0.36cm^2$

Hard yield = $Y_H = e^{-Ad} = e^{-(0.36cm^2)(1.5cm^{-2})} = 58.27\%$

Total yield = $Y = Y_H Y_S = (58.27\%)(100\%) = 58.27\%$

Dies/wafer (ignoring edge cases) = $\frac{Wafer\ area}{Die\ area} = \frac{\pi(150mm)^2}{(6mm)^2} = 1962.5 \sim 1963\ dies/wafer$

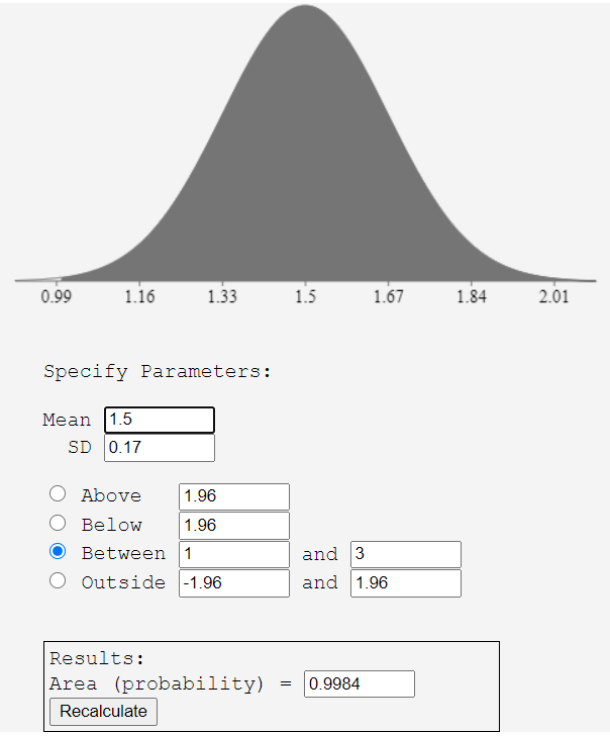
Good Dies/wafer = $(1963\ dies\ wafer) * (.5827) = 1143.8 \sim 1144\ good\ dies/wafer$

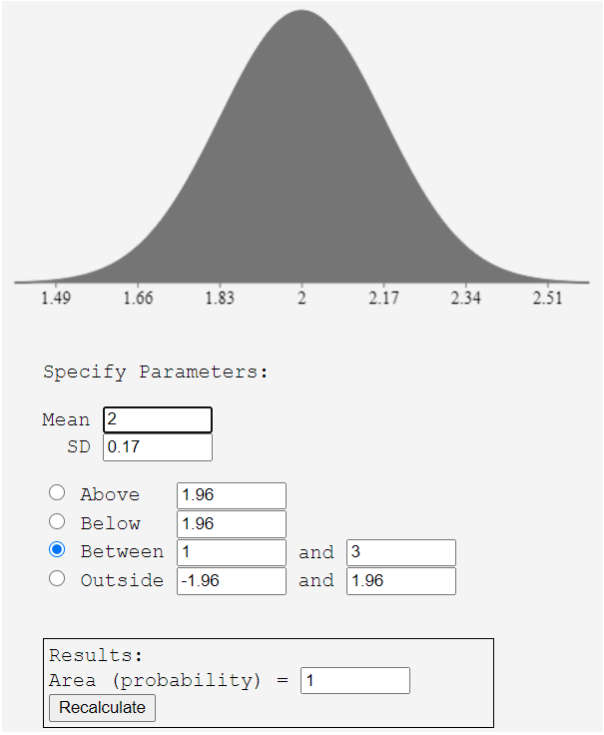
Cost per good die = $\frac{Cost\ per\ wafer}{number\ of\ good\ dies} = \frac{\$3200}{1144\ dies} = \$2.797$

4)

Using a normal distribution calculator

https://onlinestatbook.com/2/calculators/normal_dist.html





5)

14nm transistor gate area $= (14nm)^2 = 196nm^2$

14nm transistor total area = $area * overhead = area * 10 = 1960nm^2 = 1.96 * 10^{-11}cm^2$

Transistors per die = $\frac{Die\ Area}{Transistor\ Area} = \frac{0.25cm^2}{1.96*10^{-11}cm^2} = 1.276 * 10^{10}\ \frac{transistors}{die}$

New transistor area = $(3nm)^2 * overhead = 9nm^2 * 10 = 90nm^2$

New die area = $\frac{transistors}{die} * transistor\ area = 1.276 * 10^{10} * 90nm^2 = 1.148mm^2$

New dies/wafer (ignoring edge cases) = $\frac{Wafer\ Area}{Die\ area} = \frac{\pi(225mm)^2}{1.148mm^2} = 138539\ dies$

6)

a) Expected hard yield = $Y_H = e^{-Ad} = e^{-(0.85mm^2)(1cm^{-2})} = e^{-(0.0085cm^2)(1cm^{-2})}$

$Y_H = e^{-0.0085} = 0.9915 = 99.15\%$

b) Expected overall yield = $Y_{overall} = Y_H Y_S = (0.9915)(0.99)$

$Y_{overall} = 0.9815 = 98.15\%$

c) As spec'd, this ADC is suitable to be produced at the fab location, as expected overall yield is greater than the 95% yield limit. To find maximum allowable ADC area to stay within 95% yield limit, derive an equation relating ADC area to yield, with $Y_{overall} = 0.95$.

$$Y_{overall} = Y_S Y_H = Y_S e^{-(die\ area\ cm^2)(1cm^{-2})}$$

$$die\ area\ cm^2 = \frac{\ln\left(\frac{Y_{overall}}{Y_S}\right)}{-1cm^{-2}} = \frac{-0.04124}{-1cm^2} = 0.04124cm^2 = \ 4.124mm^2$$

7)

Probability that one operational amplifier meets the offset voltage criteria

$$\mu = 0V, \sigma = 3mV$$

$$P(1\ Good\ op\ amp) = \left(2 * F_N\left(\frac{5mV - 0mV}{3mV}\right) - 1\right)$$

$$P(1\ Good\ op\ amp) = \left(2 * F_N(1.66)\right) - 1)$$

$$P(1\ Good\ op\ amp) = (2 * .9515) - 1 = 1.903 - 1 = 0.903$$

Probability that both operational amplifiers meet the offset voltage criteria

$$P(2\ Good\ op\ amps) = P(1\ Good\ op\ amp) * P(1\ Good\ op\ amp)$$

$$P(2\ Good\ op\ amps) = 0.903 * 0.903 = 0.8154$$

The probability that there is an IC with both operational amplifiers meeting the offset voltage requirements with the given standard deviation and mean is 0.8154. This gives us a soft yield of 81.54%.

8)

/*implementation of HW 2 problem 8

2 specified gates included in code

switch between code with en input

en=0 -> 3-in nor

en=1 -> 2-in nand, doesnt use C

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```
`timescale 1ns/1ps                    //give us a nice timescale for simulation

module hw2q8(A, B, C, En, F);         //instantiate the module
input A, B, C, En;                    //define inputs
output F;                             //define output
reg Out;                              //define placeholder reg for use in always block
assign F = Out;                       //assign placeholder reg to output
always @ (A or B or C or En) begin    //any time an input changes
```

```
if (!En) begin                  //if enable is zero
Out = ~(A||B||C);       //F=!(A+B+C)
end                             //exit if statement
if (En) begin                   //if enable is one
Out = ~(A&B);           //F = !(A&B)
end                             //exit if statement
end                                     //exit always statement
endmodule                               //end of module
/*standard 4-input logic testbench
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`timescale 1ns/1ps                              //set timescale to something nice to simulate

module standard_tb();                           //instantiate testbench module
reg a,b,c,en;                                   //define input registers
wire out;                                       //define output wire
hw2q8 DUT(.A(a), .B(b), .C(c), .En(en), .F(out));   //instantiate Device Under Test
initial a = 0;                                  //set initial input values
initial b = 0;
initial c = 0;
initial en = 0;
always  #1 a = ~a;                              //for input n, toggle every 2^n time units
always  #2 b = ~b;
always  #4 c = ~c;
always  #8 en = ~en;
```

endmodule //end testbench module