Problem 1:

\[ Y = (AB + C)\overline{D} \]

One possible design with static CMOS gates,

This design uses **16 transistors**.

The below is one design for a compound CMOS gate

This design uses **8 transistors**
Problem 2:

\[ Y = \overline{AB} + AB \]

Problem 3:

For minimum sized 2 input NAND,

\[
R_{SWN} = 2k\Omega, R_{SWP} = 6k\Omega, C = 40fF
\]

\[
T_{HL} = 2 \times R_{SWN} \times C = 4k \times 40f = 160 \times 10^{-12} \text{ seconds} = 160 \text{ pS}
\]
Problem 4
Problem 5

The second inverter is combined with the transmission gate, rather than two separate components.

Problem 6
Problem 7

There should not be a contact between B and $N_{\text{active}}$

$N_{\text{active}}$ region is missing one contact with $V_{SS}$

There should be a contact between Y and $P_{\text{active}}$

The metal contact between A and B that connects $N_{\text{active}}$ and $V_{SS}$ needs to be removed.

Problem 8

a) $R_{W,\text{Aluminum}} = \frac{2.8 \times 10^{-8}}{0.2 \times 10^{-6}} \times \frac{180}{5} + \frac{2.8 \times 10^{-8}}{0.2 \times 10^{-6}} \times \frac{40 - 5}{5} = 6.02 \Omega$

$V_{\text{wire}} = 5 \times \frac{6.02}{100 + 6.02} = 283.9 \text{ mV}$

$V_{\text{Resistor}} = 5V - V_{\text{wire}} = 5 - 0.2839 = 4.716 V$

b) $R_{W,\text{Copper}} = 3.655 \Omega$

$V_{\text{wire}} = 5 \times \frac{3.655}{100 + 3.655} = 0.176 V$

$V_{\text{Resistor}} = 5V \times \frac{100}{100 + 3.655} = 4.824 V$

c) $V_{RW} < 5V \times 5\% = 0.25V$

$5V \times \left( \frac{R_W}{100 + R_W} \right) < 0.25V \Rightarrow R_W < 5.263 \Omega$

$R_W = 6.02 \times \frac{5 \mu m}{\text{Width}_{\text{wire}}} \Rightarrow \text{Width}_{\text{wire}} \geq 5.72 \mu m$

Problem 9:

Each inverter has $C_L = 1.5 \text{ fF} + 1.5 \text{ fF} = 3 \text{ fF}$

total load capacitance $C = 3 \text{ pF} \times 16 = 48 \text{ fF}$

$R_{SWp} = 6k\Omega \Rightarrow T_{LH} = 6k \times 48 f = 288 \times 10^{-12}S = 288 \text{ pS}$
Problem 10

Mux4to1 code

```
module MUX4to1(A, B, C, D, s1, s2, out);
input [3:0] A, B, C, D;
input s1, s2;
output [3:0] out;
reg [3:0] o;
assign out = o;
always @(*) begin
  if(s1 == 0) begin
    if(s2 == 0) begin
      o <= A;
    end
    else begin
      o <= C;
    end
  end
  else begin
    if(s2 == 0) begin
      o <= B;
    end
    else begin
      o <= D;
    end
  end
endmodule
```

Test bench Code

```
module MUX_th();

reg [3:0] A, B, C, D;
reg s1, s2;
wire [3:0] out;
MUX4to1 mux(A(A), B(B), C(C), D(D),
            s1(s1), s2(s2), out(out));
initial begin
  A = 4'd0001;
  B = 4'd0010;
  C = 4'd0110;
  D = 4'd1100;
  s1 = 0;
  s2 = 0;
end
always #20 s1 <= ~s1;
always #20 s2 <= ~s2;
endmodule
```
Simulation results

<table>
<thead>
<tr>
<th>Port</th>
<th>Value</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>MUX_in1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>MUX_in2</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>MUX_in3</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>MUX_in4</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>MUX_out</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Time: 90000 ps

Cursor 1: 87243 ps