Problem 1

Assume BJT works in forward active region

\[ I_B = \left(\frac{10 - 0.6}{500k}\right) = 18.8\mu A \]

\[ I_C = \beta I_B = 100 \times 18.8\mu A = 1.88mA \]

\[ V_C = 10 - 4000 \times 0.00188 = 2.48V \]

\( V_{out} = 0V \) (there is a capacitor creating an open circuit in DC.)

Small signal equivalent circuit:

Problem 2

For the MOSFET to be in saturation \( V_{DS} \geq V_{GS} - V_T \)

\[ V_{out} + 2 \geq 2 - 0.5 \rightarrow V_{out} \geq -0.5 \]

\[ I_D = \frac{\mu n C_{OX} W}{2L} (V_{GS} - V_T)^2 = \frac{4 - V_{out}}{R_1} \rightarrow V_{out} = 4 - 3.375 \times 10^{-3} \times R_1 \geq -0.5V \]

\( \rightarrow R_1 \leq 13.3k\Omega \)

Problem 3

\[ R_1 = 6.666k\Omega \]

\[ A_V = \frac{2I_{DQ} R}{V_{SS} - V_T} = -\frac{1.5V}{V} \]
Problem 4

Assuming that $M_1$ and $M_2$ are in saturation

$$I_{D_1} = I_{D_2} = \mu_n C_{OX} W_n (V_{GS} - V_T)^2 = \frac{\mu_n C_{OX} W_n}{2L_n} (V_{GS} - V_T)^2$$

$$I_D = 1 mA \rightarrow V_{out} = 0.96447 V$$

Problem 5

a) For quiescent values that capacitors act as open circuits, so the voltage is simply,

$$V_{CQ} = 32 - \left( \frac{3.2 - 0.6}{1.5k} \right) 1.7k = 26.8 V$$

$$V_{out} = 0 V$$

b)
Problem 6

\[ V_{out} = 12 - (12000 \times i_{DQ}) \]

\[ I_{DQ} = 100 \times 10^{-6} \times \left( \frac{6}{2 \times 4} \right) \times (0 - (-2) - 1)^2 \]

\[ I_{DQ} = 75 \mu A \]

\[ V_{out} = 11.1V \]

Problem 7

a)

\[ I_{DQ} = 100 \times 10^{-6} \times \left( \frac{6}{2 \times 3} \right) (2 - 1)^2 \]

\[ I_{DQ} = 10 \mu A \]

\[ V_{outq} = 4 + 10 \mu \times 20k = 5V \]

b)

When \( V_{in} = 0V, V_{out1} = V_{outQ} = 5V \)

When \( V_{in} = 25mV, V_{out2} = V_{outQ} + \Delta V \)

\[ g_m = 100 \times 10^{-6} \left( \frac{6}{3} \right) (1) = \frac{20 \mu A}{V} \]

\[ \Delta V = (g_m \times \Delta V_{in}) \times 20k = 0.1V \]

\[ V_{out2} = 5.1V \]

Problem 8

\[ R_{FET} = \frac{1}{\mu_n C_{OX} \left( \frac{L}{W} \right)} \]

\[ \frac{V_{out} - V_{in}}{R_F} = \frac{V_{in}}{R_{FET}} \]

\[ V_{out} = 1 + \frac{R_F}{R_{FET}} \]

\[ \frac{V_{out}}{V_{in}} = \frac{1 + \mu_n C_{OX} \left( \frac{W}{L} \right) \times R_F}{V_{in}} \]
Problem 9

a) \[ \frac{I_{E1}}{I_{E2}} = \frac{A_{E1}}{A_{E2}} = \frac{1}{4} \]

\[ I_B = I_{B1} + I_{B2} = \frac{5}{4} I_{B1} \]

\[ I_{B1} = I_{C1} + \beta I_{C1} = \beta I_{B1} + \frac{5}{4} I_{B1} \]

\[ I_{B1} = I_{in} \left( \frac{1}{\beta + \frac{5}{4}} \right) \rightarrow I_{out} = \beta I_{B2} = \beta \times 4I_{B1} = I_{in} \left( \frac{4}{1 + \frac{5}{4}} \right) \]

Assuming that \( \beta \) is large \( \rightarrow I_{out} = \frac{5}{4} I_{in} = \frac{5}{4} mA \)

b) \[ \frac{I_{D1}}{I_{D2}} = \frac{W_2}{L_2} \frac{W_1}{L_1} = \frac{10}{50} = \frac{1}{5} \]

\[ I_{out} = 5I_{in} = 0.2mA \]

Problem 10

BJT: \( I_{out} = \frac{A_{E2}}{A_{E1}} I_{in} \)

MOSFET: \( I_{out} = \frac{W_1}{L_1} \frac{W_2}{L_2} I_{in} \)

Problem 11

At the basics, \( I_d = \mu C_{ox} \left( \frac{w}{2L} \right) (V_{gs} - V_T)^2 \), and all three have the same total length and width. As that the length/width is the one degree of freedom we have to modify the MOSFET they should behave the same.

Problem 12

As this circuit is a 1-port small signal model it acts as a resistor.

\[ R_{ss} = \frac{V_{DQ}}{I_{DQ}} \]

\[ V_{DQ} = 2V \rightarrow I_{DQ} = 30.6mA \]

\[ R_{ss} = \frac{2}{0.0306} = 65.4 \Omega \]
Problem 13

Yes, this does behave as a rectifier, but it does not work particularly well. It is “Diode Connected” and behaves as a diode, but it’s I-V curve is not as good as the standard diodes used in class, but may be better than some LEDs.

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As always, we will assume we are operating in saturation region,

\[ I_D = \mu_n C_{ox} \left( \frac{W}{2L} \right) (V_{gs} - V_T)^2 = \frac{V_{dd} - V_{out1}}{R_1} \]

\[ I_D = \frac{(4 - 3)}{10k} = 0.1mA \]

\[ 100 \times 10^{-6} \times \left( \frac{W}{2L} \right) (2 - 1)^2 = 0.0001 \]

\[ \frac{W}{2L} = 1 \rightarrow W = 2L \]

\[ W = 0.6\mu, L = 0.3\mu \]

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Using Behavioral Verilog,

```
`timescale 1ns/1ps
module Counter4bit (S, CLK, Count);

input S, CLK;
output [3:0] Count;
reg [3:0] Count;

initial
Count = 4'b0000;

always@(posedge CLK) begin
  if(S)
    assign Count = Count-1;
  else
    assign Count = Count+1;
end

endmodule
```
module CounterTB ();
    reg S, CLK;
    wire [3:0] Count;

Counter4bit count1(.S(S), .CLK(CLK), .Count(Count));

initial
begin
    S = 1'b0;
    CLK = 1'b0;
end

always
    #1 CLK = ~CLK;
always
    #40 S = ~S;

endmodule