This homework assignment will not be collected or graded. Unless stated to the contrary, assume all MOS transistors have model parameters $\mu_n C_{OX} = 100 \mu A/V^2$, $V_{Th} = 1V$, $\mu_n/\mu_p = 3$, $V_{Tp} = -1V$ and all BJT transistors have model parameters $J_S A = 10^{-12} A$, $\beta_n = 100$, and $\beta_p = 30$.

Problem 1  
Assume the capacitors are very large.

a) Draw the small signal equivalent circuit for the amplifier shown
b) Determine the quiescent value of $V_C$ and $V_{OUT}$
c) Obtain the small-signal voltage gain
d) Determine the small-signal output voltage $V_{OUT}$ if $V_M = 200 \mu V$
e) What would be the output voltage be if $V_M = 200 mV$?

Problem 2  
a) Determine the maximum value of $R_1$ that will keep $M_1$ in saturation. $M_1$ has dimensions $W=12 \mu$ and $L=2 \mu$ and is in a process with $\mu_n C_{OX} = 100 \mu A/V^2$, $\mu_p C_{OX} = 30 \mu A/V^2$, $V_{TNO} = 0.5V$, $V_{TPO} = -0.5V$, $C_{OX} = 2fF/\mu^2$, $\lambda = 0$, $\gamma = 0$.
b) If $R_1$ is $1/3$ of the value determined in Part a), determine the small signal voltage gain of this circuit
c) With the value of $R_1$ used in part b), determine the total output voltage if $V_{IN}(t) = .001 \sin(5000t + 75^\circ)$.

Problem 3  
Obtain an expression for the small signal output voltage in terms of the small signal parameters if the input is given by the expression $V_{IN}(t) = V_M \cos(\omega t + \theta)$. Assume $M_1$ is operating in the saturation region.
Problem 4  Determine the total output voltage for the circuit in Problem 3 if $V_{DD}=5\text{V}$, $V_{SS}=-2\text{V}$, $W_1=15\text{u}$, $L_1=2\text{u}$, $W_2=4.5\text{u}$ and $L_2=1\text{u}$. Assume the devices are from a process with parameters $\mu_{n}C_{OX}=100\mu\text{A}/\text{v}^2$, $\mu_{p}C_{OX}=30\mu\text{A}/\text{v}^2$, $V_{TNO}=0.5\text{V}$, $V_{TPO}=-0.5\text{V}$, $C_{OX}=2f\text{F}/\mu\text{A}$, $\lambda = 0$, $\gamma = 0$.

Problem 5  Obtain the AC equivalent and the DC equivalent circuit for the following network. Assume the transistors are operating in the saturation region and all capacitors are large. You need not solve the circuit.

Problem 6  Assume the capacitors are all very large.

f) Draw the small signal equivalent circuit for the amplifier shown

g) Determine the quiescent value of $V_C$ and $V_{OUT}$

h) Obtain the small-signal voltage gain
i) Determine the small-signal output voltage $u_{OUT}$ if $V_M = 1\text{mV}$

$$V(t) = V_M \sin(\omega t + \theta)$$

$V_{DD} = 32\text{V}$

Problem 7 Obtain the quiescent output voltage and the small signal voltage gain.

Problem 8 Determine the small signal output voltage if the small signal input voltage is a sinusoidal 1KHz signal with 0-P amplitude of 25mV.
Problem 9  Obtain the small signal impedance between the two terminals exiting the box. Assume the MOSFET is operating in the Saturation region and the BJT in the Forward Active region and that the quiescent currents are both 1mA.
Problem 10
Consider a device characterized by the equations

\[ I_1 = V_1 V_2^2 \]
\[ I_2 = 0.1e^{0.2V_1^2V_2} \]

a. Determine the small signal model for a two-terminal device characterized by the equations given above.
b. Determine the numerical values for the small signal model parameters if the quiescent value of the port voltages are \( V_2 = 1 \text{V}, V_1 = 5 \text{V} \).
c. Determine the quiescent currents at the Q-point established in part b.
d. Determine the small signal currents \( i_1 \) and \( i_2 \) if the small signal voltages \( v_1 \) and \( v_2 \) were measured to be \( 1 \text{mV}_{\text{RMS}} \) and \( 2 \text{mV}_{\text{RMS}} \) respectively. Assume the same Q-point as established in part b.

Problem 11  Assume \( V_{\text{IN}} \) is a low frequency nearly sinusoidal waveform that is below 25mV 0-P and that \( W=12 \mu \text{m}, L=1 \mu \text{m} \) for the MOSFET.

a) Determine the voltage gain of this circuit if \( V_{XX}=2 \text{V} \).
b) How does the voltage gain change if \( V_{XX} \) is swept between 1.5V and 4V?
Problem 12  In the circuit shown, \( R_F = 40 \text{K} \), \( C_F = 0.1 \mu\text{F} \) and the MOSFET has dimensions \( W = 6 \mu\text{m}, L = 2 \mu\text{m} \). Assume the op amp is ideal.

a) Determine the sinusoidal steady state response if \( V_{XX} = 1.5 \text{V} \) and \( V_{IN} = 0.02 \sin 1000t \).

b) On the same axis, plot the transfer function \( V_{OUT}/V_{IN} \) for \( V_{XX} = 1.5 \text{V}, 14, \) and \( 4 \text{V} \).

c) Obtain an expression for the poles and zeros of the transfer function as a function of \( V_{XX} \) and plot as \( V_{XX} \) varies between 1.5V and 4V.

![Circuit Diagram](image)

Problem 13  In the circuit shown the dimensions of the transistor are \( W = 8 \mu\text{m} \) and \( L = 10 \mu\text{m} \). Assume \( C_1 \) is very large.

a) Draw the small signal equivalent circuit for the amplifier

b) Determine the quiescent value of \( V_D \) and \( V_{OUT} \)

c) Obtain the small-signal voltage gain

d) Determine the small-signal output voltage \( \mathbf{u}_{OUT} \) if \( V_M = 20 \text{mV} \)

![Circuit Diagram](image)
Problem 14  In the circuit shown the dimensions of the transistor are $W=10\mu$ and $L=1\mu$. Assume $C_1$ and $C_2$ are very large.

e) Draw the small signal equivalent circuit for the amplifier
f) Determine the quiescent value of $V_D$ and $V_{OUT}$
g) Obtain the small-signal voltage gain
h) Determine the small-signal output voltage $V_{OUT}$ if $V_M=200mV$

![Small signal equivalent circuit](image)

Problem 15  If $R_1=10K$, size the device so that the amplifier has a voltage gain of -8. Determine the quiescent value of the output voltage (the voltage on the drain node of $M_1$)

![Amplifier circuit](image)

Problem 16  Design an amplifier using only BJT transistors, resistors, capacitors and voltage sources that has a voltage gain of -10 when driving a 2K resistor.

Problem 17  Design an amplifier using only MOS transistors, capacitors, and voltage sources that has a voltage gain of -10 when driving an external 10K resistor.
Problem 18  Using ModelSim, build a 3-8 bit decoder. For an input of 000 to 111 it should decode into an 8 bit number with ones from position 0 to the position noted by the decimal equivalent of the 3–bit binary number. For example, 011 will correspond to 00001111 and 100 corresponds to 00011111. Be sure to include your module code, test bench code, and waveforms.
Problem 18  Using Verilog, design a serial-to-parallel converter. The converter should take in a serial input from an external source and output an 6-bit parallel result stored in a register file (just a multi-bit group of flip flops that each store one bit of data). Assume the serial input arrives prior to each rising clock edge from a microcontroller using the same clock signal. Thus, a new bit of serial data is available on each clock pulse to be stored in the register file. In addition to the serial input and clock signal, two other inputs to the system are the active low reset and conversion enable. When reset is low, the parallel register is loaded with 0's. When high, the system resumes normal operation. The conversion enable signal must be set high in order for serial-to-parallel conversions to take place. Otherwise, the incoming serial data is ignored. Finally, when writing the testbench, assume the clock period is 10ns. Please submit the module code, testbench code, and simulation waveform to receive full credit.