Instructions: Students may bring 1 page of notes (front and back) to this exam. There are 8 questions and 6 problems. The points allocated to each question and each problem are as indicated. Please solve problems in the space provided on this exam and attach extra sheets only if you run out of space in solving a specific problem.

If reference to a semiconductor processes is needed beyond what is given in a specific problem or question, assume a CMOS process is available with the following key process parameters: \( \mu_n \text{COX}=100 \mu A/\sqrt{2} \), \( \mu_p \text{COX} = \mu_n \text{COX}/3 \), \( V_{TNO}=0.5 \text{V} \), \( V_{TPO} = -0.5 \text{V} \), \( C_{OX}=2fF/\mu^2 \), \( \lambda = 0 \), and \( \gamma = 0 \). If reference to a bipolar process is made, assume this process has key process parameters \( J_S=10^{-15} \text{A}/\mu^2 \), \( \beta=100 \) and \( V_{AF} = \infty \). If reference to a diode is made, assume the process parameter \( J_S=10^{-17} \text{A}/\mu^2 \). If any other process parameters for MOS devices are needed, use the process parameters associated with the process described on the attachment to this exam. Specify clearly what process parameters you are using in any solution requiring process parameters.

1. (2pts) What type of carriers (majority or minority) carry current in the channel of a p-channel MOSFET?

2. (2pts) What does the term “self aligned” in the context of fabrication of devices in a CMOS process mean?

3. (2pts) The MOSFET was reported somewhat earlier than the BJT. How many years lapsed from the time the MOSFET was first reported to the time the BJT was first reported?

4. (2pts) What region in the MOS transistor corresponds to the saturation region of the BJT?

5. (2pts) Why is the term \( u_n \text{COX} \) for an n-channel MOSFET larger than the corresponding term \( u_p \text{COX} \) for a p-channel MOSFET?

6. (2pts) What is the purpose of the n+ buried layer in a bipolar process?
7. (2pts) What is the approximate ratio between the doping level of a p-substrate and that of the n+ source/drain diffusions in a CMOS process?

8. (2pts) Why are contacts not allowed on top of the gate region in most semiconductor processes?

9. (2pts) The capacitance of a VARACTOR varies with the dc voltage across the device. What is happening in this device that causes the capacitance to be voltage dependent?

10. (2pts) What are the design variables in the model that was introduced in class for the BJT?
Problem 1 (12 pts) The layout of a resistor is shown. This sheet resistance of one portion of the resistor is 90 $\Omega/\square$ and of a second portion is 30 $\Omega/\square$ as indicated.

a) Determine the resistance between node $\mathbb{A}$ and ground
b) Determine the nodal voltage at the point on the resistor denoted by the voltage $V_X$. 

\begin{align*}
R_{e1} &= 90 \Omega/\square \\
R_{e2} &= 30 \Omega/\square
\end{align*}
Problem 2 (12 pts) Assume the manufacturing cost of 8” wafers in a CMOS process is $1200. Determine the cost per good die if the die area is 4mm² and the defect density is 1.5/cm².
Problem 3 (12 pts)  Determine $R_C$ so that $V_{OUT}=6V$. 

![Circuit Diagram]
Problem 4 (16 pts) Assume the length of the transistor $M_1$ is $20\mu$. Determine the width of $M_1$ that will make $V_{OUT} = 4V$. 

![Circuit Diagram](image-url)
Problem 5 (12 pts) Assume the diodes $D_1$ and $D_2$ are matched.

a) Determine $V_{OUT}$ in terms of $I_1$

b) If $I_1=1\,\text{mA}$ and the diode junction area is $100\,\text{u}^2$, obtain an expression for and plot the variation of $V_{OUT}$ with temperature $T$ for $200\,\text{K}<T<400\,\text{K}$
Problem 6  (16 pts)
a) Design a circuit at the transistor level using the complex logic gate approach to implement the function \( F = AB + \overline{AC} \)
Assume you have the input variables A, B, and C available

b) If all of the devices in your circuit are of dimensions L=1u, W=1u, determine the HL propagation delay at the output of this gate if at time t = 0, the input variables transition from \([A B C] = 0 \ 1 \ 0\) to \([A B C] = 1 \ 1 \ 0\). Assume this design is in the ON 0.5u process and that the output of the complex logic gate you designed is driving a 50fF capacitive load.
## TRANSISTOR PARAMETERS

<table>
<thead>
<tr>
<th>MINIMUM</th>
<th>W/L</th>
<th>N-CHANNEL</th>
<th>P-CHANNEL</th>
<th>UNITS</th>
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<tr>
<td>Vth</td>
<td>3.0/0.6</td>
<td>0.78</td>
<td>-0.93</td>
<td>volts</td>
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<tr>
<td>SHORT</td>
<td>20.0/0.6</td>
<td>439</td>
<td>-238</td>
<td>uA/um</td>
</tr>
<tr>
<td>Wid</td>
<td>20.0/0.6</td>
<td>&lt;2.5</td>
<td>&lt;2.5</td>
<td>pA/um</td>
</tr>
<tr>
<td>LARGE</td>
<td>50/50</td>
<td>0.70</td>
<td>-0.95</td>
<td>volts</td>
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### PROCESS PARAMETERS

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<th>N+ACTV</th>
<th>P+ACTV</th>
<th>POLY</th>
<th>POLY2</th>
<th>POLY2</th>
<th>MTL1</th>
<th>MTL2</th>
<th>UNITS</th>
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<tbody>
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<td>Sheet Resistance</td>
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<td>103.2</td>
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<td>ohms</td>
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<td>Gate Oxide Thickness</td>
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<td></td>
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<td>angstrom</td>
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### COMMENTS:

- N\POLY is N-well under polysilicon.