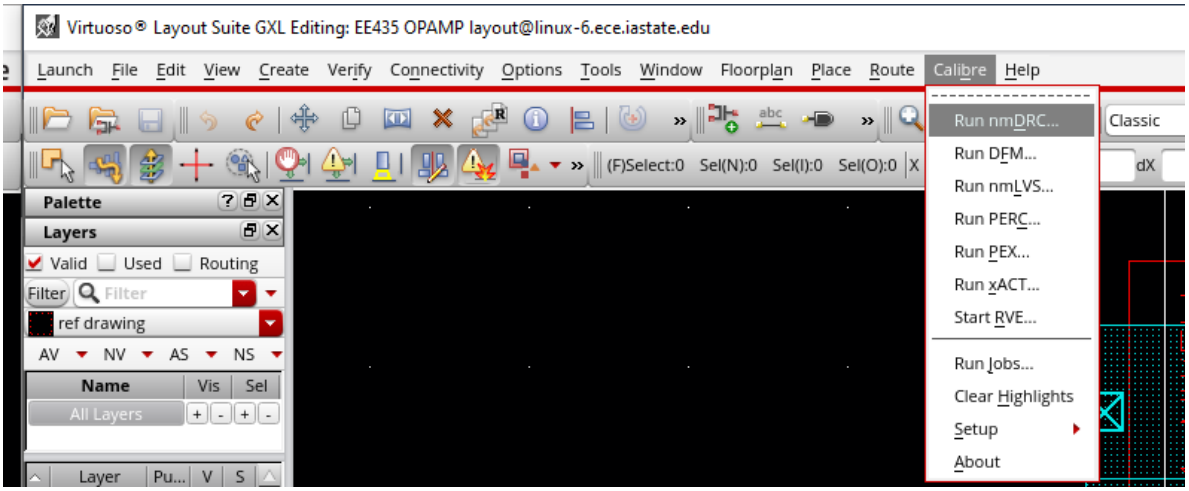
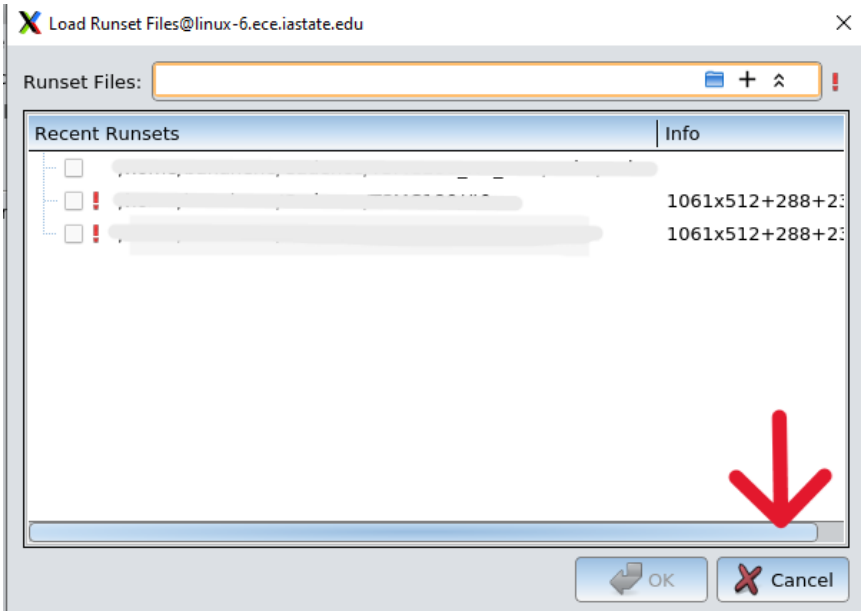
Calibre

Design Rule Check (DRC)

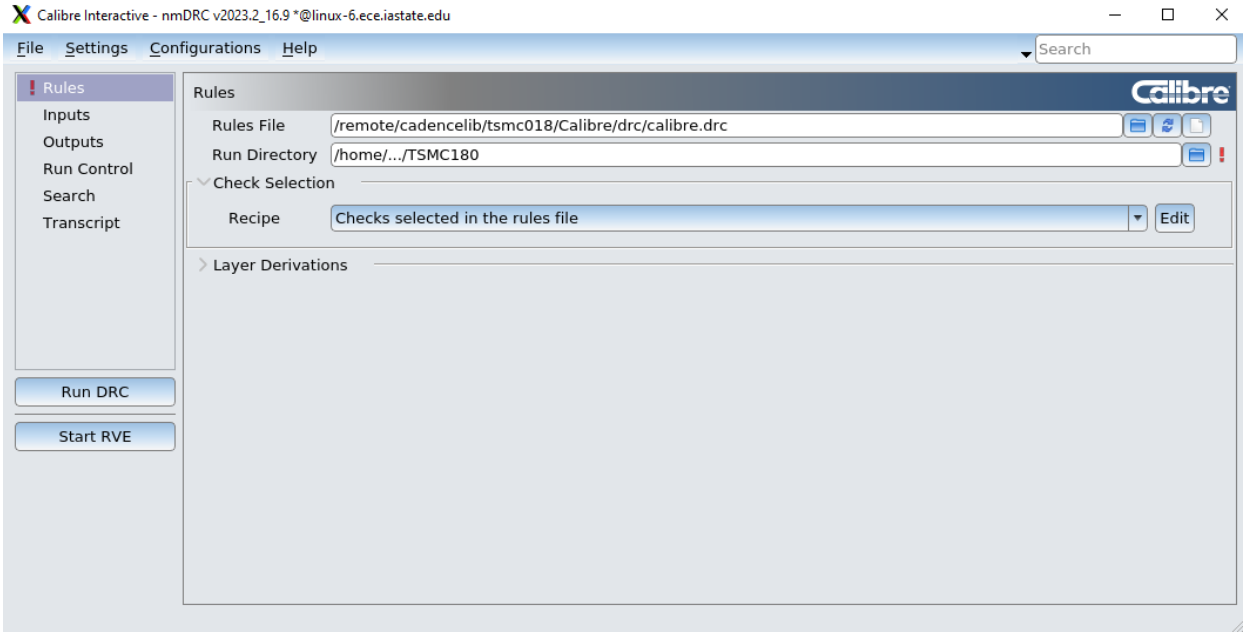
[1] To run DRC in the layout window, you need to first click on "**Calibre**" in the top menu. Then, select "**Run nmDRC**" from the options that appear.



[2] Click the **Cancel** button when the "**Load Runset File**" window pops up.

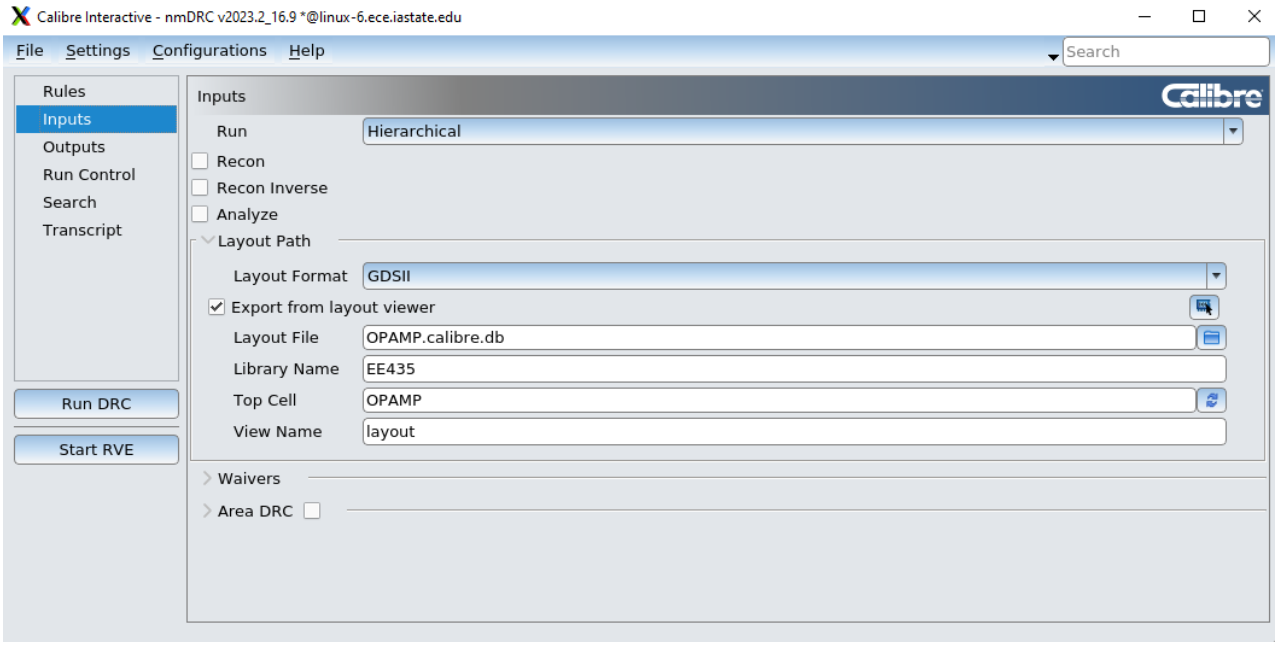


[3] Set the **DRC Rules Files** path to: /remote/cadencelib/tsmc018/Calibre/drc/calibre.drc



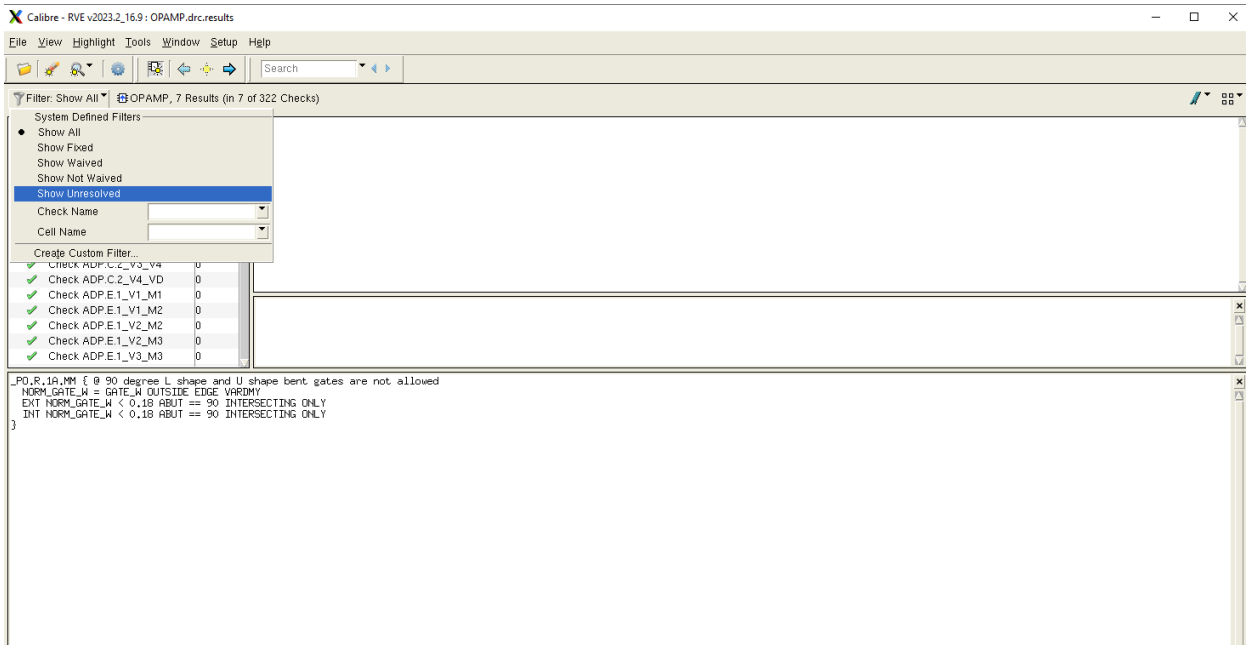
and set the **DRC Run Directory** as your working directory

[4] Ensure that "**Export from layout viewer**" is checked in the "**Inputs"** tab.



[5] Click "**Run DRC**"

[6] When the DRC process is finished, the DRC window should pop up automatically. To view all DRC errors, simply click on the "**Show all**" and select "**Show Unresolved**". This will display all the errors that need to be addressed.



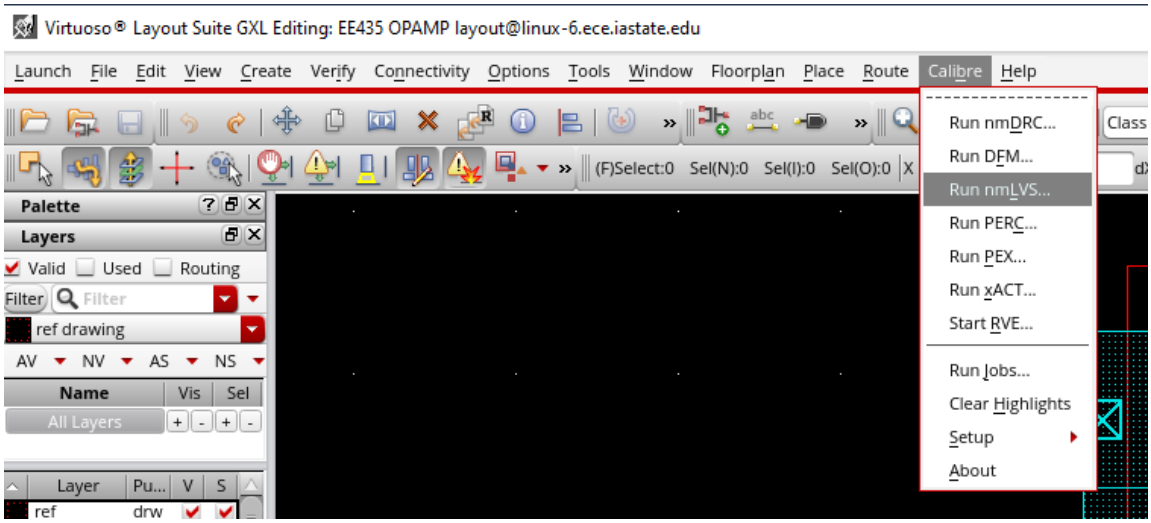
[7] Fix all errors except for

Check PO.R.5
Check PO.R.4
Check PO.R.3
Check M1.R.1
Check M2.R.1
Check M3.R.1
Check M4.R.1
Check M5.R.1
Check UTM40K.R.1
Check DRM.R.1
Check OD.R.3
Check MOM.R.2

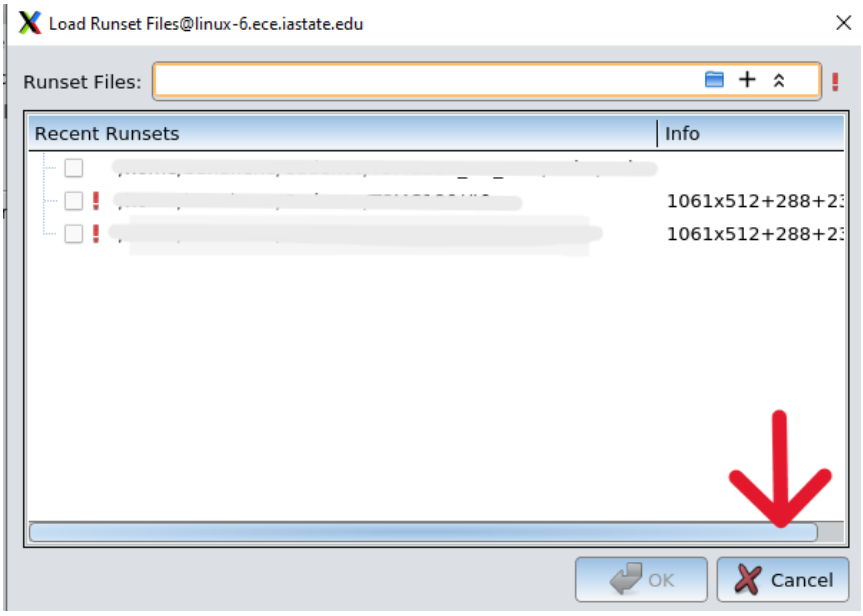
These errors are related to the mental density of the chip, which can be waived for now.

Layout Versus Schematic (LVS)

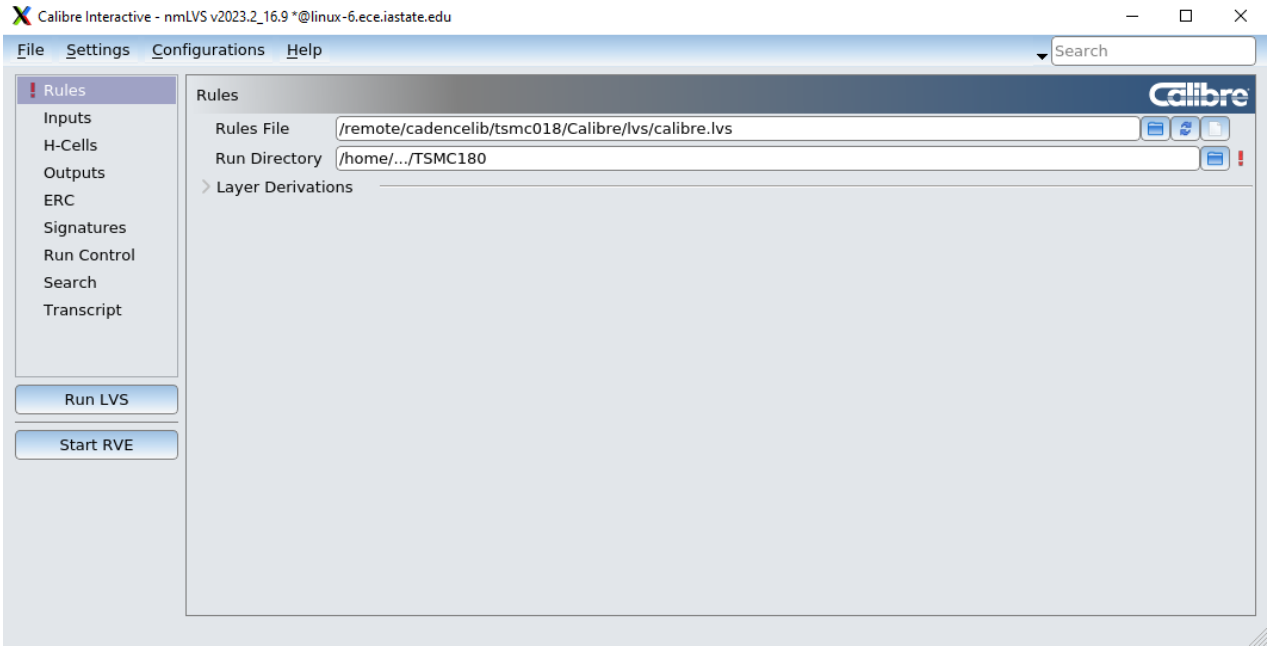
[1] To run LVS in the layout window, you need to first click on "**Calibre**" and then select "**Run nmLVS**" from the options that appear.



[2] Click the **Cancel** button when the "**Load Runset File**" window pops up. A **runset** file can be saved after for later use.

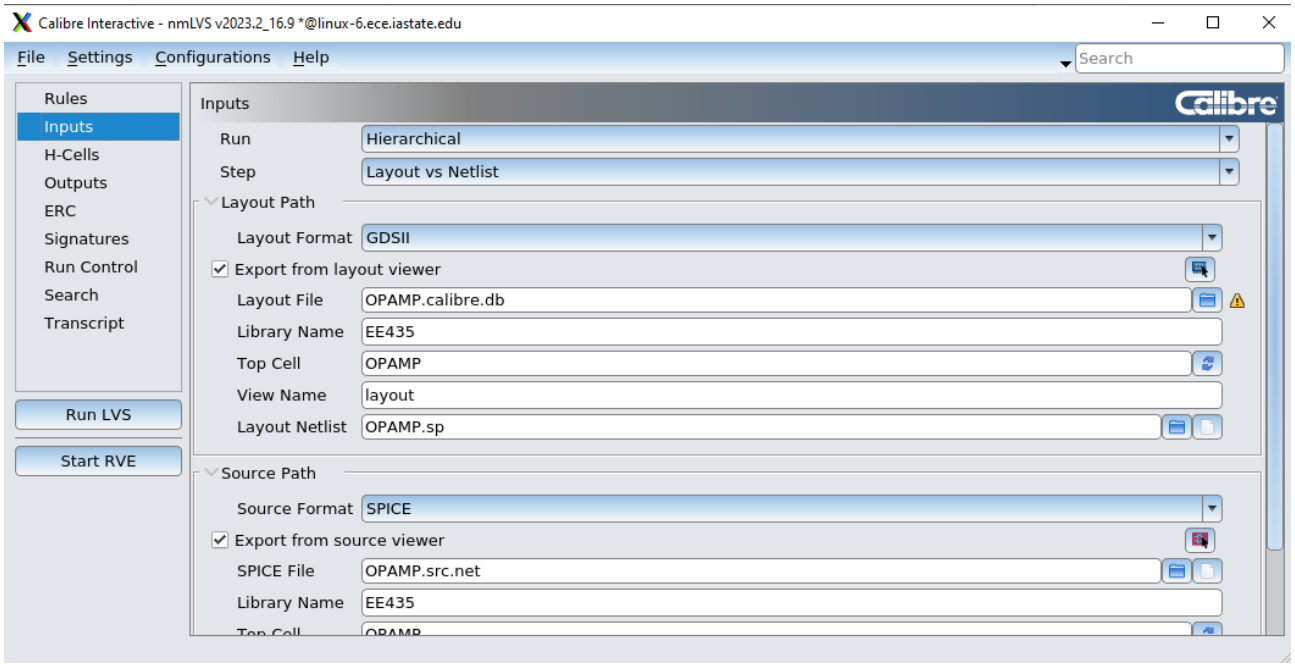


[3] Set the **LVS Rules Files** path to: /remote/cadencelib/tsmc018/Calibre/lvs/calibre.lvs

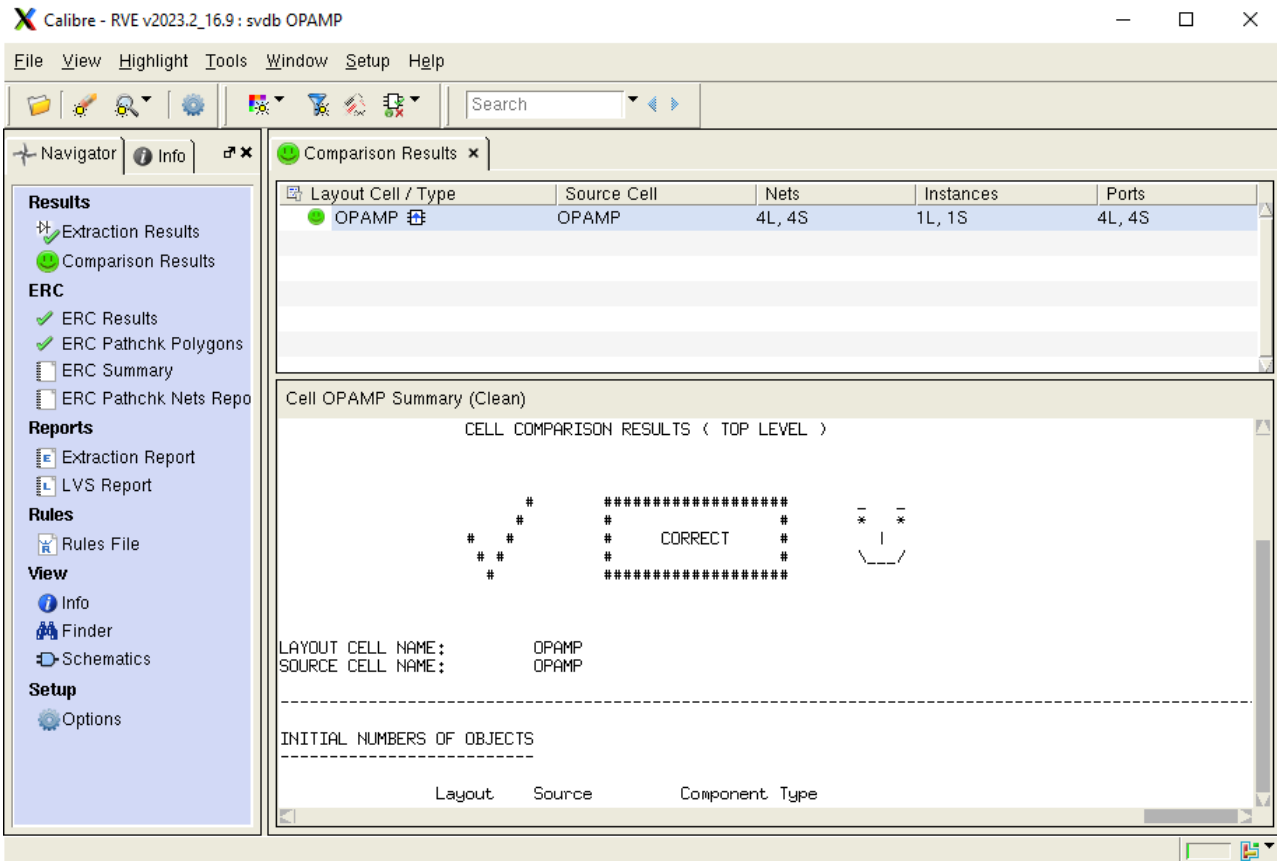


and set the **LVS Run Directory** as your working directory

[4] Ensure that "**Export from layout viewer**" and "**Export from source viewer**" are checked in the "**Inputs**" tab.



[5] Click "**Run LVS**". When LVS is done running, a report window will pop-up.



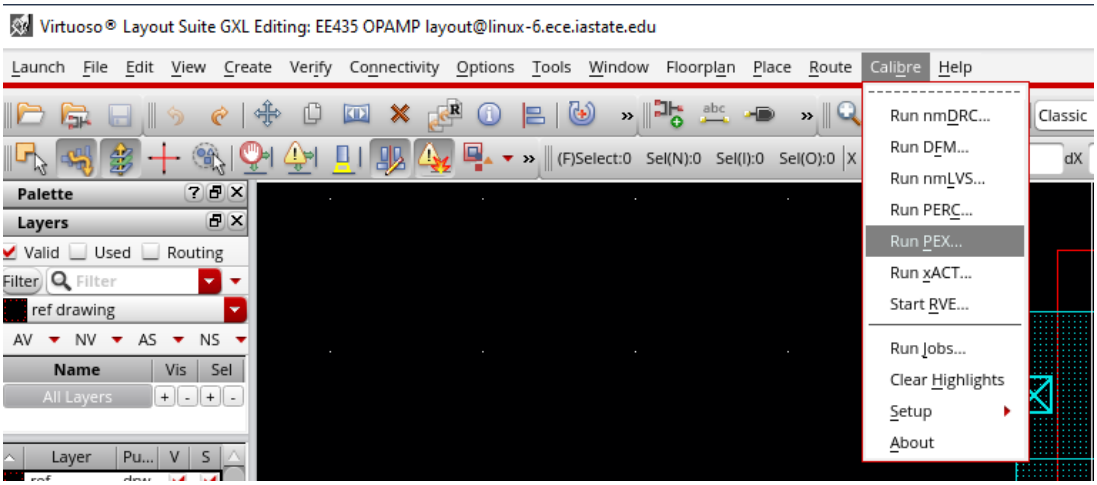
Correct the layout if any errors are reported. The desired report window is displayed in the above image.

[6] You may save this **runset** for later use so that you do not need to set it up every time.

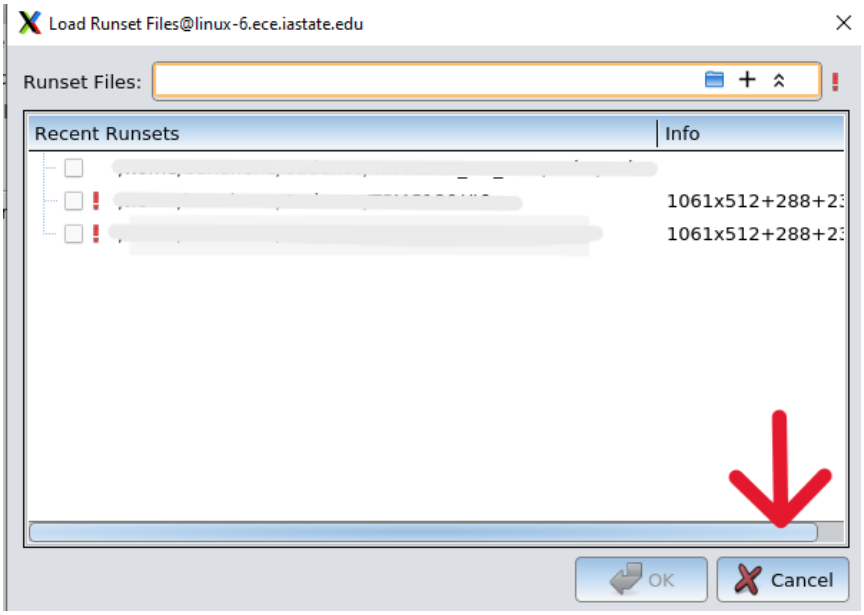
Parasitic extraction and Post-layout Simulation

Extraction:

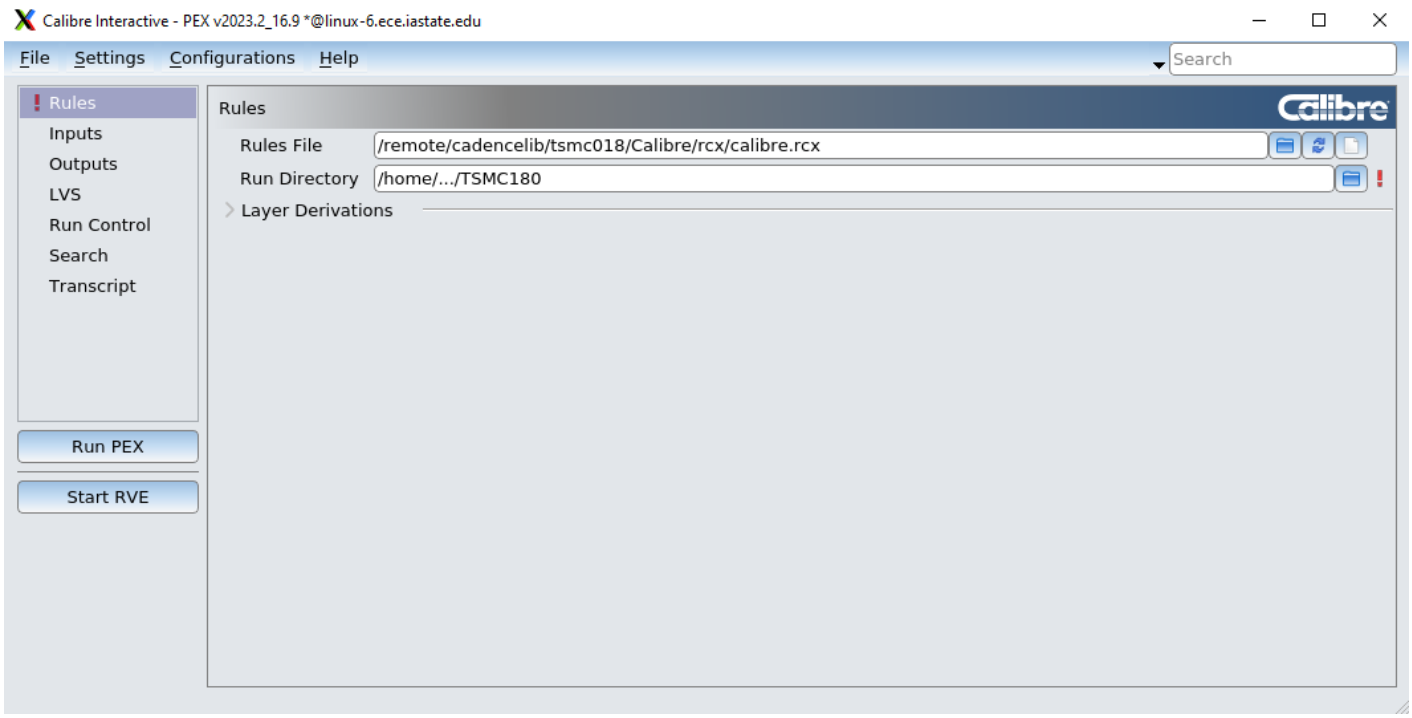
[1] PEX is used to generate the parasitic capacitance and resistance of your layout design. Click on "**Calibre**" and then select "**Run PEX**" from the options that appear.



[2] Click the **Cancel** button when the "**Load Runset File**" window pops up. A **runset** file can be saved after for later use.



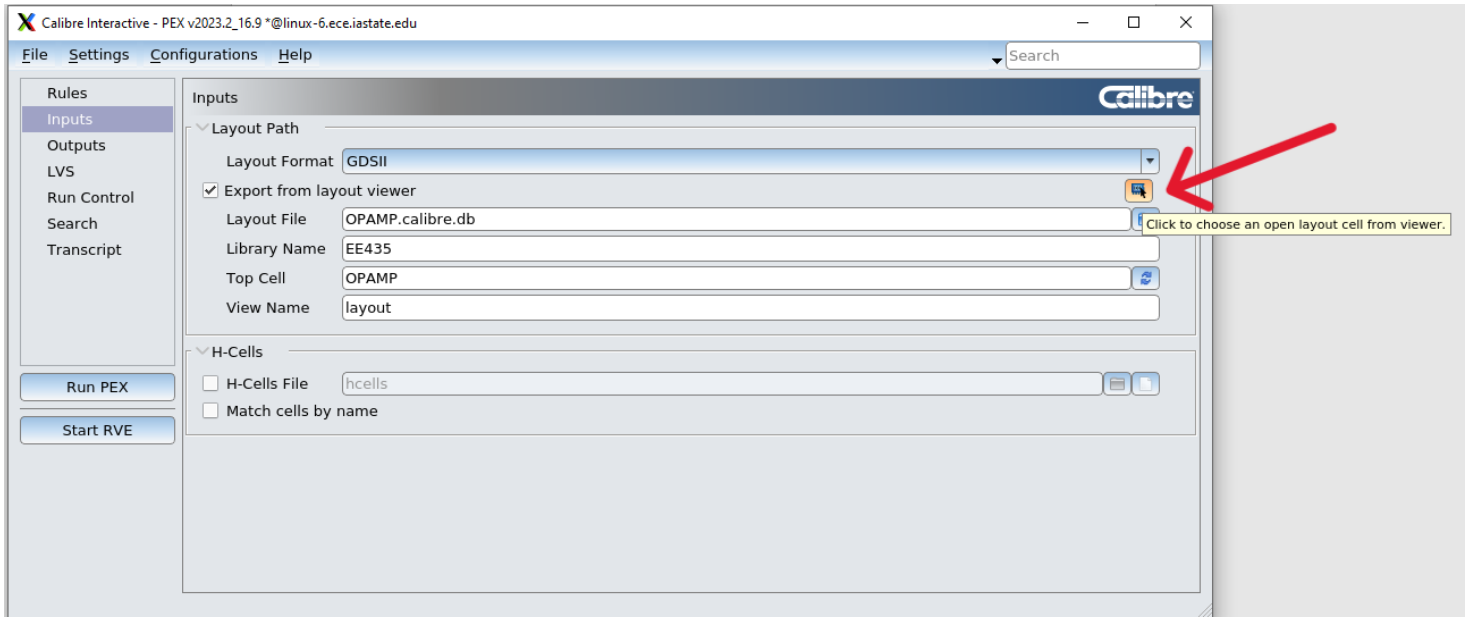
[3] Set the **PEX Rules Files** path to the location the caliber.rcx file is placed.
e.g. **/home/NetID/TSMC018/calibre.rcx** or **/home/NetID/Cadence/TSMC018/rcx/calibre.rcx**



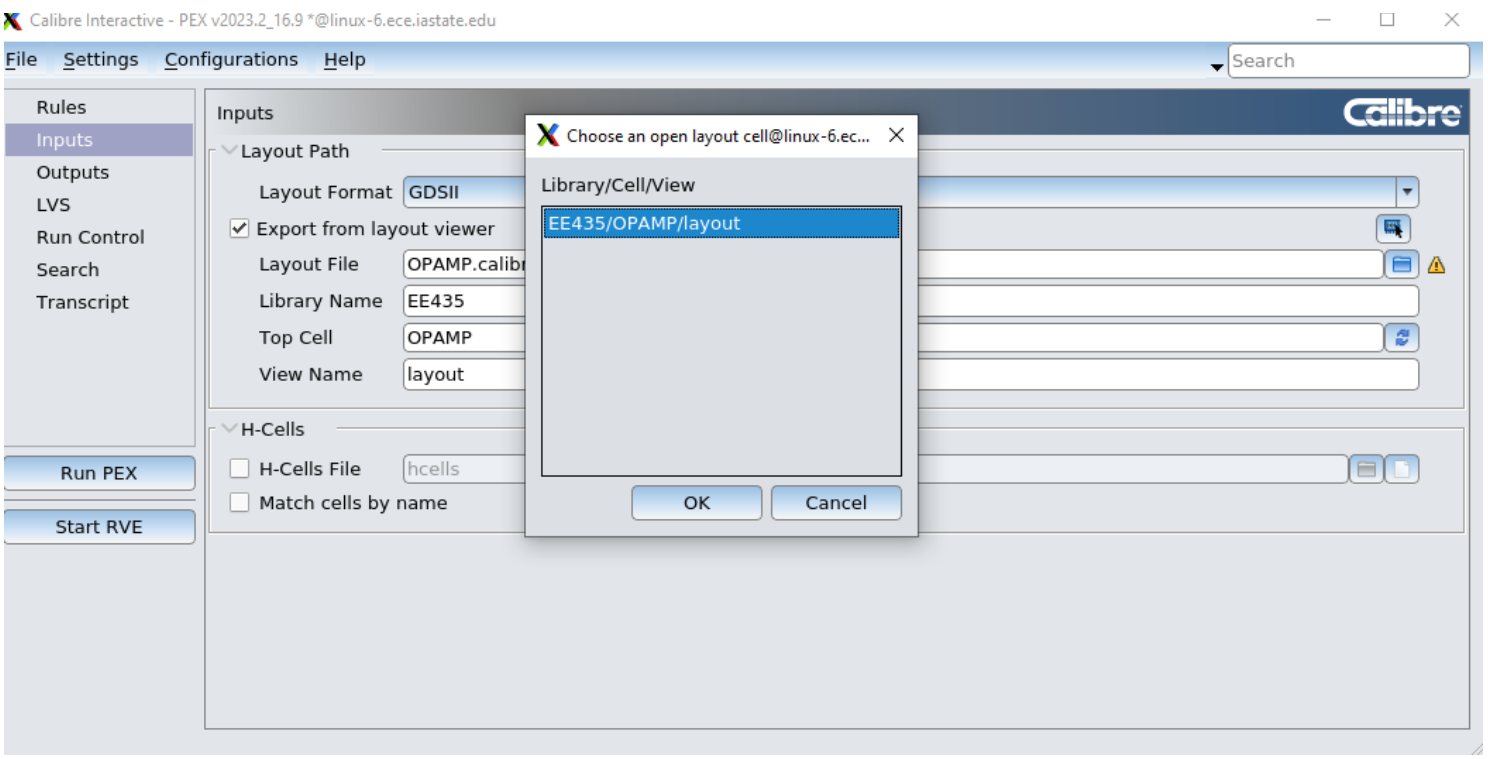
and set the **LVS Run Directory** as your working directory.

For the lab sessions, you will download the "**calibre.rcx**" file from the class website and place in a location of your choice. **DO NOT USE THE PATH IN THE IMAGE ABOVE.**

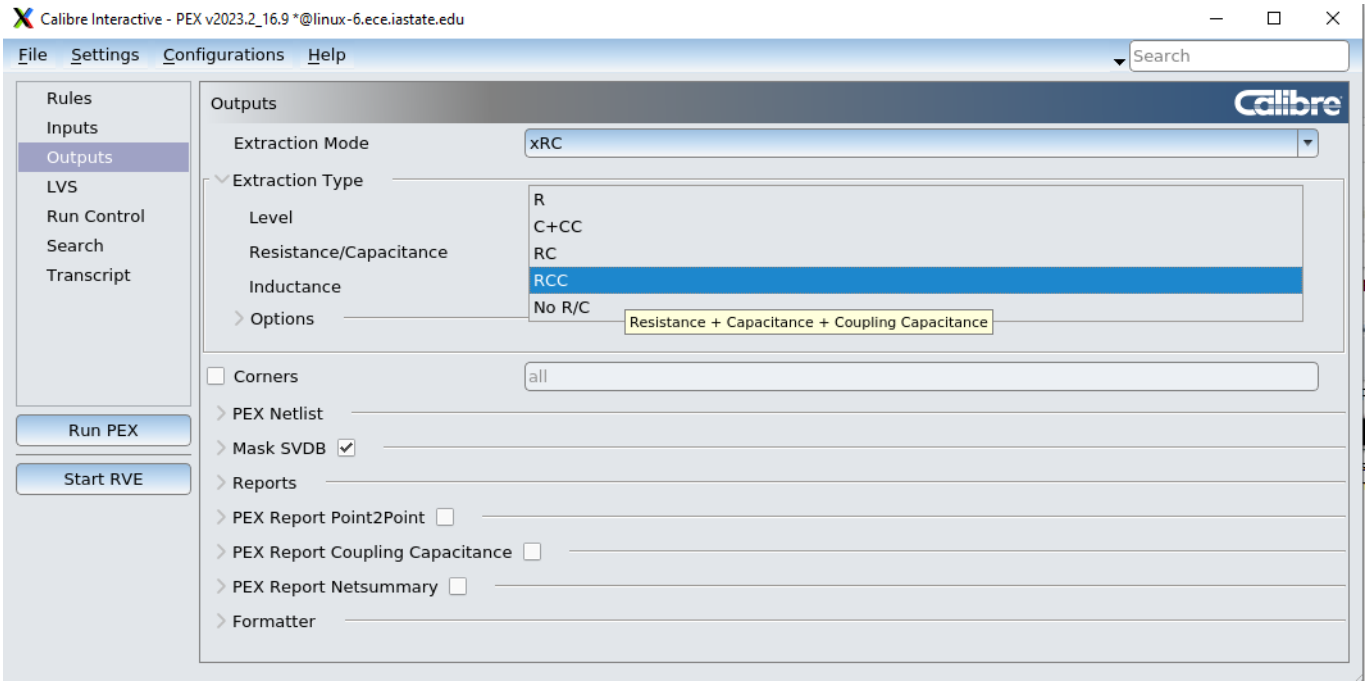
[4] In the "**Inputs"** tab, ensure that the correct library and cell are selected. If not, click the button to the right of "**Export from layout viewer**" displayed in the image below.



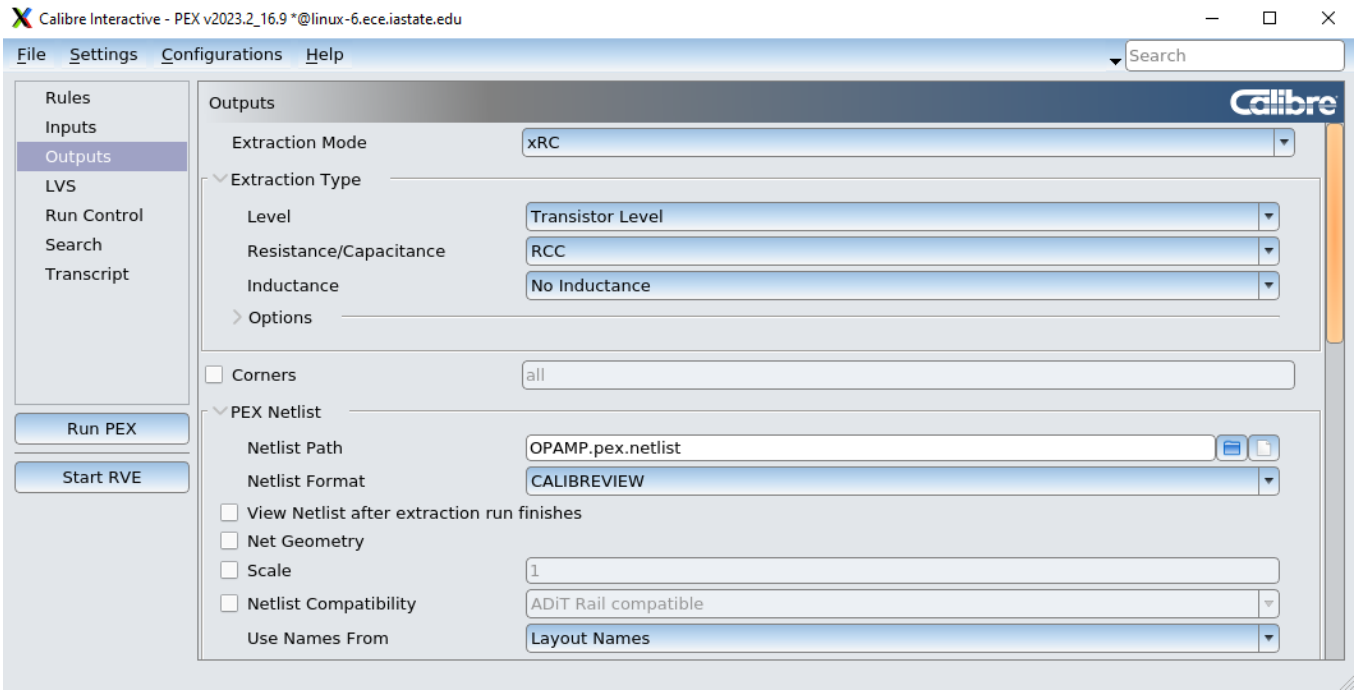
Click on OK in the pop-up window, and the correct data should be populated in the layout path



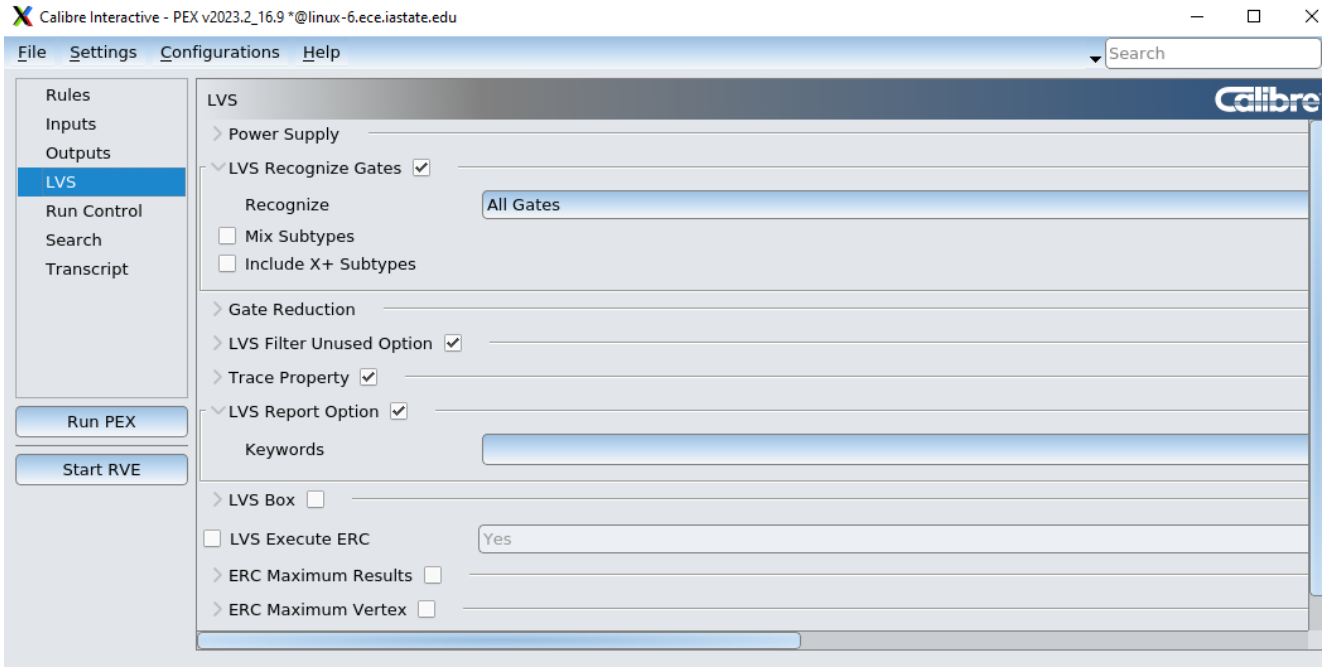
[5] In **Outputs->Extraction Type->Resistance/Capacitance,** RCC is usually preferred because it is closest to the real situation. Simulation may run longer as there are more components with this option.



[6] Under **Outputs->PEX Netlist->Netlist Format,** choose **CALIBREVIEW**

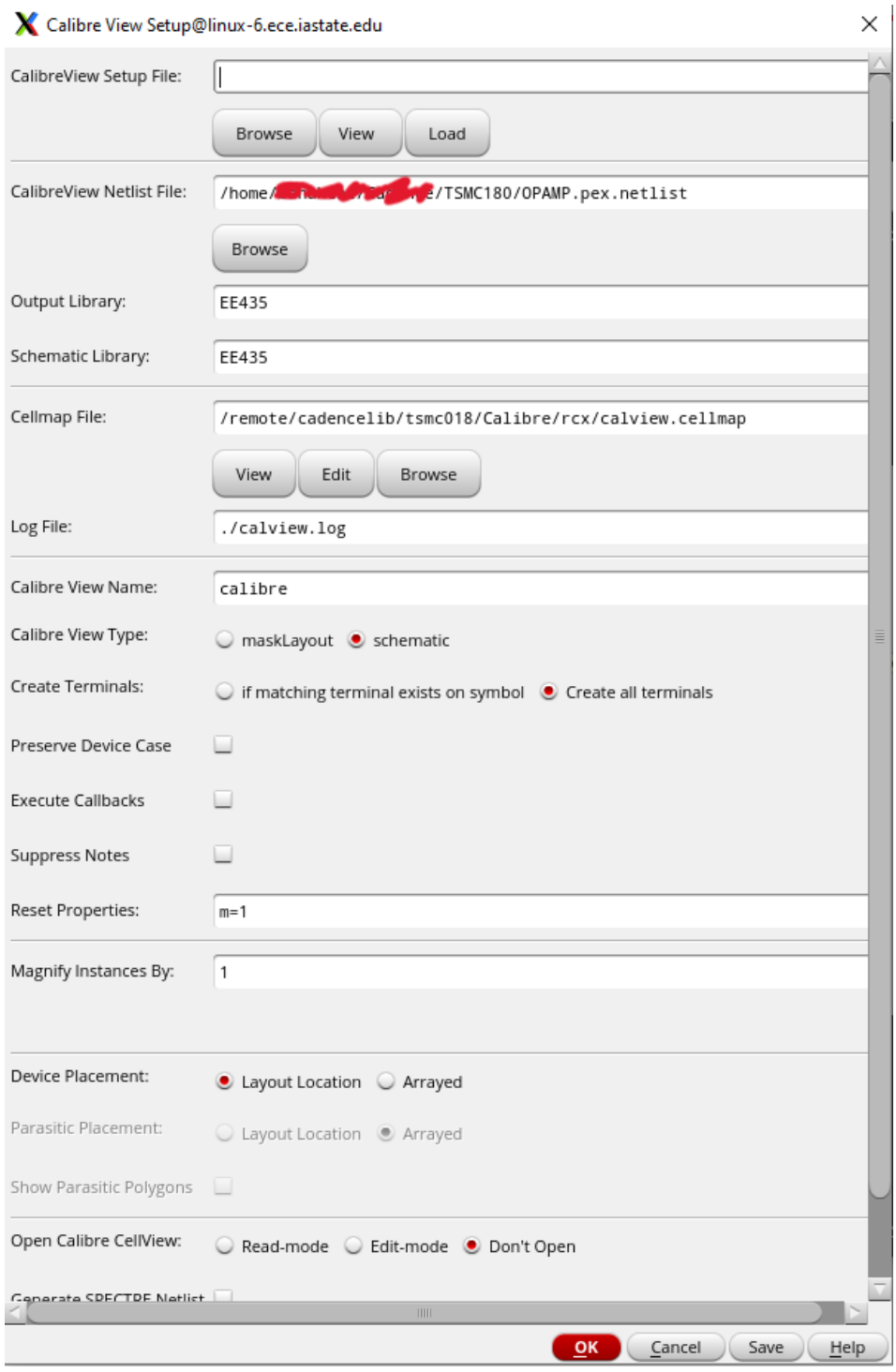


[7] In the LVS tab,

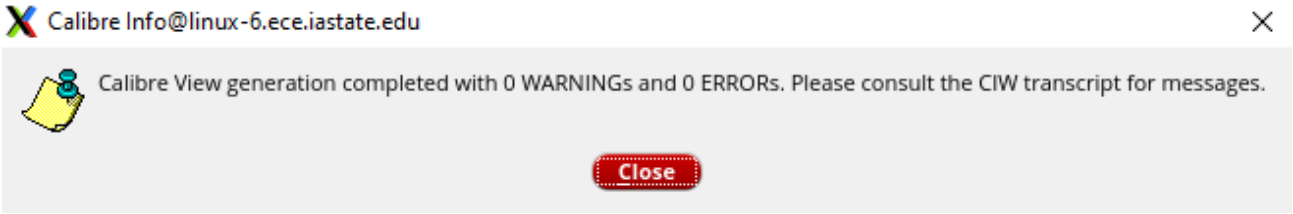


[8] After configurations are done, click **"Run PEX"**. A calibre view setup window should pop up. For the Cellmap path file use: **/remote/cadencelib/tsmc018/Calibre/rcx/calview.cellmap**

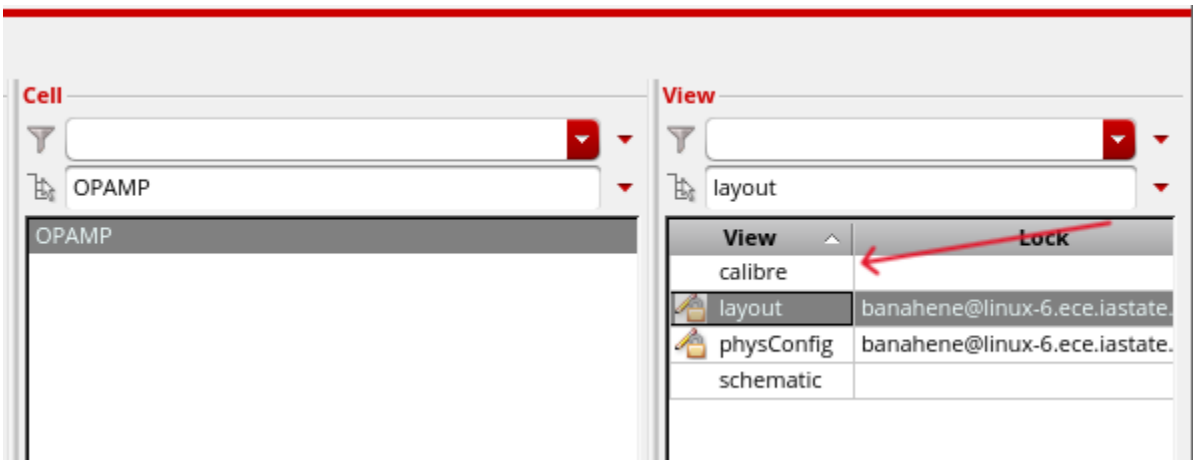
[9] Set **Calibre View Type** to **schematic** and also set **Create Terminals** to **Create all terminals**



[10] Click on OK. A Calibre Info window should pop up, correct the errors if there are any.

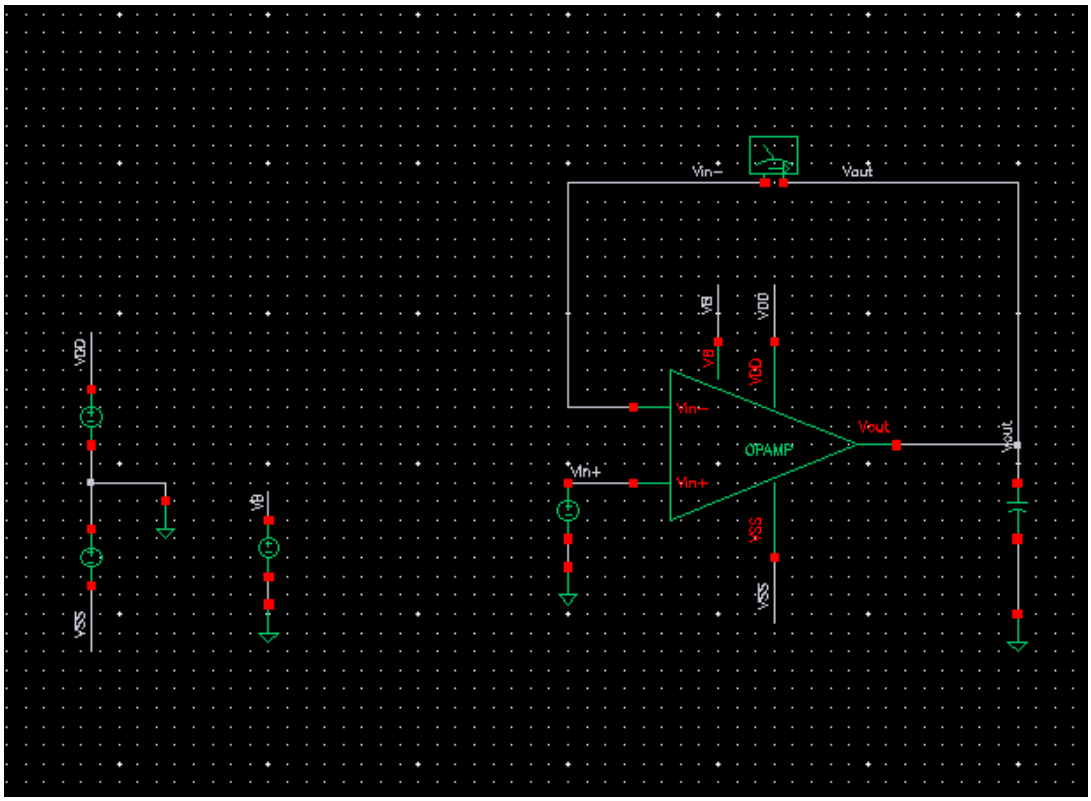


[11] You now have a **calibre** view with the extracted parasitic resistances and capacitances which will be used for the parasitic extracted simulation.

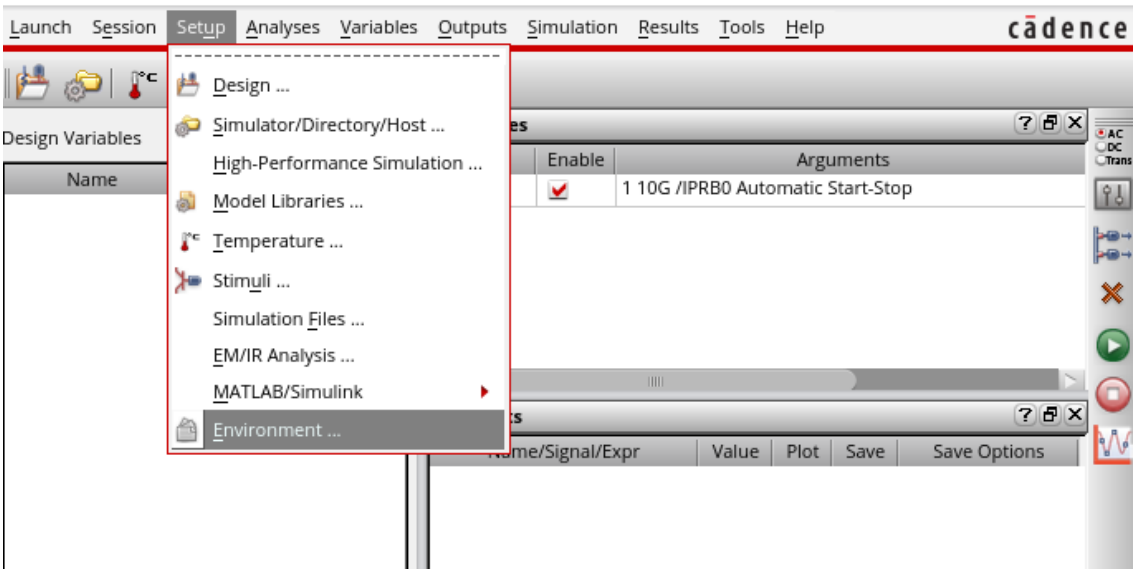


Simulation:

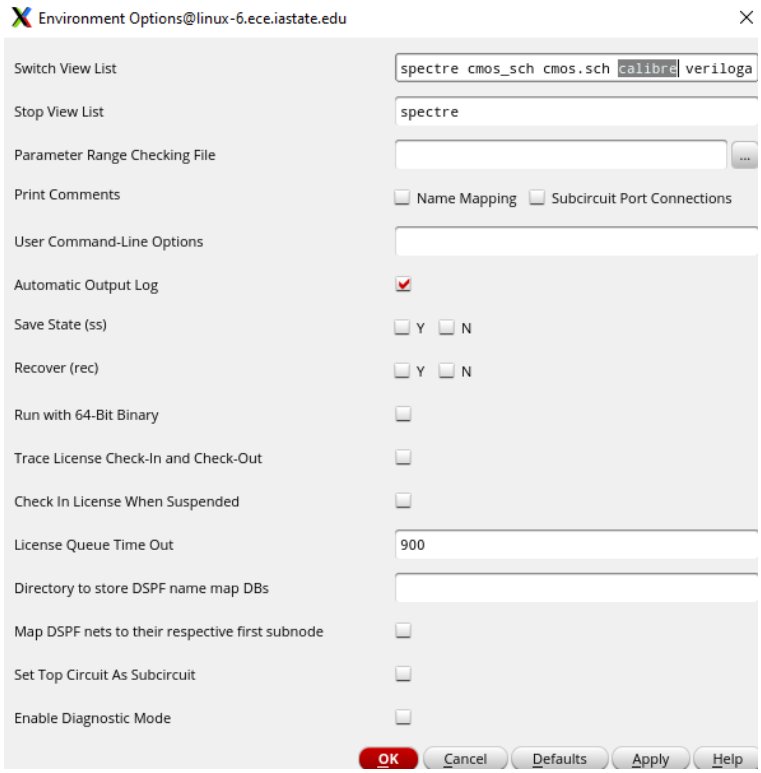
[12] Go to the testbench that you previously created for the schematic simulation



[13] For **ADE L** simulations, go to **Setup -> Environment**

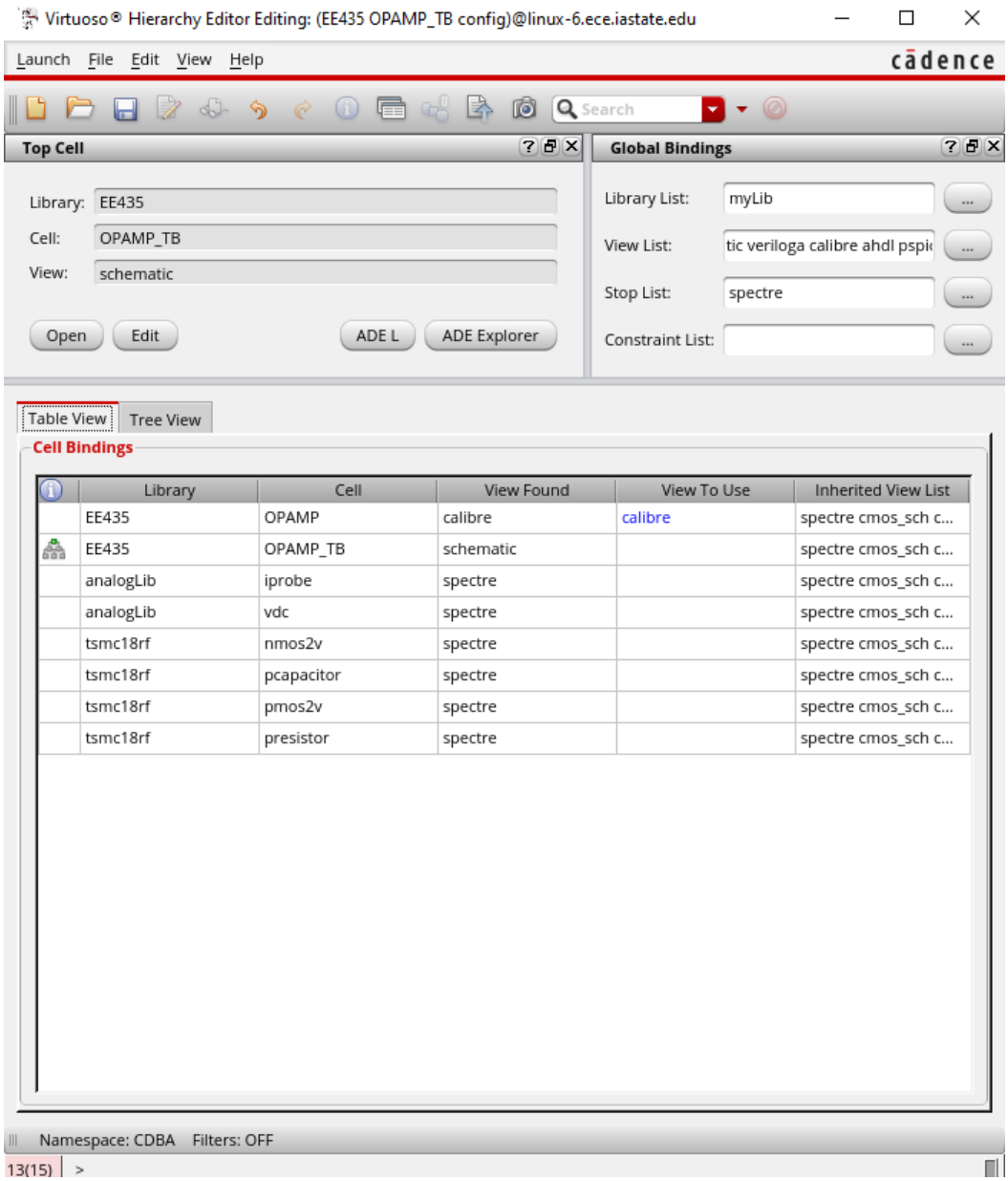


[14] Change "**schematic**" to "**calibre**" and click OK. Run simulation and results should now be extracted view



[15] For maestro simulations, change the view of the device under test to "calibre" in "View To Use" in the config view. (Image on next page)

[16] Save the changes made in the config view. Any simulation for the test device will use the extracted model.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Library: EE435
Cell: OPAMP_TB
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Library List: myLib
View List: tic veriloga calibre ahdl pspi
Stop List: spectre
Constraint List:
Table View Tree View
Cell Bindings
Library Cell View Found View To Use Inherited View List
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analogLib vdc spectre spectre cmos_sch c...
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