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Objective:

This experiment focuses on the concept of layout of integrated circuits. Manual and partially automated methods of layout will be discussed. Design rules and the use of CAD tools for verifying that all design rules are satisfied, termed design rule checkers (DRC), will be introduced. Finally, CAD tools for verifying that the actual equivalent circuit corresponding to a layout agrees with the original circuit schematic, known as layout versus schematic (LVS), will be introduced.

Note: If the inverter you designed in the previous experiment is still sized at 45μm and 15 μm for PMOS and NMOS, respectively, re-size it back down to 4.5μm and 1.5 μm.

In order to allow tens or hundreds of engineers to work on the same design a large number of design rules have been made to make sure all layouts created will work properly. The full design rules we use can be obtained from the MOSIS WEB site https://www.mosis.com/files/scmos/scmos.pdf but a subset of the design rules that will be adequate for this experiment can be found on the class WEB site at http://class.ece.iastate.edu/ee330/miscHandouts/MOSIS%20Rules%20Pictorial%202009.pdf/. These rules can be referenced when an error occurs during a Design Rule Check (DRC) check if needed.

Part 1 creating a layout

Open a layout view of the inverter, like in Part 4 of Lab 2. Most likely you have not been taught how to design a layout, so the basics will be explained here. For the first layout we will not concern ourselves with size, but in later layouts making the transistors the proper size will be important.

To start the layout we will create the basis that will become the PMOS transistor. Select the P active layer and draw a rectangle. Then select the P Select layer and draw a rectangle around the P active rectangle. Then select the N well layer and draw a rectangle around the P select rectangle. Then, run a DRC to make sure the edge of each rectangle is far enough from the next rectangle.

1.1 Run DRC Early and Often

As you design your layout you will want to run multiple DRC. To run a DRC, go to Verify → DRC →{OK or Apply}. If there is a design rule violation, the DRC tool will identify what it is and where it is at. For example, if the smallest width of a poly strip is 0.6μm, and one was drawn at 0.3μm, then the Design Rule Check will print out an error and create a yellow symbol in the layout. This symbol will not go away until you fix the error and run another DRC. If the DRC does not find any errors, the circuit should not fail when fabricated because of spacing-related concerns.

The DRC check does not guarantee that the circuit corresponding to the layout is the same as the desired circuit nor does it guarantee that the actual circuit schematic meets performance requirements. The file that contains the design rules in the ISU installation of the Cadence toolset is divaDRC.rul.
If your layout has no errors, you should see the following message in the CIW:

Total errors found: 0

If you’d like to debug your errors, you can go to Verify → Markers → Explain, and click on any of the white error markers on your layout. It is easy to guess what the white markers mean: for example, if you see that a rectangle has a white cross inside it; it means it is not properly shaped. If you see white markings in the area between two rectangles, it means that they are too close.

1.2 Create N active region

Once the DRC passes with no warnings, continue making the inverter by creating an N active rectangle. Make this approximately the same size and in line some space below the P active rectangle. Then create a N select rectangle around the N active rectangle. The N active region does not need a P well placed around it because the entire bulk of the design is P doped by default. Run DRC.

Next we want to connect our top P active rectangle to the lower N active rectangle. Select Metal 1 and create a rectangle that overlaps both. We then need to connect the Metal 1 to the N active and P active with Vias.

1.3 Vias

You will need to make connections between layers; this is done through contacts (vias). To create a via, go to Create → Via. Make sure the contact type is correct, i.e. metal1 to P active should be “M1_P”, while metal1 to N active should be “M1_N”. Remember that the substrate is p-type. Run DRC.

1.4 Create the Gate

Next we want to create the gate of the transistor using Poly1. However, instead of creating a rectangle use the Path (shortcut “P”) tool. This tool will automatically create a minimum width rectangle of any length. Start the path by clicking somewhere on your design, in this case select the top of your P active rectangle, then go to the bottom of the N active rectangle and double-click to end the path. A single click will allow you to create a corner. by default a 90 degree turn. The gate does not need vias so run DRC.

1.5 Bulk Connections

The most common thing to forget when designing the layout is to create bulk connections. Each P active region requires a via called a “N Tap”, so designs with many different P active regions require multiple N taps. The Vss line needs an “M1_P” as its bulk connection. Unlike the N tap, most designs we will be making will only need one of these bulk connections for the entire design.
These bulk connections need to be connected to the P active and N active regions. Use a Metal 1 rectangle to connect them and M1_P and M1_N vias to connect that metal to the active regions, as in Figure 5.

1.6 Pins

The final step will be to make inputs and outputs for your circuit. To create a pin, go to Create Pin. Make sure the pins are consistent with the schematic: names and I/O types. Pin names are case sensitive and cannot be changed without deleting and remaking them. Any other variables of a pin, such as its layer or I/O type can be changed in its properties later. Check the Display Terminal Name (Replaced with Create Label) and Physical Only boxes. When you know where the pin goes, make sure to have the same layer selected in the Layers toolbox.

Create the pins for your Input, Output, and Vss and Vdd connections. Vss and Vdd will be I/O type inputOutput. These will often be made of Metal 1, but the Input can be made from Poly to connect it directly to the gate rather than adding a “M1_Poly” via.

Notable DRC Error with Pins

Label/Pin “[Pin Name]” is causing two nets to have the same name. This error is fairly common when running DRC once Pins have been placed, but is not really an error most of the time. The problem is that the computer does not recognize that the active region of the transistors is being split into two different nets with the use of the gate. This error can usually be ignored, but may need to be looked into if there is a problem with the Layout Vs Schematic (LVS) later.
Once you believe the design is complete it is time to extract the layout. This means that the computer will generate a schematic from the layout. To create this schematic, go to **Verify → Extract → OK.** The extraction rules are in the `divaEXT.rul` file.

With the layout now extracted open the extracted view, this will show something similar to Figure 8. The different outlined rectangles show where nets are, while a solid color shows where a pin is. The color tells you what they are made of, the blue is Metal 1, the red is Poly, etc.

This view also shows what components the computer interprets. In Figure 8 the computer can see a pmos4 and nmos4 cell. Later we will use this to see what the computer interprets as resistors, capacitors, diodes, etc. Move the pmos4 box and the nmos4 box so they are not over the design and press **Shift+F.**

Shift+F is used to show more detail in these boxes, they should now look like Transistors with a width and length, as in Figure 9. By clicking on any box it will change the outline to be white and show what parts are connected. It also shows what point on each component that connection correlates to. As can be seen on in the figure the metal on the right is connected to the Drain of both the NMOS and PMOS, as we want for an inverter.

Notice that these images do not have Pins in them.


2.1 Layout vs. Schematic (LVS) comparison:

When you are satisfied the design is correct it is time to test it. Run the LVS tool on your layout to verify that the circuit you have laid out agrees with your original schematic. Diva is the name of the LVS tool we will be working with in the Cadence toolset. To run LVS in the Cadence environment, go to Verify – LVS. Make sure you are comparing the right schematic and extracted views by hitting Browse. Hit Run when you are ready to run the LVS.

If you have everything checked and saved before you run the LVS, you will get the message:

`Job 'directory' that was started at 'time' has succeeded. `

This only means that the LVS ran properly, not that your design passed the test. If you don’t save your schematic before running the LVS you will get a fail message, so make sure you always save your work. In order to know whether your design passes the LVS, go back to the LVS window and hit Output. Go over the file “si.out” that opens and study its different sections. This is the only text you will have for debugging. If your layout is acceptable and if you scroll down a bit you should see:

The net-lists match.

If they don’t match, you need to alter your layout and re-do all the extraction and LVS steps again until they match.

Figure 10

How to locate a net on the extracted view:

Sometimes it is very hard to find a net in your extracted view. Probing the design makes finding nets a much easier job. Probing can be initiated by the command Verify/ Probe. In the Probing form, click on Add Net. Then go to the CIW, and type “X” (X is the name of the net that you wish to locate) at the command prompt, including the double quotes, and press Enter. Back to the extracted cell-view window, you should see a mask layer being highlighted, which has the given net name. You can also left-click on a net and look at the CIW to know its name. The latter method is faster and more suitable for smaller designs, while the first one is better for larger designs.
Part 3 Using P cells

Now that you are used to using the Layout tools, we are going to remake the inverter more efficiently. Instead of creating the PMOS and NMOS cells by hand, we are going to use Instances of standard cells that automatically create minimum sized P active and N active regions for use.

Start by going to the library manager and select the Inverter schematic. Right click on it and go to Copy, under “To” name the Cell “Inverter2” as in Figure 13. Create a layout for this new Inverter2 schematic (File→New→Cell View→Layout).

In the layout create a new Instance (shortcut “I”) we want to automatically generate a PMOS layout, so select the NCSU_TechLib_ami06 library and the pmos Cell, the view should default to layout (Figure 13). This will appear as a red box that says PMOS, place this in the layout and press Shift+F.

You will now see something similar to the original PMOS you made, but likely much smaller. The instance is automatically minimally sized, but we can change many things by clicking on it and going to Properties (shortcut “Q”).

There are many important things that can be changed here, including the Width, Length, Fingers, and Multiplicity. For an Inverter we want these at their default values, but change the Multiplier to 3 to see the design change to include 3 gates and 4 areas designed to make connections with Metal 1. This will be used to create NAND and NOR gates later, for now return to Multiplicity 1 to continue making the inverter.

Next create another instance this time of NMOS and connect the two gates with a Path (Shortcut "P") of Poly, connect one side of each transistor with Metal 1, and add extensions out to be used to connect to Pins and Bulk Connections. There are many ways to design this to take up as little area as possible, but remember to always make it easy to connect to the inputs and outputs with different parts. One example is shown on the right, Figure 13.

Note: There are multiple errors in the design in Figure 13. The most common thing to forget has been forgotten, and the width of the PMOS cell is not the same as in your schematic. These should both be fixable without much change to the drawing.

We advise you always put Vdd on the top, Vss on the Bottom, all of the Inputs on the Left, and all the Outputs on the Right. When finished extract and run LVS.
Part 4 Looking Forward

In the next experiment, a logic circuit will be designed jointly by two students. For this design, every student will be given a Boolean function for use in the next experiment. The Boolean function will be realized with NAND and NOR logic gates. One student will be responsible for creating a three input NAND gate and the other for creating a three input NOR gate. Find a partner and decide who will be responsible for each gate. The prelab for next week is based upon the NAND or NOR gate you choose to work with and includes drawing a stick diagram of the gates you will be designing. You might find it useful to discuss with your partner where the inputs and outputs as well as $V_{DD}$ and Ground will be located on your NAND and NOR gate and what layer will be used for the inputs and outputs before leaving the laboratory (for example, you might agree that $V_{DD}$ will be on the top of your layout, ground on the bottom of the layout, inputs will be on the left of the layout, and outputs on the right of the layout. Of course, you may choose other pin placements as well).
Useful keyboard shortcuts in schematic view:

<table>
<thead>
<tr>
<th>Action</th>
<th>Key</th>
</tr>
</thead>
<tbody>
<tr>
<td>Add Instance</td>
<td>i</td>
</tr>
<tr>
<td>Add Pin</td>
<td>P</td>
</tr>
<tr>
<td>Wire</td>
<td>w</td>
</tr>
<tr>
<td>Undo</td>
<td>u</td>
</tr>
<tr>
<td>Redo</td>
<td>shift +u</td>
</tr>
<tr>
<td>Properties</td>
<td>q</td>
</tr>
<tr>
<td>Rotate</td>
<td>r</td>
</tr>
<tr>
<td>Copy</td>
<td>c</td>
</tr>
<tr>
<td>Check and Save</td>
<td>F8</td>
</tr>
<tr>
<td>Zoom to Fit</td>
<td>f</td>
</tr>
<tr>
<td>Move</td>
<td>m</td>
</tr>
<tr>
<td>Wire Name</td>
<td>L</td>
</tr>
</tbody>
</table>

Useful keyboard shortcuts in layout view:

<table>
<thead>
<tr>
<th>Action</th>
<th>Key</th>
</tr>
</thead>
<tbody>
<tr>
<td>Create rectangle</td>
<td>r</td>
</tr>
<tr>
<td>More detail in layout</td>
<td>shift + f</td>
</tr>
<tr>
<td>Less detail in layout</td>
<td>ctrl + f</td>
</tr>
<tr>
<td>Stretch rectangle</td>
<td>s</td>
</tr>
<tr>
<td>Zoom to Fit</td>
<td>f</td>
</tr>
<tr>
<td>create ruler</td>
<td>k</td>
</tr>
<tr>
<td>clear all rulers</td>
<td>shift + k</td>
</tr>
<tr>
<td>Undo</td>
<td>u</td>
</tr>
<tr>
<td>Redo</td>
<td>shift +u</td>
</tr>
<tr>
<td>Copy</td>
<td>c</td>
</tr>
<tr>
<td>Properties</td>
<td>q</td>
</tr>
</tbody>
</table>