EE 330 Laboratory 5

Creating bonding pads
Spring 2011

**Objective:** The objective of this experiment is investigate the design of a basic bonding pad and simple ESD protection circuitry.

**Part 1: Layout of a resistor**

The first step of this lab is to learn how to create a resistor. A resistor can be created using almost any layer available in the process. For example, to create a resistor using poly, draw a poly with terminals at its ends as shown below (poly is red, metal1 is blue, and cyan is res_id). For correct extraction of these “intended” resistors, you need to cover the poly with the identification layer called *res_id*. From its name, we can deduce that this is an identification layer, not an actual physical layer for fabrication. The number of squares of poly covered by the *res_id* layer are used to calculate the value of the resistance.

![Resistor Diagram](image)

The *res_id* layer must be used to create resistors in all possible except for the high_res layer. The high_res (high resistance) layer, in contrast with *res_id*, is a physical layer i.e., sent to foundry but does not correspond to actual physical shape. When used with the poly2(elec for our environment) layer, the high_res layer results in increased resistance of poly2 (elec) layer. If you intend to use the high_res layer, follow the design rules on MOSIS website (see section 27). The following table provides the sheet resistance of all the layers that can be used to create resistors for the AMI 0.5u process.

<table>
<thead>
<tr>
<th>Layer</th>
<th>Sheet resistance per square</th>
</tr>
</thead>
<tbody>
<tr>
<td>nwell</td>
<td>819</td>
</tr>
<tr>
<td>poly</td>
<td>25</td>
</tr>
<tr>
<td>elec (poly2)</td>
<td>26</td>
</tr>
<tr>
<td>metal1</td>
<td>0.090000</td>
</tr>
<tr>
<td>metal3</td>
<td>0.050000</td>
</tr>
<tr>
<td>metal2</td>
<td>0.090000</td>
</tr>
<tr>
<td>highres</td>
<td>1192</td>
</tr>
</tbody>
</table>
You are to create a resistor of value approximately 5 KΩ (+/- 20 Ω) while minimizing the area of the resistor, without using highres. Extract the resistor to see its calculated value. You can ignore the resistance of the contacts for the purpose of this lab. Show this resistor (and its value) to your TA.

**Part 2: Introduction to bonding pads**

A bonding pad is used to connect the circuit on a die to a pin on a packaged chip. One side of a wire (often gold) connects to the bonding pad while the other side connects to the package. Although only the “top-metal” (metal3 for the AMI 0.5u process) is required to create a connection with the bonding wire, typically the bonding pad is made from all the metal layers stacked on top of each other and connected through vias. This arrangement allows connection from the core of the chip to the pad and, in turn, the outside world using any metal layer.

The last major processing step in the manufacturing of a die is the “passivation” layer (an insulator) that covers the entire chip to protect circuit from environmental contamination or minor damage on the surface. Since the bonding pads need to be accessible for electrical connection to the chip package, this top passivation layer must be removed from the bonding pads. This top passivation layer is termed the glass layer. As with all layers in a semiconductor process, the glass layer is governed by its own set of design rules (see Section 10 of MOSIS design rules).

**Part 2.1: Layout of a bonding pad**

Using the above information, create a bonding pad comprised of stacked layers of metal1, metal2, metal3 with a pad opening with the glass layer. Use the appropriate stacked vias (stacking of vias is allowed in the AMI 0.5u process) to interconnect these metal layers. Use the maximum possible number of vias to connect two adjacent metal layers. The pad should be as small as possible while still meeting design rules but the opening in the glass layer is to be 78µm x 78µm and this requirement is key in determining the lower bound for the area of the pad.

**Part 3: Pad Protection Circuitry**

Protecting the circuit from electro static discharge (ESD) induced damage is crucial. Typically, protection circuitry is designed by engineers specializing in ESD protection and is provided to the circuit designers. For the purpose of this lab, you are going to create a simple protection circuitry, not necessarily something that is reliable enough to be used in an actual circuit, but good enough to get you introduced to the idea of protecting from ESD damage.

The schematic of a simple protection circuit is shown on the next page. In this circuit, each diode protects the chip core connected to the die at the pad from any transient voltages beyond the power supply values. For example, a spike from the outside world, or excessive charge buildup at the gate of a transistor connected to the mid-point of the diodes would forward bias the top diode. Consequently, the diode will conduct and protect the core of the chip from getting...
damaged. The resistor is poly, at a resistance of -50 ohms.

**Part 3.1: Schematic of the ESD protection circuit**

Create a new cell (you may call it bondingPadWithESD or something similar) and enter the schematic of ESD circuitry described previously (the Pad is just a pin). This schematic will be used for LVS later.

**Part 3.2: Layout of a diode**

Diodes can be created two ways: p+ and n+ diffusions inside either an n-well or the substrate. For the purpose of this lab, we will layout each diode in its own n-well. For extraction to work correctly, you have to completely cover the two adjacent diffusions with the layer dio_id.

For this lab, the total area occupied by the protection circuit (both diodes) will be equal to the total area of the bonding pad itself. With this in mind, create the layout of one diode in a cell by itself and make sure that it extracts as a diode. We will ignore the electrical properties of this diode and focus only on the correct connectivity.

(Insert for old picture above)

**Part 3.3: Layout of the complete bonding pad**

With a layout of a single diode and a bonding pad available, you will now create a layout of bonding pad with ESD protection. Create a layout view of the cell bondingPadWithESD, instantiate the needed components, and complete the bonding pad design. Make sure you pass LVS. This complete bonding pad will be used later in the lab. Build a symbol for this protection circuitry.

We also must specify a model for the diodes. Create a diode model that tells the software how to model the diode in the schematic. To do so, create a text file called diode.scs and include the following text:

```
simulator lang = spectre
library dio
section d
```
For each diode, edit the property 'model' so that it says 'diode' in each. This will tell the simulator to use the file just created as the model. **Show your layout to the TA.**

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**Part 3.4: Human Body Model**

The human body model is an electrical equivalent of a human touching a circuit with static discharge. It is modeled as a 100pF capacitor discharging through a 1500 ohm resistor in series to the DUT. Devices are qualified into different classes depending upon how much voltage they can handle from this configuration. This of course corresponds to how much static electricity you build up before touching your device! The different classes can be found at the bottom of this page.

Create a new cell view and call it circuitry test. Add the human body model and your protection circuitry. Remember to hook up Vss and Vdd! Run the circuit to an output of 1pF. Set the starting voltage of the charged capacitor using the 'Initial Conditions' query in the properties of the 100pF capacitor. Set the starting voltage of the output capacitor to 0V.

**Before running your test circuit, tell the ADE to include the diode file created earlier.** To do so, goto the “Setup” menu and select “Model Libraries …”. Browse to where you saved the “diode.scs” file, type in “d” to the Section, and click on the “add” button. Proceed with the simulation (transient, etc.) as usual.
Run the circuit for a variety of starting voltages and see how the protection circuitry works. If we specify that any voltage above 5V destroys the circuitry, to what class of devices would this belong? How would you improve the protection of the circuit?

<table>
<thead>
<tr>
<th>Class</th>
<th>ESD withstand voltage, $V_w$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 ~ 250 V</td>
</tr>
<tr>
<td>1A</td>
<td>250 ~ 500 V</td>
</tr>
<tr>
<td>1B</td>
<td>500 ~ 1000 V</td>
</tr>
<tr>
<td>1C</td>
<td>1000 ~ 2000 V</td>
</tr>
<tr>
<td>2</td>
<td>2000 ~ 4000 V</td>
</tr>
<tr>
<td>3A</td>
<td>4000 ~ 8000 V</td>
</tr>
<tr>
<td>3B</td>
<td>&gt; 8000 V</td>
</tr>
</tbody>
</table>

Show your output to the TA.

**Deliverables**

1. Resistor
2. Bonding Pad Layout
3. Human Body Model