EE 330
Lecture 10

IC Fabrication Technology
- Interconnects
- Back-end Processes

Devices in Semiconductor Processes
Quiz 9  What is the major reason shallow trench isolation (STI) is used instead of Local Oxidation to create the field oxide in a MOS process?
And the number is ....
And the number is ....
Quiz 9

What is the major reason shallow trench isolation (STI) is used instead of Local Oxidation to create the field oxide in a MOS process?

Solution:

STI helps keep the surface of the wafer planar
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Review from Last Time

Etching

Selective Removal of Unwanted Materials

• Wet Etch
  – Inexpensive but under-cutting a problem

• Dry Etch
  – Often termed ion etch or plasma etch
Diffusion

• Controlled Migration of Impurities
  – Time and Temperature Dependent
  – Both vertical and lateral diffusion occurs
  – Crystal orientation affects diffusion rates in lateral and vertical dimensions
  – Materials Dependent
  – Subsequent Movement
  – Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  – Diffusion at 800°C to 1200°C

• Source of Impurities
  – Deposition
  – Ion Implantation
    • Only a few Å deep
    • More accurate control of doping levels
    • Fractures silicon crystalline structure during implant
    • Annealing occurs during diffusion
Oxidation

- SiO$_2$ is widely used as an insulator
  - Excellent insulator properties
- Used for gate dielectric
  - Gate oxide layers very thin
- Used to separate devices by raising threshold voltage
  - Treated as field oxide
  - Field oxide layers very thick
- Methods of Oxidation
  - Thermal Growth (LOCOS)
    - Consumes host silicon
    - $x$ units of SiO$_2$ consumes $0.47x$ units of Si
    - Undercutting of photoresist
    - Compromises planar surface for thick layers
    - Excellent quality
  - Chemical Vapor Deposition
    - Needed to put SiO$_2$ on materials other than Si
Epitaxy

• Single Crystaline Extension of Substrate Crystal
  – Commonly used in bipolar processes
  – CVD techniques
  – Impurities often added during growth
  – Grows slowly to allow alignment with substrate
Polysilicon

- Elemental contents identical to that of single crystalline silicon
  - Electrical properties much different
  - If doped heavily makes good conductor
  - If doped moderately makes good resistor
  - Widely used for gates of MOS devices
  - Widely used to form resistors
  - Grows fast over non-crystalline surface
  - Silicide often used in regions where resistance must be small
    - Refractory metal used to form silicide
    - Designer must indicate where silicide is applied (or blocked)
Review from Last Time

Polysilicon

Single-Crystaline Silicon
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Ion Implantation
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Contacts, Interconnect and Metalization

• Contacts usually of a fixed size
  – All etches reach bottom at about the same time
  – Multiple contacts widely used
  – Contacts not allowed to Poly on thin oxide in most processes
  – Dog-bone often needed for minimum-length devices
Contacts

Unacceptable Contact

Vulnerable to pin holes
(usually all contacts are same size)

Acceptable Contact
Contacts

Acceptable Contact
Contacts

Design Rule Violation

“Dog Bone” Contact
Contacts

Common Circuit Connection

Standard Interconnection

Buried Contact

Can save area but not allowed in many processes
Metalization

- Aluminum widely used for interconnect
- Copper finding some applications
- Must not exceed maximum current density
  - around 1ma/u
- Ohmic Drop must be managed
- Parasitic Capacitances must be managed
- Interconnects from high to low level metals require connections to each level of metal
- Stacked vias permissible in some processes
Multiple Level Interconnects

3-rd level metal connection to n-active without stacked vias
Multiple Level Interconnects

3-rd level metal connection to n-active with stacked vias
Interconnects

• Metal is preferred interconnect
  – Because conductivity is high
• Parasitic capacitances and resistances of concern in all interconnects
• Polysilicon used for short interconnects
  – Silicided to reduce resistance
  – Unsilicided when used as resistors
• Diffusion used for short interconnects
  – Parasitic capacitances are high
Interconnects

• Metal is preferred interconnect
  – Because conductivity is high

Parasitic capacitances and resistances of concern in all interconnects

• Polysilicon used for short interconnects
  – Silicided to reduce resistance
  – Unsilicided when used as resistors

• Diffusion used for short interconnects
  – Parasitic capacitances are high
Resistance in Interconnects
Resistance in Interconnects

\[ R = \frac{L}{A} \rho \]

\[ A = HW \]

\(\rho\) independent of geometry and characteristic of the process
H \ll W \text{ and } H \ll L \text{ in most processes}
Interconnect behaves as a "thin" film
Sheet resistance often used instead of conductivity to characterize film

\[ R = \frac{L}{A} \rho = \frac{L}{W} \left[ \frac{\rho}{H} \right] \]

\[ R_{\square} = \rho/H \quad \text{and} \quad R = R_{\square} [L / W] \]
Resistance in Interconnects

\[ R = R_\square \left[ \frac{L}{W} \right] \]

The “Number of Squares” approach to resistance determination in thin films

\[ N_S = 21 \]

\[ \frac{L}{W} = 21 \]

\[ R = R_\square N_S \]
Resistance in Interconnects

Corners Contribute about .55 Squares

Fractional Squares Can Be Represented By Their Fraction

The “squares” approach is not exact but is good enough for calculating resistance in almost all applications

In this example:

\[ N_S = 12 + .55 + .7 = 13.25 \]

\[ R = R_{\square} \cdot 13.25 \]
Example:

The layout of a film resistor with electrodes A and B is shown. If the sheet resistance of the film is 40 $\Omega/\square$, determine the resistance between nodes A and B.
Solution

\[ N_S = 9 + 9 + 3 + 2 \times 0.55 = 22.1 \]

\[ R_{AB} = R_{\square} N_S = 40 \times 22.1 = 884 \text{\Omega} \]
Resistance in Interconnects
(can be used to build resistors!)

• Serpentine often used when large resistance *required*
• Polysilicon or diffusion often used for resistor creation
• Effective at managing the aspect ratio of large resistors
• May include hundreds or even thousands of squares
Resistance in Interconnects
(can be used to build resistors!)

Area requirements determined by both minimum width and minimum spacing design rules
Capacitance in Interconnects

\[ C = C_D A \]

\( C_D \) is the capacitance density and \( A \) is the area of the overlap.
Capacitance in Interconnects

Equivalent Circuit

\[ C_{12} = CD_{12} A_5 \]
\[ C_{1S} = CD_{1S} (A_1 + A_2 + A_5) \]
\[ C_{2S} = CD_{2S} (A_3 + A_4) \]
Example

Two metal layers, Metal 1 and Metal 2, are shown. Both are above field oxide. Determine the capacitance between Metal 1 and Metal 2. Assume the process has capacitance densities from $M_1$ to substrate of $0.05\text{fF/}\mu\text{m}^2$, from $M_1$ to $M_2$ of $0.07\text{fF/}\mu\text{m}^2$ and from $M_2$ to substrate of $0.025\text{fF/}\mu\text{m}^2$. 
Example

Solution

\[ A_{C1C2} = (20\mu)^2 = 400\mu^2 \]

The capacitance density from \( M_1 \) to \( M_2 \) is \( .07fF/\mu^2 \)

\[ C_{12} = A_{C1C2} \cdot C_{D12} = 400\mu^2 \cdot 0.07fF/\mu^2 = 28fF \]
Capacitance and Resistance in Interconnects

• See MOSIS WEB site for process parameters that characterize parasitic resistances and capacitances

www.mosis.org
MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU
TECHNOLOGY: SCN05

VENDOR: AMIS
FEATURE SIZE: 0.5 microns

Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

<table>
<thead>
<tr>
<th>TRANSISTOR PARAMETERS</th>
<th>W/L</th>
<th>N-CHANNEL</th>
<th>P-CHANNEL</th>
<th>UNITS</th>
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<tr>
<td>MINIMUM</td>
<td>3.0/0.6</td>
<td>0.79</td>
<td>-0.92</td>
<td>volts</td>
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<td>Vth</td>
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<td></td>
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<tr>
<td>SHORT</td>
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<td>uA/um</td>
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<tr>
<td>Vpt</td>
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<td>Gamma</td>
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<td>V^0.5</td>
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<tr>
<td>K' (Uo*Cox/2)</td>
<td>56.4</td>
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<td>uA/V^2</td>
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<tr>
<td>Low-field Mobility</td>
<td>463.87</td>
<td>149.69</td>
<td>cm^2/V*s</td>
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</table>

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

<table>
<thead>
<tr>
<th>Design Technology</th>
<th>XL (um)</th>
<th>XW (um)</th>
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</thead>
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SCMOS_SUBM (\(\lambda=0.30\)) & 0.10 & 0.00 \\
SCMOS (\(\lambda=0.35\)) & 0.00 & 0.20 \\

<table>
<thead>
<tr>
<th>FOX TRANSISTORS</th>
<th>GATE</th>
<th>N+ACTIVE</th>
<th>P+ACTIVE</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>Vth</td>
<td>Poly</td>
<td>&gt;15.0</td>
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<td>volts</td>
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<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2 HR</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
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<tr>
<td>Sheet Resistance</td>
<td>83.5</td>
<td>105.3</td>
<td>23.5</td>
<td>999</td>
<td>44.2</td>
<td>0.09</td>
<td>0.10</td>
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<td>Contact Resistance</td>
<td>64.9</td>
<td>149.7</td>
<td>17.3</td>
<td></td>
<td>29.2</td>
<td>0.97</td>
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<td>ohms</td>
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<td>Gate Oxide Thickness</td>
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<tr>
<th>PROCESS PARAMETERS</th>
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<th>N(\backslash)PLY</th>
<th>N_W</th>
<th>UNITS</th>
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<tr>
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<td>824</td>
<td>816</td>
<td>ohms/sq</td>
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<tr>
<td>Contact Resistance</td>
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<td>ohms</td>
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**COMMENTS:** N\(\backslash\)POLY is N-well under polysilicon.

<table>
<thead>
<tr>
<th>CAPACITANCE PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>N_W</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>Area (substrate)</td>
<td>425</td>
<td>731</td>
<td>84</td>
<td>27</td>
<td>12</td>
<td>7</td>
<td>37</td>
<td>aF/(\mu)m(^2)</td>
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<tr>
<td>Area (N+active)</td>
<td>2434</td>
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<td>35</td>
<td>16</td>
<td>11</td>
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<td>aF/(\mu)m(^2)</td>
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<tr>
<td>Area (P+active)</td>
<td>2335</td>
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<td></td>
<td>aF/(\mu)m(^2)</td>
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<tr>
<td>Area (poly)</td>
<td>938</td>
<td>56</td>
<td>15</td>
<td>9</td>
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<td>aF/(\mu)m(^2)</td>
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<td>Area (poly2)</td>
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<td>Area (metal1)</td>
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<td>aF/(\mu)m(^2)</td>
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<td>Fringe (substrate)</td>
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<td>238</td>
<td>49</td>
<td>33</td>
<td>23</td>
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<td>Fringe (poly)</td>
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<td>Fringe (metal1)</td>
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<tr>
<td>Overlap (N+active)</td>
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<td>aF/(\mu)m</td>
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<tr>
<td>Overlap (P+active)</td>
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<td>aF/(\mu)m</td>
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<td>Inverters K</td>
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<td>Vinv</td>
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<tr>
<td>Vinv</td>
<td>1.5</td>
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<tr>
<td>Vol (100 uA)</td>
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</table>
Voh (100 uA)  2.0  4.85 volts
Vinv  2.0  2.46 volts
Gain  2.0  -19.72

Ring Oscillator Freq.
DIV256 (31-stg,5.0V)  95.31 MHz
D256_WIDE (31-stg,5.0V)  147.94 MHz

Ring Oscillator Power
DIV256 (31-stg,5.0V)  0.49 uW/MHz/gate
D256_WIDE (31-stg,5.0V)  1.01 uW/MHz/gate

COMMENTS: SUBMICRON

□ T6AU SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jan 11/07
* LOT: T6AU  WAF: 7101
* Temperature_parameters=Default

.MODELS CMOSN NMOS 

+VERSION = 3.1  TNOM = 27  TOX = 1.42E-8
+XJ = 1.5E-7  NCH = 1.7E17  VTH0 = 0.629035
+K1 = 0.8976376  K2 = -0.09255  K3 = 24.0984767
+K3B = -8.2369696  W0 = 1.041146E-8  NLX = 1E-9
+DVTOW = 0  DVT1W = 0  DVT2W = 0
+DVT0 = 2.7123969  DVT1 = 0.4232931  DVT2 = -0.1403765
+U0 = 451.2322004  UA = 3.091785E-13  UB = 1.702517E-18
+UC = 1.22401E-11  VSAT = 1.715884E5  A0 = 0.6580918
+AGS = 0.130484  B0 = 2.446405E-6  B1 = 5E-6
+KETA = -3.043349E-3  A1 = 8.18159E-7  A2 = 0.3363058
+RDSW = 1.36705E5E3  PRWG = 0.0328586  PRWB = 0.0104806
+WR = 1  WINT = 2.443677E-7  LINT = 6.999776E-8
+XL = 1E-7  XW = 0  DWG = -1.256454E-8
+DWB = 3.676235E-8  VOFF = -1.493503E-4  NFACTOR = 1.0354201
+CIT = 0  CDSC = 2.4E-4  CDSCD = 0
+CDSCB = 0  ETA0 = 2.342963E-3  ETAB = -1.5324E-4
+DSUB = 0.0764123  PCLM = 2.5941582  PDIBLC1 = 0.8187825
+PDIBLC2 = 2.366707E-3  PDIBLCB = -0.0431505  DROUT = 0.9919348
+PSCBE1 = 6.611774E8  PSCBE2 = 3.238266E-4  FVAG = 0
+DELT A = 0.01  RSH = 83.5  MOBMOD = 1
+PRT  =  0  UTE  =  -1.5  KT1  =  -0.11
+KT1L  =  0  KT2  =  0.022  UA1  =  4.31E-9
+UB1  =  -7.61E-18  UC1  =  -5.6E-11  AT  =  3.3E4
+WL  =  0  WLN  =  1  WW  =  0
+WWN  =  1  WWL  =  0  LL  =  0
+LLN  =  1  LW  =  0  LWN  =  1
+LWL  =  0  CAPMOD  =  2  KPART  =  0.5
+CGDO  =  2.32E-10  CGSO  =  2.32E-10  CGBO  =  1E-9
+CJ  =  4.282017E-4  PB  =  0.9317787  MJ  =  0.4495867
+CJSW  =  3.034055E-10  PBSW  =  0.8  MJSW  =  0.1713852
+CJSWG  =  1.64E-10  PBSWG  =  0.8  MJSWG  =  0.1713852
+CF  =  0  PVTH0  =  0.0520855  PRDSW  =  112.8875816
+PK2  =  -0.0289036  WKETA  =  -0.0237483  LKETA  =  1.728324E-3
*
.MMODEL CMOSF_PMOS {
+VERSION  =  3.1  TNOM  =  27  TOX  =  1.42E-8
+XJ  =  1.5E-7  NCH  =  1.7E17  VTH0  =  -0.9232867
+K1  =  0.5464347  K2  =  8.119291E-3  K3  =  5.1623206
+K3B  =  -0.8373484  W0  =  1.30945E-8  NLX  =  5.772187E-8
+DVTOW  =  0  DVT1W  =  0  DVT2W  =  0
+DVT0  =  -2.0973823  DVT1  =  -0.5356454  DVT2  =  -0.1185455
+U0  =  220.5922586  UA  =  3.144939E-9  UB  =  1E-21
+UC  =  -6.19354E-11  VSAT  =  1.176415E5  A0  =  0.8441929
+AGS  =  0.1447245  B0  =  1.149181E-6  B1  =  5E-6
+KETA  =  -1.093365E-3  A1  =  3.467482E-4  A2  =  0.4667486
+RDSW  =  3E3  PRWG  =  -0.0418549  PRWB  =  -0.0212201
+WR  =  1  WINT  =  3.007497E-7  LLINT  =  1.040439E-7
+XL  =  1E-7  XW  =  0  DWG  =  -2.133869E-8
+DWB  =  1.706031E-8  VOFF  =  -0.0801591  NFACCTOR  =  0.9468597
+CIT  =  0  CDSC  =  2.4E-4  CDSCD  =  0
+CDSCB  =  0  ETA0  =  0.4060383  ETAB  =  -0.0633609
+DSUB  =  1  PCLM  =  2.2703293  PDIUBLC1  =  0.0279014
+FDBLBC2  =  3.20116E-3  FDBLBC  =  -0.057478  DROUT  =  0.1718548
+PSCBE1  =  4.876974E9  PSCBE2  =  5E-10  PVAG  =  0
+DELT A  =  0.01  RSH  =  105.3  MGBMOD  =  1
+PRT  =  0  UTE  =  -1.5  KT1  =  -0.11
+KT1L  =  0  KT2  =  0.022  UA1  =  4.31E-9
+UB1  =  -7.61E-18  UC1  =  -5.6E-11  AT  =  3.3E4
+WL  =  0  WLN  =  1  WW  =  0
+WWN  =  1  WWL  =  0  LL  =  0
+LLN  =  1  LW  =  0  LWN  =  1
+LWL  =  0  CAPMOD  =  2  KPART  =  0.5
+CGDO  =  3.12E-10  CGSO  =  3.12E-10  CGBO  =  1E-9
LEVEL  =  49
+CJ     =  7.254264E-4  PB     =  0.9682229  MJ     =  0.4969013
+CJSW   =  2.496599E-10 PBSW   =  0.99   MJSW   =  0.386204
+CJSWG  =  6.4E-11   PBSWG  =  0.99   MJSWG  =  0.386204
+CF     =  0          PVTH0  =  5.98016E-3 PRDSW  =  14.8598424
+PK2    =  3.73981E-3  WKETA  =  7.286716E-4 LKETA  =  -4.768569E-3  
*
**Consider Resistance and Capacitance Parameters**

<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2_HR</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>83.5</td>
<td>105.3</td>
<td>23.5</td>
<td>999</td>
<td>44.2</td>
<td>0.09</td>
<td>0.10</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>64.9</td>
<td>149.7</td>
<td>17.3</td>
<td></td>
<td>29.2</td>
<td>0.97</td>
<td></td>
<td>ohms</td>
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<tr>
<td>Gate Oxide Thickness</td>
<td>142</td>
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<td>angstrom</td>
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</table>

<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>M3</th>
<th>N\PLY</th>
<th>N_W</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>0.05</td>
<td>824</td>
<td>816</td>
<td>ohms/sq</td>
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<tr>
<td>Contact Resistance</td>
<td>0.79</td>
<td></td>
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<td>ohms</td>
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</table>

**COMMENTS:** N\POLY is N-well under polysilicon.

<table>
<thead>
<tr>
<th>CAPACITANCE PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>N_W</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>Area (substrate)</td>
<td>425</td>
<td>731</td>
<td>84</td>
<td></td>
<td>27</td>
<td>12</td>
<td>7</td>
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<td>aF/um^2</td>
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<tr>
<td>Area (N+active)</td>
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<td>35</td>
<td>16</td>
<td>11</td>
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<td>aF/um^2</td>
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<tr>
<td>Area (P+active)</td>
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<td></td>
<td></td>
<td></td>
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<td></td>
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<td>aF/um^2</td>
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<tr>
<td>Area (poly)</td>
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<td>938</td>
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<td>15</td>
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<tr>
<td>Area (poly2)</td>
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<td>aF/um^2</td>
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<tr>
<td>Area (metal1)</td>
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<td>aF/um^2</td>
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<tr>
<td>Area (metal2)</td>
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<td>aF/um^2</td>
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<tr>
<td>Fringe (substrate)</td>
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<td>238</td>
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<td>49</td>
<td>33</td>
<td>23</td>
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<td>aF/um</td>
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<tr>
<td>Fringe (poly)</td>
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<td>28</td>
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<td>aF/um</td>
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<tr>
<td>Fringe (metal1)</td>
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<td>34</td>
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<tr>
<td>Fringe (metal2)</td>
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<td>Overlap (N+active)</td>
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<td>aF/um</td>
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<tr>
<td>Overlap (P+active)</td>
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<td></td>
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<td></td>
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<td>aF/um</td>
</tr>
</tbody>
</table>
Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6µ wide and 800µ long and compare that with the same interconnect if M₁ were used.

\[ n_{SQ} = \frac{800\,\mu}{0.6\,\mu} = 1333 \]

\[ A = (0.6\,\mu)(800\,\mu) = 480\,\mu^2 \]

\[ R_{POLY} = n_{SQ} R_{SH} = 23.5 \times 1333 = 31.3\,K\Omega \]

\[ C_{P-SUB} = A \times C_{DPS} = 480\,\mu^2 \times 85\,aF\,\mu^{-2} = 40.8\,fF \]
Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6µ wide and 800µ long and compare that with the same interconnect if M1 were used.

\[ n_{sq} = \frac{800 \mu}{0.6 \mu} = 1333 \]

\[ A = (0.6 \mu)(800 \mu) = 480 \mu^2 \]

\[ R_{M1} = n_{SQ} R_{SH} = 0.09 \cdot 1333 = 120 \Omega \]

\[ C_{M1-SUB} = A \cdot C_{DM1S} = 480 \mu^2 \cdot 27 \text{aF} \mu^{-2} = 13.0 \text{fF} \]