EE 330
Lecture 10

IC Fabrication Technology  Part III
- Metalization and Interconnects
- Parasitic Capacitances
- Back-end Processes
Samsung topples Intel to become the world's largest chipmaker

Samsung has ended Intel's 25-year run as the world's biggest seller of chipsets after it posted its 2017 end of year financials.
This graphic shows global semiconductor industry sales each year from 1987 to 2018. In 2017, sales are expected to reach 409 billion U.S. dollars worldwide. Semiconductors are crucial components of electronics devices and the industry is highly competitive. The year-on-year growth rate in 2017 is expected to see growth rates of 20.6 percent. The largest semiconductor chip maker is Intel, which generated 54 billion U.S. dollars in revenue in 2016, placing it among the largest companies in terms of semiconductor industry revenues. A semiconductor is a substance that conducts electricity under some but not all circumstances. Manufacturers are able to
Global semiconductor industry revenue from 2009 to 2017, by vendor (in billion U.S. dollars)

This statistic shows the global revenue generated by the leading semiconductor vendors in the industry from 2009 to 2017. In 2017, Samsung was the leading semiconductor vendor with more than 61 billion U.S. dollars in revenue.

Semiconductor industry revenue - additional information

Intel was the leading vendor in the semiconductor industry in 2014 as the company generated revenue of over 50.8 billion U.S. dollars. This is a steady increase on the 33.4 billion U.S. dollar revenue it
Overall, Samsung's entire business reported full-year profit of KRW 53.65 trillion ($50.7 billion) on revenue of KRW 239.58 trillion, $225 billion. For the final quarter of 2017, revenue was KRW 65.98 trillion ($62 billion) with KRW 15.15 trillion ($14 billion) in operating profit.
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Ion Implantation
- Oxidation
- Epitaxy
- Polysilicon
- Planarization

→ Contacts, Interconnect and Metalization
Contacts

Vulnerable to pin holes
(usually all contacts are same size)

Acceptable Contact

Unacceptable Contact
Contacts

Acceptable Contact
Contacts

Design Rule Violation

“Dog Bone” Contact
Contacts

Common Circuit Connection

Standard Interconnection

Buried Contact

Can save area but not allowed in many processes
Metalization

- Aluminum widely used for interconnect
- Copper often replacing aluminum in recent processes
- Must not exceed maximum current density
  - around 1ma/u for aluminum and copper
- Ohmic Drop must be managed
- Parasitic Capacitances must be managed
- Interconnects from high to low level metals require connections to each level of metal
- Stacked vias permissible in some processes
Metalization

Aluminum

• Aluminum is usually deposited uniformly over entire surface and etched to remove unwanted aluminum

• Mask is used to define area in photoresist where aluminum is to be removed

Copper

• Plasma etches not effective at removing copper because of absence of volatile copper compounds

• Barrier metal layers needed to isolate silicon from migration of copper atoms

• Damascene or Dual-Damascene processes used to pattern copper
Patterning of Aluminum

Contact Opening from Mask

Photoresist
Patterning of Aluminum

Contact Opening after SiO$_2$ etch

Photoresist
Patterning of Aluminum

Contact Opening after SiO₂ etch

Photoresist
Patterning of Aluminum

Metal Applied to Entire Surface
Patterning of Aluminum

Photoresist Patterned with Metal Mask
Patterning of Aluminum

Aluminum After Metal Etch (photoresist still showing)
Copper Interconnects

Limitations of Aluminum Interconnects

- Electromigration
- Conductivity not real high

Relevant Key Properties of Copper

- Reduced electromigration problems at given current level
- Better conductivity

Challenges of Copper Interconnects

- Absence of volatile copper compounds (does not etch)
- Copper diffuses into surrounding materials (barrier metal required)
<table>
<thead>
<tr>
<th>Material</th>
<th>$\rho$ ($\Omega\cdot m$) at 20 °C</th>
<th>$\sigma$ (S/m) at 20 °C</th>
<th>Temperature coefficient (K$^{-1}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Carbon (graphene)</td>
<td>$1.00 \times 10^{-8}$</td>
<td>$1.00 \times 10^{8}$</td>
<td>$-0.0002$</td>
</tr>
<tr>
<td>Silver</td>
<td>$1.59 \times 10^{-8}$</td>
<td>$6.30 \times 10^{7}$</td>
<td>$0.0038$</td>
</tr>
<tr>
<td>Copper</td>
<td>$1.68 \times 10^{-8}$</td>
<td>$5.96 \times 10^{7}$</td>
<td>$0.003862$</td>
</tr>
<tr>
<td>Annealed copper[^note 2]</td>
<td>$1.72 \times 10^{-8}$</td>
<td>$5.80 \times 10^{7}$</td>
<td>$0.00393$</td>
</tr>
<tr>
<td>Gold[^note 3]</td>
<td>$2.44 \times 10^{-8}$</td>
<td>$4.10 \times 10^{7}$</td>
<td>$0.0034$</td>
</tr>
<tr>
<td>Aluminium[^note 4]</td>
<td>$2.82 \times 10^{-8}$</td>
<td>$3.50 \times 10^{7}$</td>
<td>$0.0039$</td>
</tr>
<tr>
<td>Calcium</td>
<td>$3.36 \times 10^{-8}$</td>
<td>$2.98 \times 10^{7}$</td>
<td>$0.0041$</td>
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<tr>
<td>Tungsten</td>
<td>$5.60 \times 10^{-8}$</td>
<td>$1.79 \times 10^{7}$</td>
<td>$0.0045$</td>
</tr>
<tr>
<td>Zinc</td>
<td>$5.90 \times 10^{-8}$</td>
<td>$1.69 \times 10^{7}$</td>
<td>$0.0037$</td>
</tr>
<tr>
<td>Nickel</td>
<td>$6.99 \times 10^{-8}$</td>
<td>$1.43 \times 10^{7}$</td>
<td>$0.006$</td>
</tr>
<tr>
<td>Lithium</td>
<td>$9.28 \times 10^{-8}$</td>
<td>$1.08 \times 10^{7}$</td>
<td>$0.006$</td>
</tr>
<tr>
<td>Iron</td>
<td>$9.71 \times 10^{-8}$</td>
<td>$1.00 \times 10^{7}$</td>
<td>$0.005$</td>
</tr>
<tr>
<td>Platinum</td>
<td>$1.06 \times 10^{-7}$</td>
<td>$9.43 \times 10^{6}$</td>
<td>$0.00392$</td>
</tr>
<tr>
<td>Tin</td>
<td>$1.09 \times 10^{-7}$</td>
<td>$9.17 \times 10^{6}$</td>
<td>$0.0045$</td>
</tr>
<tr>
<td>Carbon steel (1010)</td>
<td>$1.43 \times 10^{-7}$</td>
<td>$6.99 \times 10^{6}$</td>
<td></td>
</tr>
<tr>
<td>Material</td>
<td>$\sigma$ (A·m$^{-1}$)</td>
<td>$\rho$ (Ω·m)</td>
<td>$\mu$ (H·m$^{-1}$)</td>
</tr>
<tr>
<td>-------------------------------</td>
<td>-------------------------</td>
<td>----------------</td>
<td>-------------------</td>
</tr>
<tr>
<td>Lead</td>
<td>$2.20 \times 10^{-7}$</td>
<td>$4.55 \times 10^6$</td>
<td>0.0039</td>
</tr>
<tr>
<td>Titanium</td>
<td>$4.20 \times 10^{-7}$</td>
<td>$2.38 \times 10^6$</td>
<td>0.0038</td>
</tr>
<tr>
<td>Grain oriented electrical steel</td>
<td>$4.60 \times 10^{-7}$</td>
<td>$2.17 \times 10^6$</td>
<td></td>
</tr>
<tr>
<td>Manganin</td>
<td>$4.82 \times 10^{-7}$</td>
<td>$2.07 \times 10^6$</td>
<td>0.000002</td>
</tr>
<tr>
<td>Constantan</td>
<td>$4.90 \times 10^{-7}$</td>
<td>$2.04 \times 10^6$</td>
<td>0.000008</td>
</tr>
<tr>
<td>Stainless steel$^{[5]}$</td>
<td>$6.90 \times 10^{-7}$</td>
<td>$1.45 \times 10^6$</td>
<td>0.00094</td>
</tr>
<tr>
<td>Mercury</td>
<td>$9.80 \times 10^{-7}$</td>
<td>$1.02 \times 10^6$</td>
<td>0.0009</td>
</tr>
<tr>
<td>Nichrome$^{[6]}$</td>
<td>$1.10 \times 10^{-6}$</td>
<td>$6.7 \times 10^5$</td>
<td>0.0004</td>
</tr>
<tr>
<td>GaAs</td>
<td>$1.00 \times 10^{-3}$ to $1.00 \times 10^8$</td>
<td>$1.00 \times 10^{-8}$ to $10^3$</td>
<td>0.0004</td>
</tr>
<tr>
<td>Carbon (amorphous)</td>
<td>$5.00 \times 10^{-4}$ to $8.00 \times 10^{-4}$</td>
<td>$1.25 \times 10^3$ to $2 \times 10^3$</td>
<td>$-0.0005$</td>
</tr>
<tr>
<td>Carbon (graphite)$^{[7]}$</td>
<td>$2.50 \times 10^{-6}$ to $5.00 \times 10^{-6}$</td>
<td></td>
<td>$2.00 \times 10^5$ to $3.00 \times 10^5$</td>
</tr>
<tr>
<td></td>
<td>$3.00 \times 10^{-3}$ $\parallel$ basal plane</td>
<td>$3.30 \times 10^2$ $\perpendicular$ basal plane</td>
<td></td>
</tr>
<tr>
<td>PEDOT:PSS</td>
<td>$2 \times 10^{-6}$ to $1 \times 10^{-1}$</td>
<td>$1 \times 10^1$ to $4.6 \times 10^5$</td>
<td>?</td>
</tr>
<tr>
<td>Germanium$^{[8]}$</td>
<td>$4.60 \times 10^{-1}$</td>
<td>2.17</td>
<td>$-0.048$</td>
</tr>
<tr>
<td>Sea water$^{[9]}$</td>
<td>$2.00 \times 10^{-1}$</td>
<td>4.80</td>
<td></td>
</tr>
<tr>
<td>Swimming pool water$^{[10]}$</td>
<td>$3.33 \times 10^{-1}$ to $4.00 \times 10^{-1}$</td>
<td>0.25 to 0.30</td>
<td></td>
</tr>
<tr>
<td>Material</td>
<td>resistivity × 10^2</td>
<td>permittivity × 10^-3</td>
<td>dielectric loss</td>
</tr>
<tr>
<td>----------------------------------</td>
<td>--------------------</td>
<td>----------------------</td>
<td>-----------------</td>
</tr>
<tr>
<td>Silicon</td>
<td>6.40 × 10²</td>
<td>1.56 × 10⁻³</td>
<td>−0.075</td>
</tr>
<tr>
<td>Wood (damp)</td>
<td>1.00 × 10³ to 1.00 × 10⁴</td>
<td>10⁻⁴ to 10⁻³</td>
<td></td>
</tr>
<tr>
<td>Deionized water</td>
<td>1.80 × 10⁵</td>
<td>5.50 × 10⁻⁶</td>
<td></td>
</tr>
<tr>
<td>Glass</td>
<td>1.00 × 10¹¹ to 1.00 × 10¹⁵</td>
<td>10⁻¹⁵ to 10⁻¹¹</td>
<td>?</td>
</tr>
<tr>
<td>Hard rubber</td>
<td>1.00 × 10¹³</td>
<td>10⁻¹⁴</td>
<td>?</td>
</tr>
<tr>
<td>Wood (oven dry)</td>
<td>1.00 × 10¹⁴ to 1.00 × 10¹⁶</td>
<td>10⁻¹⁶ to 10⁻¹⁴</td>
<td></td>
</tr>
<tr>
<td>Sulfur</td>
<td>1.00 × 10¹⁵</td>
<td>10⁻¹⁶</td>
<td>?</td>
</tr>
<tr>
<td>Air</td>
<td>1.30 × 10¹⁴ to 3.30 × 10¹⁴</td>
<td>3 × 10⁻¹⁵ to 8 × 10⁻¹⁵</td>
<td></td>
</tr>
<tr>
<td>Carbon (diamond)</td>
<td>1.00 × 10¹²</td>
<td>~10⁻¹³</td>
<td></td>
</tr>
<tr>
<td>Fused quartz</td>
<td>7.50 × 10¹⁷</td>
<td>1.30 × 10⁻¹⁸</td>
<td>?</td>
</tr>
<tr>
<td>PET</td>
<td>1.00 × 10²¹</td>
<td>10⁻²¹</td>
<td>?</td>
</tr>
<tr>
<td>Teflon</td>
<td>1.00 × 10²³ to 1.00 × 10²⁵</td>
<td>10⁻²⁵ to 10⁻²³</td>
<td>?</td>
</tr>
</tbody>
</table>
Copper Interconnects

Practical methods of realizing copper interconnects took many years to develop.

Copper interconnects widely used in some processes today.
Patterning of Copper

Damascene Process

Contact Opening after SiO$_2$ etch

Photoresist
Patterning of Copper

Damascene Process

Tungsten (W)

CMP Target

W has excellent conformality when formed from WF6
Chemical-Mechanical Planarization (CMP)

- Polishing Pad and Wafer Rotate in non-concentric pattern to thin, polish, and planarize surface
- Abrasive/Chemical polishing
- Depth and planarity are critical

Acknowledgement:
http://en.wikipedia.org/wiki/Chemical-mechanical_planarization
Patterning of Copper

Damascone Process

After first CMP Step

W-plug

CMP Target
Patterning of Copper

Damascene Process
After first CMP Step

Oxidation
Patterning of Copper

Damasocene Process

Photoresist Patterned with Metal Mask Defines Trench
Patterning of Copper

Damascene Process

Shallow Trench after Etch

W-plug
Patterning of Copper

Damascene Process

(BARRIER METAL ADDED BEFORE COPPER TO CONTAIN THE COPPER ATOMS)
Patterning of Copper

Damascene Process

W-plug

Copper Deposition
Patterning of Copper

Damascene Process

Copper Deposition

W-plug

CMP Target

Copper is deposited or electroplated (Barrier Metal Used for Electroplating Seed)
Patterning of Copper

Damascene Process

After Second CMP Step

W-plug

Copper

CMP Target
Patterning of Copper

Dual-Damascene Process

Shallow Trench Defined in PR with Metal Mask

Photoresist
Patterning of Copper

Dual-Damascene Process

Shallow Trench After Etch

Photoresist
Patterning of Copper

Dual-Damascene Process

Via Defined in PR with Via Mask

Photoresist
Patterning of Copper

Dual-Damascene Process

Via Etch Defines Contact Region

Photoresist

(Barrier Metal added before copper but not shown)
Patterning of Copper

Dual-Damascene Process

Copper Deposited on Surface

Copper is deposited or electroplated (Barrier Metal Used for Electroplating Seed)
Patterning of Copper

Dual-Damascene Process

Copper Deposited on Surface

CMP Target
Patterning of Copper

Dual-Damascene Process

Copper Via

Copper Interconnect

CMP Target
Patterning of Copper

Both Damascene Processes Realize Same Structure

**Damascene Process**
- Two Dielectric Deposition Steps
- Two CMP Steps
- Two Metal Deposition Steps
- Two Dielectric Etches
- W-Plug

**Dual-Damascene Process**
- One Dielectric Deposition Steps
- One CMP Steps
- One Metal Deposition Steps
- Two Dielectric Etches
- Via formed with metal step
Multiple Level Interconnects

3-rd level metal connection to n-active without stacked vias
Multiple Level Interconnects

3-rd level metal connection to n-active with stacked vias
Interconnect Layers May Vary in Thickness or Be Mostly Uniform

**FIG 4.30** Interconnect geometry

<table>
<thead>
<tr>
<th>Layer</th>
<th>t (nm)</th>
<th>w (nm)</th>
<th>s (nm)</th>
<th>AR</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>1720</td>
<td>860</td>
<td>860</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>1000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>1600</td>
<td>800</td>
<td>800</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>1000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1080</td>
<td>540</td>
<td>540</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>700</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>700</td>
<td>320</td>
<td>320</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>700</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>700</td>
<td>320</td>
<td>320</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>700</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>480</td>
<td>250</td>
<td>250</td>
<td>1.9</td>
</tr>
<tr>
<td></td>
<td>800</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FIG 4.31** Layer stack for 6-metal Intel 180 nm process

12.5μ
Interconnects

• Metal is preferred interconnect
  – Because conductivity is high
• Parasitic capacitances and resistances of concern in all interconnects
• Polysilicon used for short interconnects
  – Silicided to reduce resistance
  – Unsilicided when used as resistors
• Diffusion used for short interconnects
  – Parasitic capacitances are high
Interconnects

- Metal is preferred interconnect
  - Because conductivity is high

Parasitic capacitances and resistances of concern in all interconnects

- Polysilicon used for short interconnects
  - Silicided to reduce resistance
  - Unsilicided when used as resistors

- Diffusion used for short interconnects
  - Parasitic capacitances are high
Resistance in Interconnects
Resistance in Interconnects

\[ R = \frac{L}{A} \rho \]

\( \rho \) independent of geometry and characteristic of the process
Resistance in Interconnects

\[ R = \frac{L}{A} \rho = \frac{L}{W} \left[ \frac{\rho}{H} \right] \]

H \ll W and H \ll L in most processes
Interconnect behaves as a “thin” film
Sheet resistance often used instead of conductivity to characterize film

\[ R_\square = \rho/H \quad R = R_\square [L / W] \]
Resistance in Interconnects

The "Number of Squares" approach to resistance determination in thin films

\[ R = R_{\square} \left[ \frac{L}{W} \right] \]

\[ N_S = 21 \]

\[ L / W = 21 \]

\[ R = R_{\square} N_S \]
Resistance in Interconnects

The “squares” approach is not exact but is good enough for calculating resistance in almost all applications.

In this example:

\[ N_S = 12 + 0.55 + 0.7 = 13.25 \]

\[ R = R_\square 13.25 \]
Example:

The layout of a film resistor with electrodes A and B is shown. If the sheet resistance of the film is 40 $\Omega$/□, determine the resistance between nodes A and B.
Solution

\[ N_S = 9 + 9 + 3 + 2(0.55) = 22.1 \]

\[ R_{AB} = R \square N_S = 40 \times 22.1 = 884 \Omega \]
Resistance in Interconnects
(can be used to build resistors!)

- Serpentine often used when large resistance required
- Polysilicon or diffusion often used for resistor creation
- Effective at managing the aspect ratio of large resistors
- May include hundreds or even thousands of squares
Resistance in Interconnects
(can be used to build resistors!)

Area requirements determined by both minimum width and minimum spacing design rules
End of Lecture 10