EE 330
Lecture 10

IC Fabrication Technology
Part III
- Interconnects
- Back-end Processes
Quiz 9

What is the major reason shallow trench isolation (STI) is used instead of Local Oxidation to create the field oxide in a MOS process?
And the number is ....
And the number is ....
Quiz 9

What is the major reason shallow trench isolation (STI) is used instead of Local Oxidation to create the field oxide in a MOS process?

Solution:

STI helps keep the surface of the wafer planar.
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Implantation
- Etching
- Diffusion
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Etching

Selective Removal of Unwanted Materials

• Wet Etch
  – Inexpensive but under-cutting a problem

• Dry Etch
  – Often termed ion etch or plasma etch
Diffusion

• Controlled Migration of Impurities
  – Time and Temperature Dependent
  – Both vertical and lateral diffusion occurs
  – Crystal orientation affects diffusion rates in lateral and vertical dimensions
  – Materials Dependent
  – Subsequent Movement
  – Electrical Properties Highly Dependent upon Number and Distribution of Impurities
  – Diffusion at 800°C to 1200°C

• Source of Impurities
  – Deposition
  – Ion Implantation
    • Only a few Å deep
    • More accurate control of doping levels
    • Fractures silicon crystalline structure during implant
    • Annealing occurs during diffusion
Oxidation

- SiO$_2$ is widely used as an insulator
  - Excellent insulator properties
- Used for gate dielectric
  - Gate oxide layers very thin
- Used to separate devices by raising threshold voltage
  - termed field oxide
  - field oxide layers very thick
- Methods of Oxidation
  - Thermal Growth (LOCOS)
    - Consumes host silicon
    - $x$ units of SiO$_2$ consumes $0.47x$ units of Si
    - Undercutting of photoresist
    - Compromises planar surface for thick layers
    - Excellent quality
  - Chemical Vapor Deposition
    - Needed to put SiO$_2$ on materials other than Si
Review from Last Time

Epitaxy

• Single Crystaline Extension of Substrate Crystal
  – Commonly used in bipolar processes
  – CVD techniques
  – Impurities often added during growth
  – Grows slowly to allow alignment with substrate
Polysilicon

• Elemental contents identical to that of single crystaline silicon
  – Electrical properties much different
  – If doped heavily makes good conductor
  – If doped moderately makes good resistor
  – Widely used for gates of MOS devices
  – Widely used to form resistors
  – Grows fast over non-crystaline surface
  – Silicide often used in regions where resistance must be small
    • Refractory metal used to form silicide
    • Designer must indicate where silicide is applied (or blocked)
Review from Last Time

Polysilicon

Single-Crystaline Silicon
Interconnects

• Metal is preferred interconnect
  – Because conductivity is high

Parasitic capacitances and resistances of concern in all interconnects

• Polysilicon used for short interconnects
  – Silicided to reduce resistance
  – Unsilicided when used as resistors

• Diffusion used for short interconnects
  – Parasitic capacitances are high
Resistance in Interconnects
Resistance in Interconnects

\[ R = \frac{L}{A \rho} \]

\( A = HW \)

\( \rho \) independent of geometry and characteristic of the process
Resistance in Interconnects

H << W and H << L in most processes
Interconnect behaves as a “thin” film
Sheet resistance often used instead of conductivity to characterize film

\[ R = \frac{L}{A} \rho = \frac{L}{W} \left[ \frac{\rho}{H} \right] \]

\[ R_{\square} = \rho / H \]

\[ R = R_{\square} [L / W] \]
Resistance in Interconnects

The “Number of Squares” approach to resistance determination in thin films

\[ R = R_\square [L / W] \]

\[ N_S = 21 \]

\[ L / W = 21 \]

\[ R = R_\square N_S \]
Resistance in Interconnects

Fractional Squares Can Be Represented By Their Fraction

The “squares” approach is not exact but is good enough for calculating resistance in almost all applications

In this example:

\[ N_S = 12 + .55 + .7 = 13.25 \]

\[ R = R \_ {13.25} \]
Example:

The layout of a film resistor with electrodes A and B is shown. If the sheet resistance of the film is $40 \ \Omega/\square$, determine the resistance between nodes A and B.
Solution

\[ N_S = 9 + 9 + 3 + 2(0.55) = 22.1 \]

\[ R_{AB} = R_\square N_S = 40 \times 22.1 = 884 \Omega \]
Resistance in Interconnects
(can be used to build resistors!)

- Serpentine often used when large resistance required
- Polysilicon or diffusion often used for resistor creation
- Effective at managing the aspect ratio of large resistors
- May include hundreds or even thousands of squares
Resistance in Interconnects
(can be used to build resistors!)

Area requirements determined by both minimum width and minimum spacing design rules
Capacitance in Interconnects

\[ C = C_D A \]

\( C_D \) is the capacitance density and \( A \) is the area of the overlap.
Capacitance in Interconnects

Equivalent Circuit

\[ C_{12} = CD_{12} A_5 \]

\[ C_{1S} = CD_{1S} (A_1 + A_2 + A_5) \]

\[ C_{2S} = CD_{2S} (A_3 + A_4) \]
Example

Two metal layers, Metal 1 and Metal 2, are shown. Both are above field oxide. Determine the capacitance between Metal 1 and Metal 2. Assume the process has capacitance densities from $M_1$ to substrate of $0.05\text{fF}/\mu\text{m}^2$, from $M_1$ to $M_2$ of $0.07\text{fF}/\mu\text{m}^2$ and from $M_2$ to substrate of $0.025\text{fF}/\mu\text{m}^2$. 

![Diagram of two metal layers with dimensions and labels](image-url)
The capacitance density from $M_1$ to $M_2$ is $0.07\text{fF/µ}^2$.

Solution

\[ A_{C1C2} = (20\mu)^2 = 400\mu^2 \]

The capacitance density from $M_1$ to $M_2$ is $0.07\text{fF/µ}^2$.

\[ C_{12} = A_{C1C2} \cdot C_{D12} = 400\mu^2 \cdot 0.07\text{fF/µ}^2 = 28\text{fF} \]
Capacitance and Resistance in Interconnects

• See MOSIS WEB site for process parameters that characterize parasitic resistances and capacitances

www.mosis.org
MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU
TECHNOLOGY: SCN05
VENDOR: AMIS
FEATURE SIZE: 0.5 microns

Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

<table>
<thead>
<tr>
<th>TRANSISTOR PARAMETERS</th>
<th>W/L</th>
<th>N-CHANNEL</th>
<th>P-CHANNEL</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>MINIMUM</td>
<td>3.0/0.6</td>
<td>0.79</td>
<td>-0.92</td>
<td>volts</td>
</tr>
<tr>
<td>Vth</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SHORT</td>
<td>20.0/0.6</td>
<td>446</td>
<td>-239</td>
<td>uA/um</td>
</tr>
<tr>
<td>Idss</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vth</td>
<td>0.68</td>
<td></td>
<td>-0.90</td>
<td>volts</td>
</tr>
<tr>
<td>Vpt</td>
<td>10.0</td>
<td></td>
<td>-10.0</td>
<td>volts</td>
</tr>
<tr>
<td>WIDE</td>
<td>20.0/0.6</td>
<td>&lt; 2.5</td>
<td>&lt; 2.5</td>
<td>pA/um</td>
</tr>
<tr>
<td>Ids0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LARGE</td>
<td>50/50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vth</td>
<td>0.68</td>
<td></td>
<td>-0.95</td>
<td>volts</td>
</tr>
<tr>
<td>Vjbkd</td>
<td>10.9</td>
<td></td>
<td>-11.6</td>
<td>volts</td>
</tr>
<tr>
<td>Ijlk</td>
<td>&lt;50.0</td>
<td></td>
<td>&lt;50.0</td>
<td>pA</td>
</tr>
<tr>
<td>Gamma</td>
<td>0.48</td>
<td>0.58</td>
<td>V^0.5</td>
<td></td>
</tr>
<tr>
<td>K' (Uo*Cox/2)</td>
<td>56.4</td>
<td>-18.2</td>
<td>uA/V^2</td>
<td></td>
</tr>
<tr>
<td>Low-field Mobility</td>
<td>463.87</td>
<td>149.69</td>
<td>cm^2/V*s</td>
<td></td>
</tr>
</tbody>
</table>

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

<table>
<thead>
<tr>
<th>Design Technology</th>
<th>XL (um)</th>
<th>XW (um)</th>
</tr>
</thead>
</table>
### SCMOS_SUBM (lambda=0.30)

<table>
<thead>
<tr>
<th>FOX TRANSISTORS</th>
<th>GATE</th>
<th>N+ACTIVE</th>
<th>P+ACTIVE</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vth</td>
<td>Poly</td>
<td>&gt;15.0</td>
<td>&lt;-15.0</td>
<td>volts</td>
</tr>
</tbody>
</table>

### PROCESS PARAMETERS

<table>
<thead>
<tr>
<th>Sheet Resistance</th>
<th>83.5</th>
<th>105.3</th>
<th>23.5</th>
<th>999</th>
<th>44.2</th>
<th>0.09</th>
<th>0.10</th>
<th>ohms/sq</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contact Resistance</td>
<td>64.9</td>
<td>149.7</td>
<td>17.3</td>
<td>29.2</td>
<td>0.97</td>
<td></td>
<td></td>
<td>ohms</td>
</tr>
<tr>
<td>Gate Oxide Thickness</td>
<td>142</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>angstrom</td>
</tr>
</tbody>
</table>

### PROCESS PARAMETERS

<table>
<thead>
<tr>
<th>Sheet Resistance</th>
<th>0.05</th>
<th>824</th>
<th>816</th>
<th>ohms/sq</th>
</tr>
</thead>
<tbody>
<tr>
<td>Contact Resistance</td>
<td>0.79</td>
<td></td>
<td></td>
<td>ohms</td>
</tr>
</tbody>
</table>

**COMMENTS:** N\POLY is N-well under polysilicon.

### CAPACITANCE PARAMETERS

<table>
<thead>
<tr>
<th>Area (substrate)</th>
<th>425</th>
<th>731</th>
<th>84</th>
<th>27</th>
<th>12</th>
<th>7</th>
<th>37</th>
<th>aF/um^2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (N+active)</td>
<td>2434</td>
<td></td>
<td></td>
<td>35</td>
<td>16</td>
<td>11</td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (P+active)</td>
<td>2335</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (poly)</td>
<td>938</td>
<td>56</td>
<td>15</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (poly2)</td>
<td>49</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal1)</td>
<td>31</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal2)</td>
<td>35</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Fringe (substrate)</td>
<td>344</td>
<td>238</td>
<td>49</td>
<td>33</td>
<td>23</td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (poly)</td>
<td>59</td>
<td>38</td>
<td>28</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal1)</td>
<td>51</td>
<td>34</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal2)</td>
<td>52</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Overlap (N+active)</td>
<td>232</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Overlap (P+active)</td>
<td>312</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
</tbody>
</table>

### CIRCUIT PARAMETERS

<table>
<thead>
<tr>
<th>Inverters</th>
<th>K</th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Vinv</td>
<td>1.0</td>
<td>2.02</td>
<td>volts</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vinv</td>
<td>1.5</td>
<td>2.28</td>
<td>volts</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vol (100 uA)</td>
<td>2.0</td>
<td>0.13</td>
<td>volts</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Voh (100 uA)   2.0  4.85 volts
Vinv   2.0  2.46 volts
Gain   2.0  -19.72

Ring Oscillator Freq.
DIV256 (31-stg,5.0V)   95.31 MHz
D256_WIDE (31-stg,5.0V)  147.94 MHz

Ring Oscillator Power
DIV256 (31-stg,5.0V)   0.49 uW/MHz/gate
D256_WIDE (31-stg,5.0V) 1.01 uW/MHz/gate

COMMENTS: SUBMICRON

□ T6AU SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jan 11/07
* LOT: T6AU  WAF: 7101
* Temperature_parameters=Default

.MODEL CMOSN NMOS

+VERSION = 3.1
+XJ   = 1.5E-7
+K1   = 0.8976376
+K3B  = -8.2369696
+DVTOW = 0
+DVT0  = 2.7123969
+U0    = 451.2322004
+UC    = 1.22401E-11
+AGS   = 0.130484
+KETA  = -3.043349E-3
+RDSW  = 1.367055E3
+WR    = 1
+XL    = 1E-7
+DWB   = 3.676235E-8
+CIT   = 0
+CDSCB = 0
+DSUB  = 0.0764123
+PDIBLC2 = 2.366707E-3
+PSCE1  = 6.611774E8
+DELTA = 0.01

LEVEL = 49
TNOM   = 27
TOX    = 1.42E-8
NCH    = 1.7E17
VTH0   = 0.629035
K2     = -0.09255
K3     = 24.0984767
W0     = 1.041146E-8
NLX    = 1E-9
DVT1W   = 0
DVT1    = 0.4232931
DVT2    = -0.1403765
UA    = 3.091785E-13
UB    = 1.702517E-18
VSAT   = 1.715884E5
A0     = 0.6580918
B0     = 2.446405E-6
A1     = 8.18159E-7
A2     = 0.3363058
PRWG   = 0.0328586
PRWB   = 0.0104806
WINT   = 2.443677E-7
LINT   = 6.999776E-8
XW     = 0
VOFF   = -1.493503E-4
NFACTOR = 1.0354201
CDSC   = 2.4E-4
CDSCD  = 0
ETA0   = 2.342963E-3
ETAB   = -1.5324E-4
PCLM   = 2.5941582
PDIBLC1 = 0.8187825
PDIBLCB = -0.0431505
DROUT  = 0.9919348
PSCE2  = 3.238266E-4
PVAG   = 0
RSH    = 83.5
MOBMOD = 1
+PRT = 0  UTE = -1.5  KT1 = -0.11
+KT1L = 0  KT2 = 0.022  UA1 = 4.31E-9
+UB1 = -7.61E-18  UC1 = -5.6E-11  AT = 3.3E4
+WL = 0  WL1 = 1  WW = 0
+WWN = 1  WWL = 0  LL = 0
+LNN = 1  LW = 0  LWN = 1
+LWL = 0  CAPMOD = 2  XPART = 0.5
+CGDO = 2.32E-10  CGSO = 2.32E-10  CGBO = 1E-9
+CJ = 4.282017E-4  PB = 0.9317787  MJ = 0.4495867
+CJSW = 3.034055E-10  PBSW = 0.8  MJSW = 0.1713852
+CJSWG = 1.64E-10  PBSWG = 0.8  MJSWG = 0.1713852
+CF = 0  PVTH0 = 0.0520855  PRDSW = 112.8875816
+PK2 = -0.0289036  WKETA = -0.0237483  LKETA = 1.728324E-3

* .MODEL CMOS2 PMOS ( LEVEL = 49
+VERSION = 3.1  TNOM = 27  TOX = 1.42E-8
+XJ = 1.5E-7  NCH = 1.7E17  VTH0 = -0.9232867
+K1 = 0.5464347  K2 = 8.119291E-3  K3 = 5.1623206
+K3 = 0.8373484  W0 = 1.309458E-5  NLX = 5.772187E-8
+DVTOW = 0  DVT1W = 0  DVT2W = 0
+DVT0 = 2.0973823  DVT1 = 0.5356454  DVT2 = -0.1185455
+U0 = 220.5922586  UA = 3.144939E-9  UB = 1E-21
+UC = -6.19354E-11  VSAT = 1.176415E5  A0 = 0.8441929
+AGS = 0.1447245  B0 = 1.149181E6  B1 = 5E-6
+KETA = -1.093365E-3  A1 = 3.467482E-4  A2 = 0.4667486
+RDSW = 3E3  PRWG = -0.0418549  PRWB = -0.0212201
+WR = 1  WINT = 3.007497E-7  LINT = 1.040439E-7
+XL = 1E-7  XW = 0  DWG = -2.133809E-8
+DWB = 1.706031E-8  VOFF = -0.0801591  NFACTOR = 0.9468597
+CT = 0  CESC = 2.4E-4  CDSCD = 0
+CDSCB = 0  ETA0 = 0.4060383  ETAB = -0.0633609
+DSUB = 1  PCLM = 2.2703293  PDIBLC1 = 0.0279014
+PDIBLC2 = 3.201161E-3  PDIBLCB = -0.057478  DROUT = 0.1718548
+PSCBE1 = 4.876974E9  PSCBE2 = 5E-10  PVAG = 0
+DELT = 0.01  RSH = 105.3  MOBMOD = 1
+PRT = 0  UTE = -1.5  KT1 = -0.11
+KT1L = 0  KT2 = 0.022  UA1 = 4.31E-9
+UB1 = -7.61E-18  UC1 = -5.6E-11  AT = 3.3E4
+WL = 0  WL1 = 1  WW = 0
+WWN = 1  WWL = 0  LL = 0
+LNN = 1  LW = 0  LWN = 1
+LWL = 0  CAPMOD = 2  XPART = 0.5
+CGDO = 3.12E-10  CGSO = 3.12E-10  CGBO = 1E-9
+CJ       = 7.254264E-4  PB       = 0.9682229  MJ       = 0.4969013
+CJSW     = 2.496599E-10 PBSW     = 0.99   MJSW     = 0.386204
+CJSWG    = 6.4E-11    PBSWG    = 0.99   MJSWG    = 0.386204
+CF       = 0          PVTH0    = 5.98016E-3 PRDSW    = 14.8598424
+PK2      = 3.73981E-3 WKETA    = 7.286716E-4 LKETA    = -4.768569E-3
*

Consider Resistance and Capacitance Parameters

PROCESS PARAMETERS

<table>
<thead>
<tr>
<th></th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>PLY2_HR</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>83.5</td>
<td>105.3</td>
<td>23.5</td>
<td>999</td>
<td>44.2</td>
<td>0.09</td>
<td>0.10</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>64.9</td>
<td>149.7</td>
<td>17.3</td>
<td></td>
<td>29.2</td>
<td></td>
<td>0.97</td>
<td>ohms</td>
</tr>
<tr>
<td>Gate Oxide Thickness</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>angstrom</td>
</tr>
</tbody>
</table>

PROCESS PARAMETERS

<table>
<thead>
<tr>
<th></th>
<th>M3</th>
<th>N\PLY</th>
<th>N_W</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>0.05</td>
<td>824</td>
<td>816</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>0.79</td>
<td></td>
<td></td>
<td>ohms</td>
</tr>
</tbody>
</table>

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS

<table>
<thead>
<tr>
<th></th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>N_W</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (substrate)</td>
<td>425</td>
<td>731</td>
<td>84</td>
<td></td>
<td>27</td>
<td>12</td>
<td>7</td>
<td>37</td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (N+active)</td>
<td></td>
<td></td>
<td></td>
<td>2434</td>
<td>35</td>
<td>16</td>
<td>11</td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (P+active)</td>
<td></td>
<td></td>
<td></td>
<td>2335</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (poly)</td>
<td></td>
<td></td>
<td></td>
<td>938</td>
<td>56</td>
<td>15</td>
<td>9</td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (poly2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>49</td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal1)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>31</td>
<td>13</td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>35</td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Fringe (substrate)</td>
<td>344</td>
<td>238</td>
<td></td>
<td>49</td>
<td>33</td>
<td>23</td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (poly)</td>
<td></td>
<td></td>
<td></td>
<td>59</td>
<td>38</td>
<td>28</td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal1)</td>
<td></td>
<td></td>
<td></td>
<td>51</td>
<td>34</td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>52</td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Overlap (N+active)</td>
<td></td>
<td></td>
<td></td>
<td>232</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Overlap (P+active)</td>
<td></td>
<td></td>
<td></td>
<td>312</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
</tbody>
</table>