EE 330
Lecture 10

IC Fabrication Technology
Part III

- Resistance and Capacitance in Interconnects
- Back-end Processes

Devices in Semiconductor Processes

Review from Last Time

- Contacts usually of a fixed size
  - All etches reach bottom at about the same time
  - Multiple contacts widely used
  - Contacts not allowed to Poly on thin oxide in most processes
  - Dog-bone often needed for minimum-length devices

Review from Last Time

Metalization

- Aluminum widely used for interconnect
- Copper finding some applications
- Must not exceed maximum current density
  - around 1ma/u
- Ohmic Drop must be managed
- Parasitic Capacitances must be managed
- Interconnects from high to low level metals require connections to each level of metal
- Stacked vias permissible in some processes

Interconnect Layers May Vary in Thickness or Be Mostly Uniform

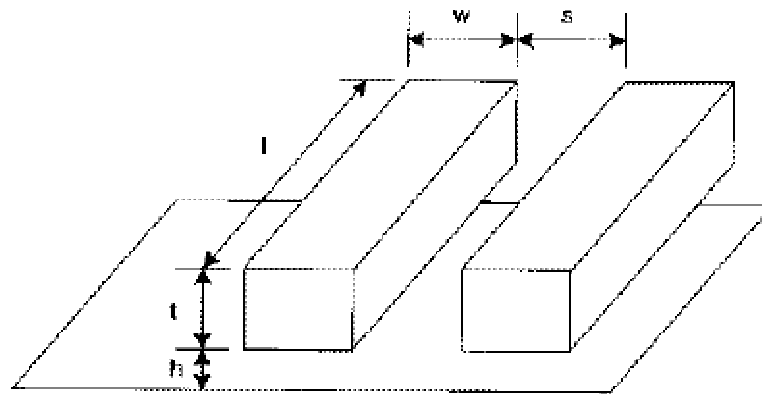
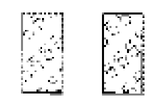
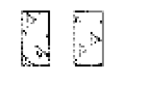
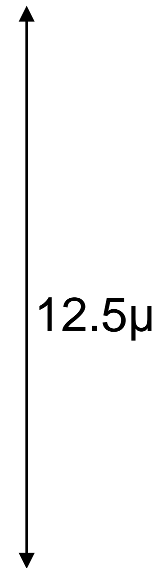


FIG 4.30 Interconnect geometry

Layer	t (nm)	w (nm)	s (nm)	AR
6	1720	860	860	2.0
	1000			
5	1600	800	800	2.0
	1000			
4	1080	540	540	2.0
	700			
3	700	320	320	2.2
	700			
2	700	320	320	2.2
	700			
1	480	250	250	1.9
	800			





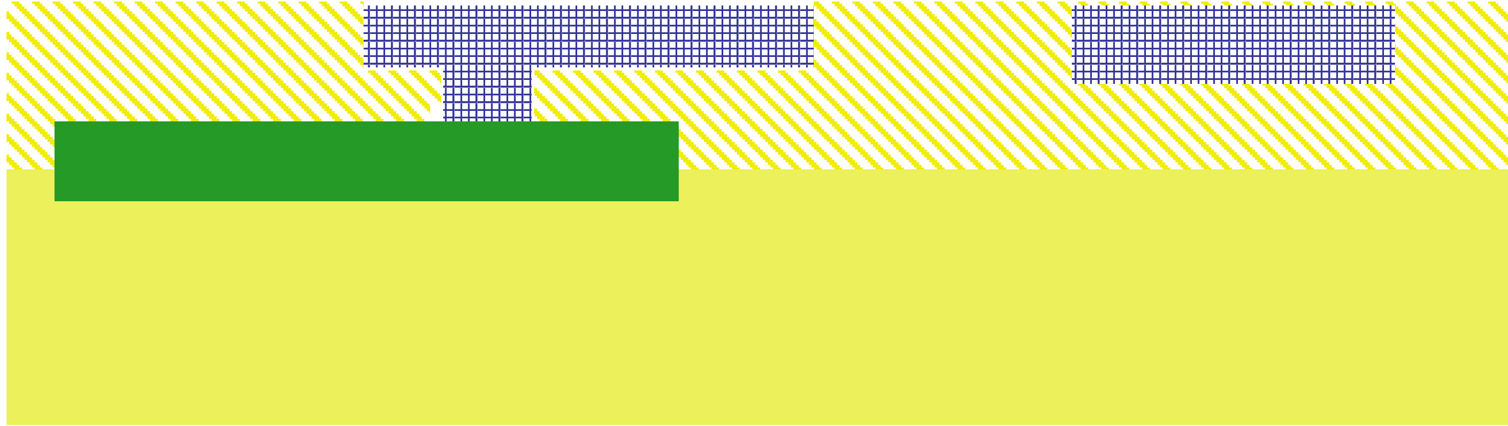


Substrate

FIG 4.31 Layer stack for 6-metal Intel 180 nm process

Review from Last Time

Patterning of Copper



Both Damascene Processes Realize Same Structure

Damascene Process

Two Dielectric Deposition Steps
Two CMP Steps
Two Metal Deposition Steps
Two Dielectric Etches
W-Plug

Dual-Damascene Process

One Dielectric Deposition Steps
One CMP Steps
One Metal Deposition Steps
Two Dielectric Etches
Via formed with metal step

Interconnects

- Metal is preferred interconnect
  - Because conductivity is high
- Parasitic capacitances and resistances of concern in all interconnects
- Polysilicon used for short interconnects
  - Silicided to reduce resistance
  - Unsilicided when used as resistors
- Diffusion used for short interconnects
  - Parasitic capacitances are high

Interconnects

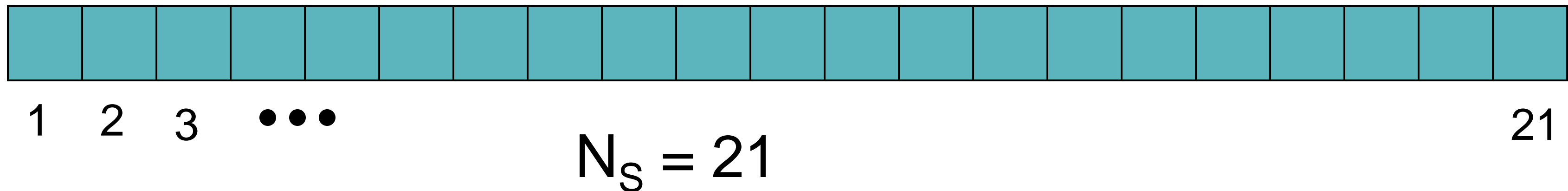
- Metal is preferred interconnect
  - Because conductivity is high
- Parasitic capacitances and resistances of concern in all interconnects
- Polysilicon used for short interconnects
  - Silicided to reduce resistance
  - Unsilicided when used as resistors
- Diffusion used for short interconnects
  - Parasitic capacitances are high

Review from Last Time

Resistance in Interconnects

R=R [L / W]

The “Number of Squares” approach to resistance determination in thin films



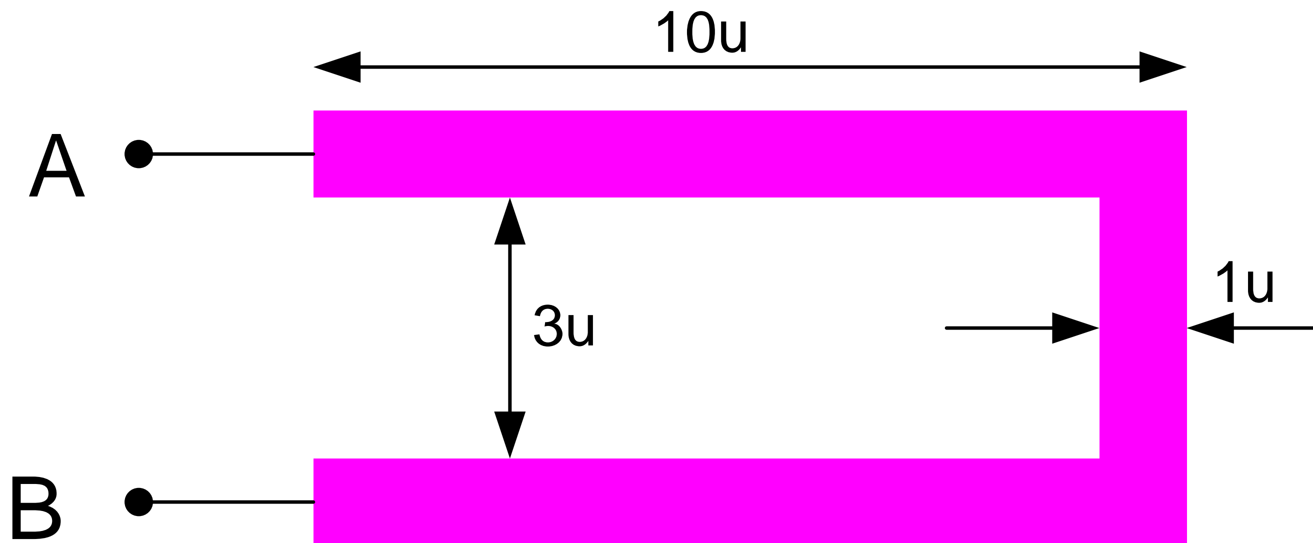
$N_S = 21$

$L / W = 21$

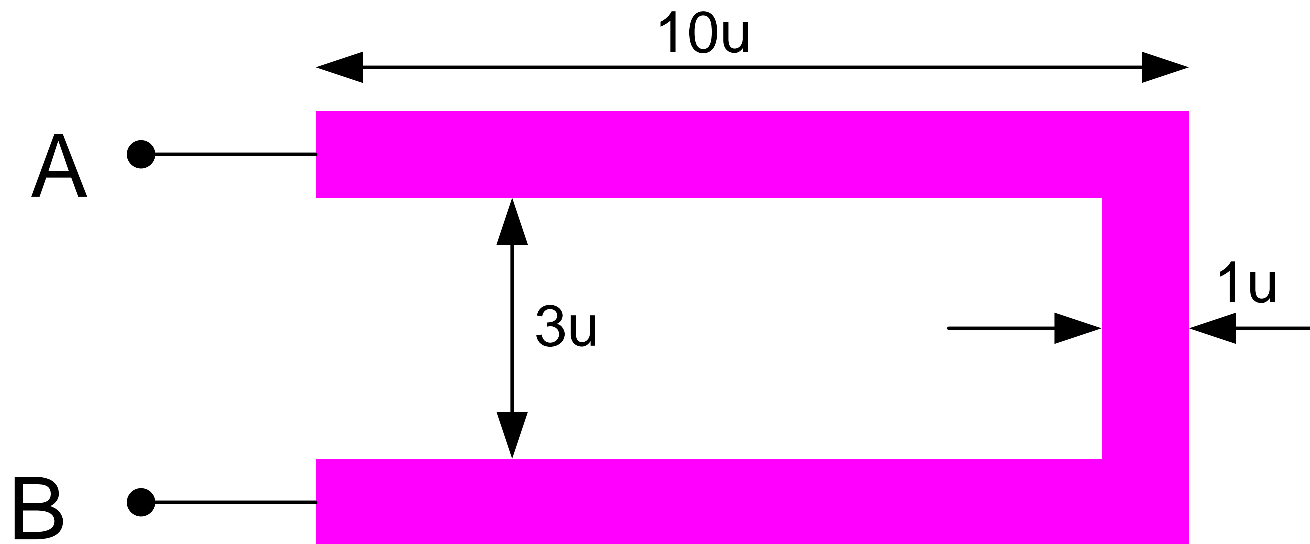
$R = R\ N_S$

Example:

The layout of a film resistor with electrodes A and B is shown. If the sheet resistance of the film is 40 Ω/ , determine the resistance between nodes A and B.



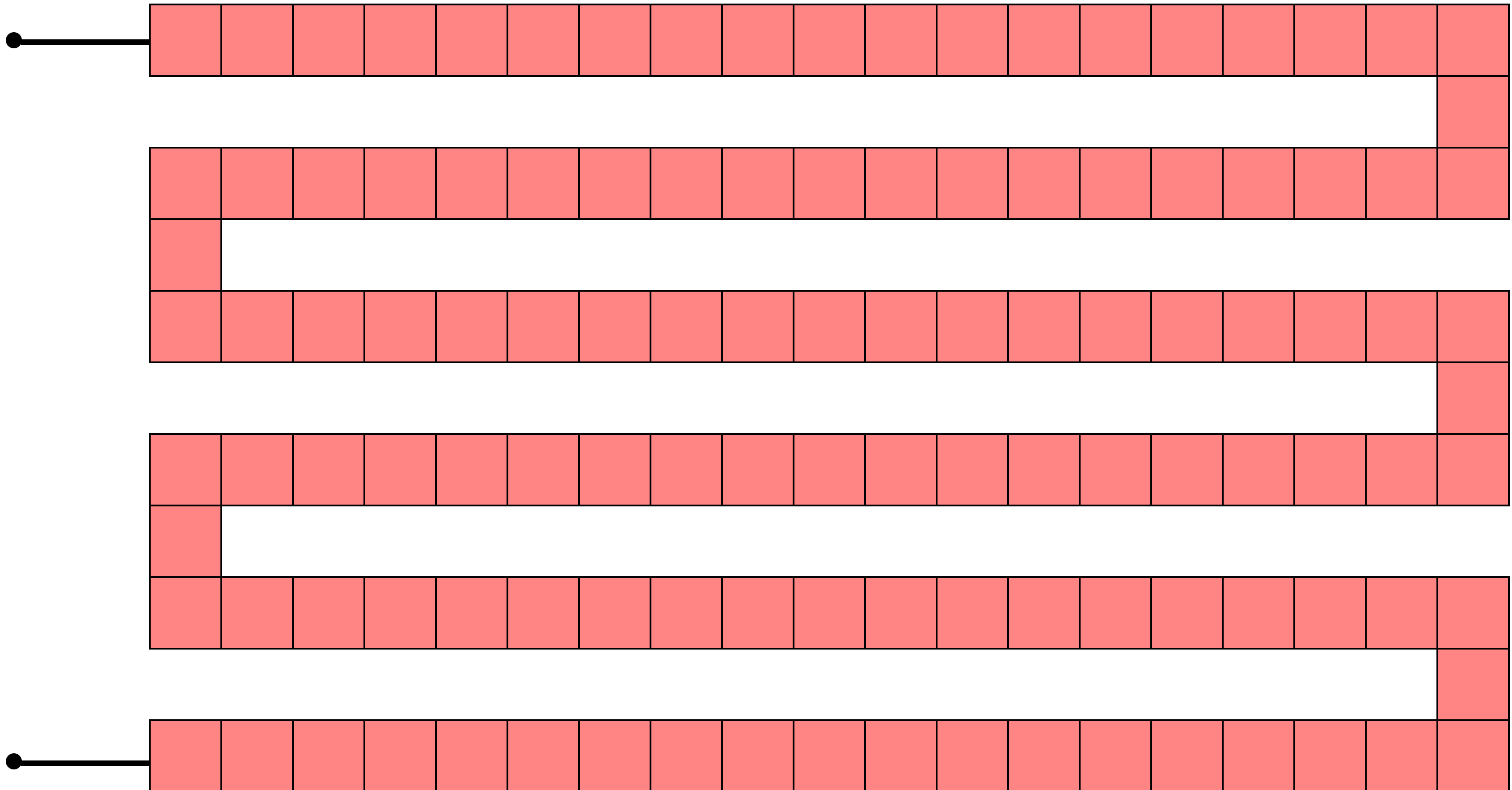
Solution



$$N_S = 9+9+3+2(.55) = 22.1$$

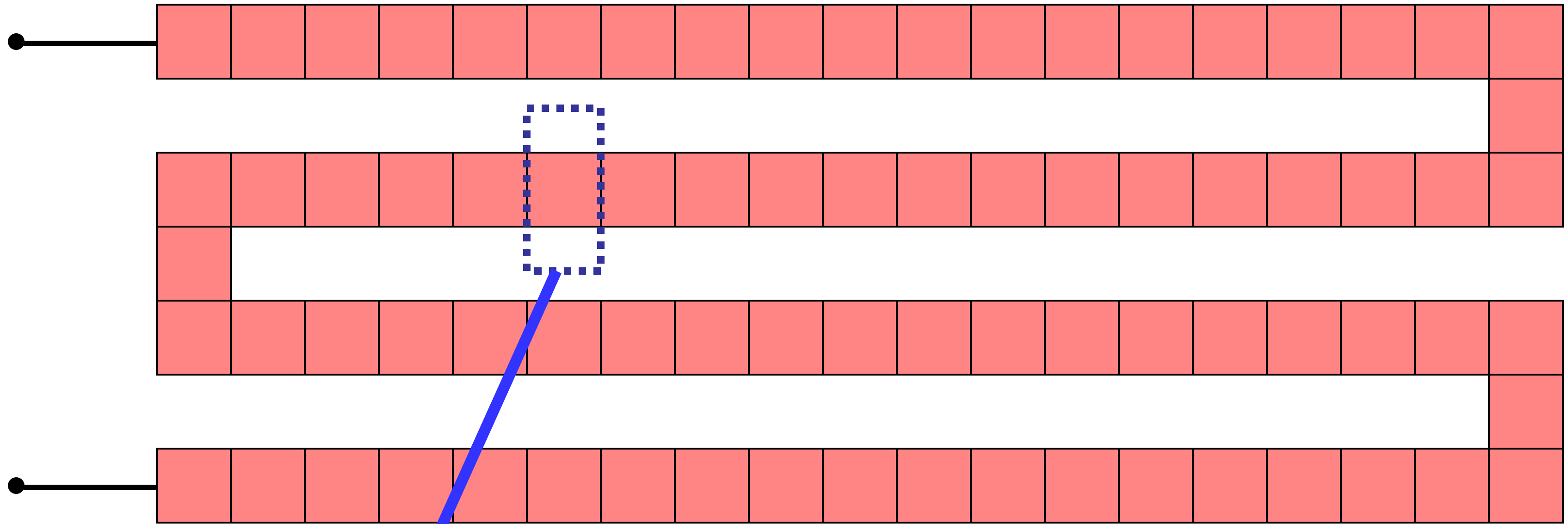
$$R_{AB} = R\ N_S = 40 \times 22.1 = 884\Omega$$

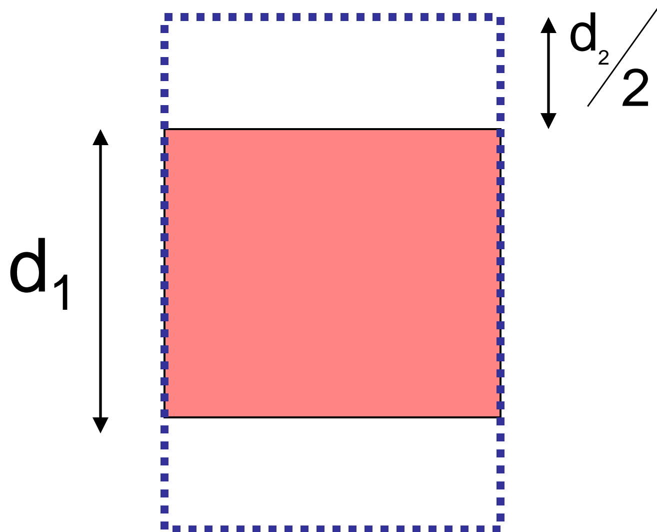
Resistance in Interconnects
(can be used to build resistors!)



- Serpentine often used when large resistance required
- Polysilicon or diffusion often used for resistor creation
- Effective at managing the aspect ratio of large resistors
- May include hundreds or even thousands of squares

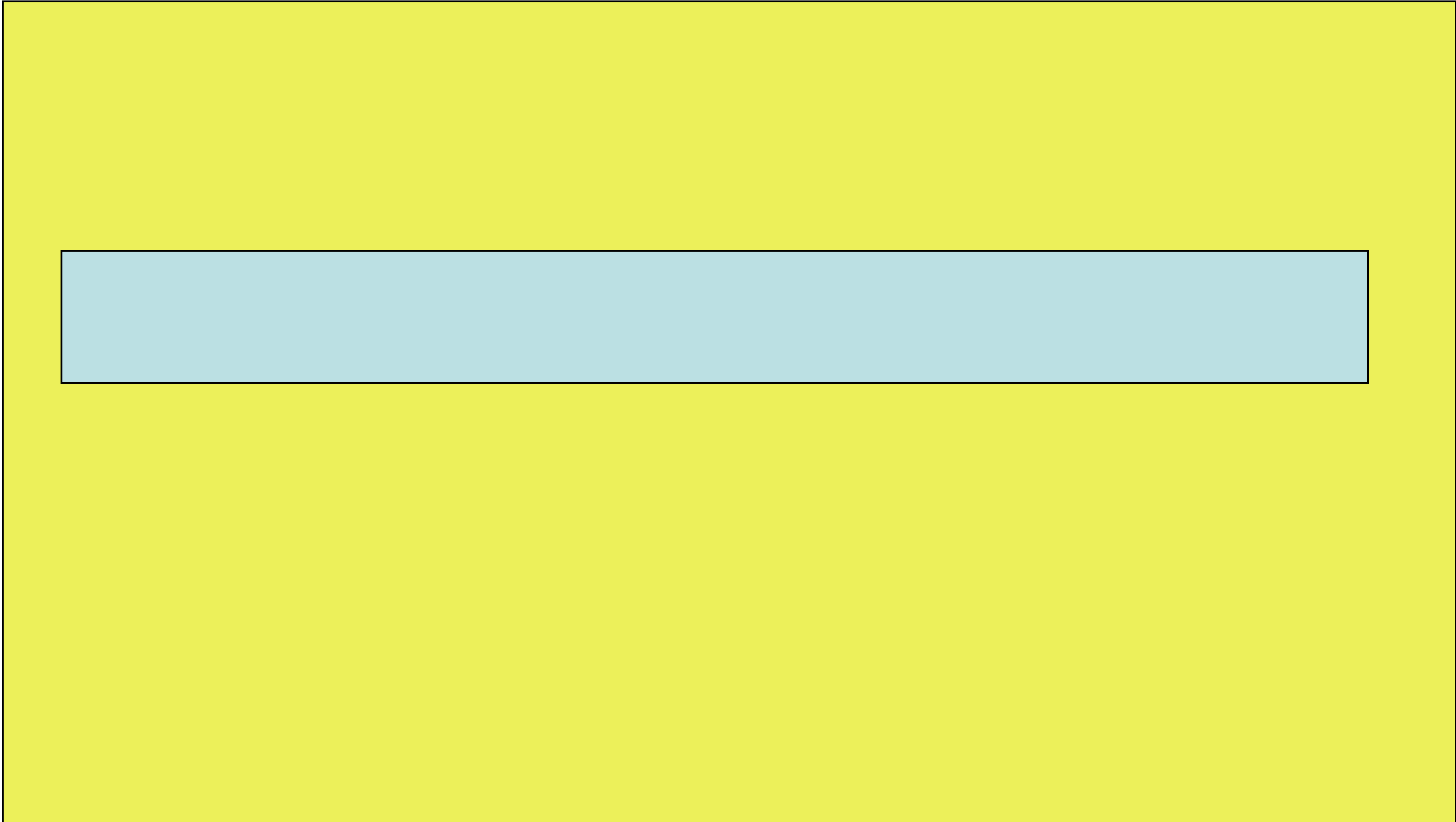
Resistance in Interconnects
(can be used to build resistors!)





Area requirements determined by both minimum width and minimum spacing design rules

Capacitance in Interconnects



$$C = C_D A$$

C_D is the capacitance density and A is the area of the overlap

Capacitance in Interconnects

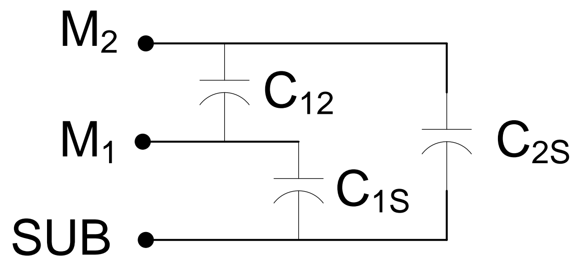
Metal 2

A_3

Metal 1 A_1 A_5 A_2

A_4

Substrate



Equivalent Circuit

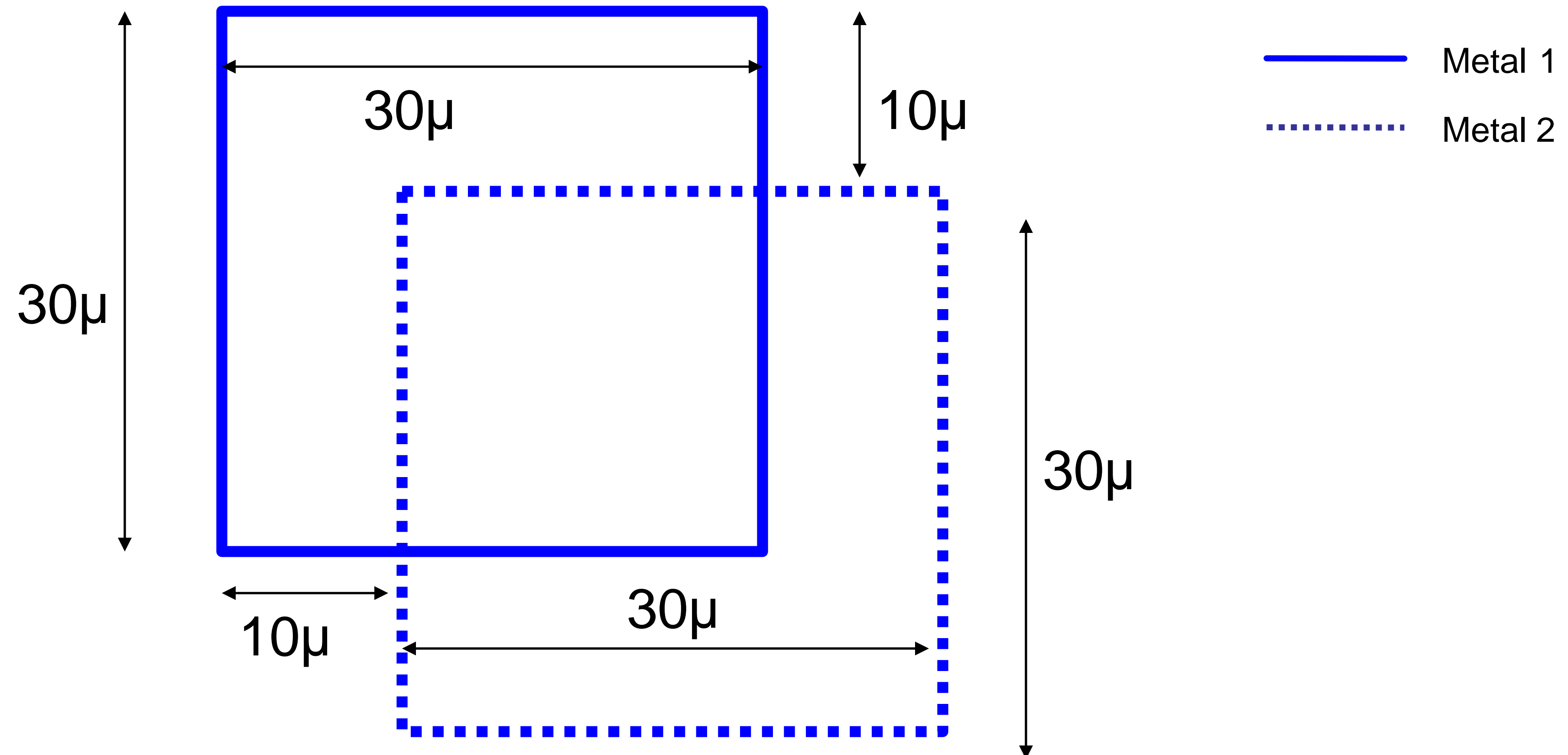
$$C_{12} = CD_{12}\, A_5$$

$$C_{1S} = CD_{1S}\, (A_1 + A_2 + A_5)$$

$$C_{2S} = CD_{2S}\, (A_3 + A_4)$$

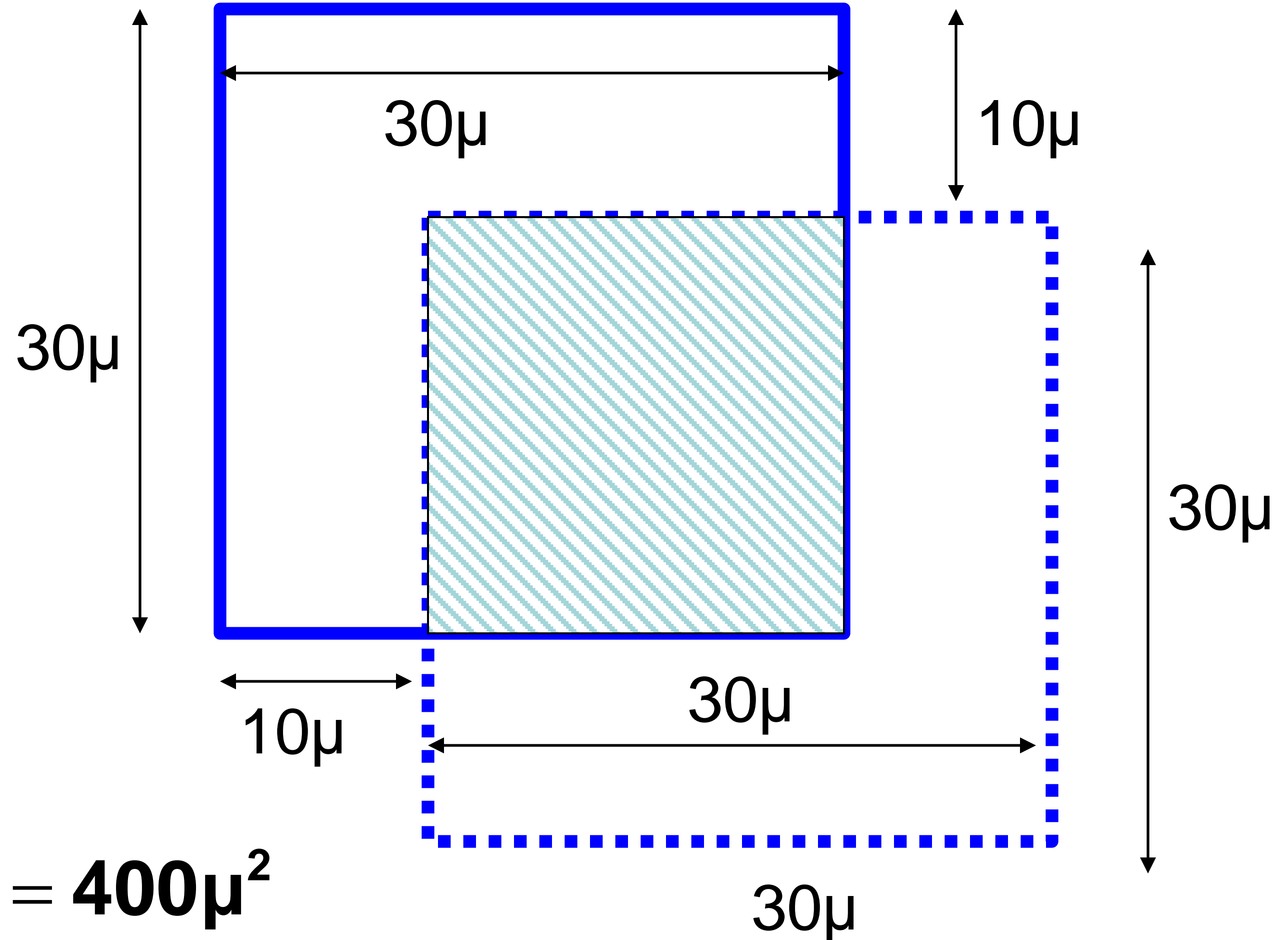
Example

Two metal layers, Metal 1 and Metal 2, are shown. Both are above field oxide. Determine the capacitance between Metal 1 and Metal 2. Assume the process has capacitance densities from M_1 to substrate of $.05fF/u^2$, from M_1 to M_2 of $.07fF/u^2$ and from M_2 to substrate of $.025fF/u^2$.



Example

Solution



$$A_{C1C2} = (20\mu)^2 = 400\mu^2$$

The capacitance density from M_1 to M_2 is .07fF/u^2

$$C_{12} = A_{C1C2} \bullet C_{D12} = 400\mu^2 \bullet 0.07\text{fF}/\mu^2 = 28\text{fF}$$

Capacitance and Resistance in Interconnects

- See MOSIS WEB site for process parameters that characterize parasitic resistances and capacitances

www.mosis.org

MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU — VENDOR: AMIS

TECHNOLOGY: SCN05 — FEATURE SIZE: 0.5 microns

Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

TRANSISTOR PARAMETERS	W/L	N-CHANNEL	P-CHANNEL	UNITS
MINIMUM	3.0/0.6			
Vth		0.79	-0.92	volts
SHORT	20.0/0.6			
Idss		446	-239	uA/um
Vth		0.68	-0.90	volts
Vpt		10.0	-10.0	volts
WIDE	20.0/0.6			
Ids0		< 2.5	< 2.5	pA/um
LARGE	50/50			
Vth		0.68	-0.95	volts
Vjbkd		10.9	-11.6	volts
Ijlk		<50.0	<50.0	pA
Gamma		0.48	0.58	V^0.5
K' (Uo*Cox/2)		56.4	-18.2	uA/V^2
Low-field Mobility		463.87	149.69	cm^2/V*s

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

Design Technology	XL (um)	XW (um)

SCMOS_SUBM (lambda=0.30)	0.10	0.00
SCMOS (lambda=0.35)	0.00	0.20

FOX TRANSISTORS	GATE	N+ACTIVE	P+ACTIVE	UNITS
Vth	Poly	>15.0	<-15.0	volts

PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.5	105.3	23.5	999	44.2	0.09	0.10	ohms/sq
Contact Resistance	64.9	149.7	17.3		29.2		0.97	ohms
Gate Oxide Thickness	142							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	824	816	ohms/sq
Contact Resistance	0.79			ohms

COMMENTS: N\POLY is N-well under polysilicon.

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	425	731	84		27	12	7	37	aF/um^2
Area (N+active)			2434		35	16	11		aF/um^2
Area (P+active)			2335						aF/um^2
Area (poly)				938	56	15	9		aF/um^2
Area (poly2)					49				aF/um^2
Area (metal1)						31	13		aF/um^2
Area (metal2)							35		aF/um^2
Fringe (substrate)	344	238			49	33	23		aF/um
Fringe (poly)					59	38	28		aF/um
Fringe (metal1)						51	34		aF/um
Fringe (metal2)							52		aF/um
Overlap (N+active)			232						aF/um
Overlap (P+active)			312						aF/um

CIRCUIT PARAMETERS			UNITS
Inverters	K		
Vinv	1.0	2.02	volts
Vinv	1.5	2.28	volts
Vol (100 uA)	2.0	0.13	volts

```
  Voh (100 uA)                2.0       4.85  volts
  Vinv                        2.0       2.46  volts
  Gain                        2.0     -19.72
 Ring Oscillator Freq.
  DIV256 (31-stg,5.0V)                 95.31  MHz
  D256_WIDE (31-stg,5.0V)             147.94  MHz
 Ring Oscillator Power
  DIV256 (31-stg,5.0V)                  0.49  uW/MHz/gate
  D256_WIDE (31-stg,5.0V)               1.01  uW/MHz/gate

COMMENTS: SUBMICRON
```

□ T6AU SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

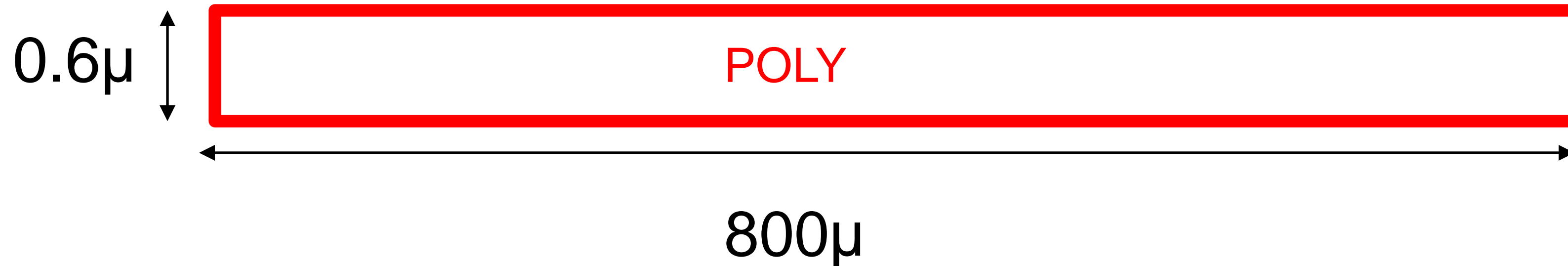
```
* DATE: Jan 11/07
* LOT: T6AU                  WAF: 7101
* Temperature_parameters=Default
.MODEL CMOSN NMOS (                                LEVEL   = 49
+VERSION = 3.1            TNOM    = 27             TOX     = 1.42E-8
+XJ      = 1.5E-7         NCH     = 1.7E17         VTH0    = 0.629035
+K1      = 0.8976376      K2      = -0.09255       K3      = 24.0984767
+K3B     = -8.2369696     W0      = 1.041146E-8    NLX     = 1E-9
+DVT0W   = 0              DVT1W   = 0              DVT2W   = 0
+DVT0    = 2.7123969      DVT1    = 0.4232931      DVT2    = -0.1403765
+U0      = 451.2322004    UA      = 3.091785E-13   UB      = 1.702517E-18
+UC      = 1.22401E-11    VSAT    = 1.715884E5     A0      = 0.6580918
+AGS     = 0.130484       B0      = 2.446405E-6    B1      = 5E-6
+KETA    = -3.043349E-3   A1      = 8.18159E-7     A2      = 0.3363058
+RDSW    = 1.367055E3     PRWG    = 0.0328586      PRWB    = 0.0104806
+WR      = 1              WINT    = 2.443677E-7    LINT    = 6.999776E-8
+XL      = 1E-7           XW      = 0              DWG     = -1.256454E-8
+DWB     = 3.676235E-8    VOFF    = -1.493503E-4   NFACTOR = 1.0354201
+CIT     = 0              CDSC    = 2.4E-4         CDSCD   = 0
+CDSCB   = 0              ETA0    = 2.342963E-3    ETAB    = -1.5324E-4
+DSUB    = 0.0764123      PCLM    = 2.5941582      PDIBLC1 = 0.8187825
+PDIBLC2 = 2.366707E-3    PDIBLCB = -0.0431505     DROUT   = 0.9919348
+PSCBE1  = 6.611774E8     PSCBE2  = 3.238266E-4    PVAG    = 0
+DELTA   = 0.01           RSH     = 83.5           MOBMOD  = 1
```

```
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO    = 2.32E-10      CGSO    = 2.32E-10      CGBO    = 1E-9
+CJ      = 4.282017E-4   PB      = 0.9317787     MJ      = 0.4495867
+CJSW    = 3.034055E-10  PBSW    = 0.8           MJSW    = 0.1713852
+CJSWG   = 1.64E-10      PBSWG   = 0.8           MJSWG   = 0.1713852
+CF      = 0             PVTH0   = 0.0520855     PRDSW   = 112.8875816
+PK2     = -0.0289036    WKETA   = -0.0237483    LKETA   = 1.728324E-3    )
*
.MODEL CMOSP PMOS (                              LEVEL   = 49
+VERSION = 3.1           TNOM    = 27            TOX     = 1.42E-8
+XJ      = 1.5E-7        NCH     = 1.7E17        VTH0    = -0.9232867
+K1      = 0.5464347     K2      = 8.119291E-3   K3      = 5.1623206
+K3B     = -0.8373484    W0      = 1.30945E-8    NLX     = 5.772187E-8
+DVT0W   = 0             DVT1W   = 0             DVT2W   = 0
+DVT0    = 2.0973823     DVT1    = 0.5356454     DVT2    = -0.1185455
+U0      = 220.5922586   UA      = 3.144939E-9   UB      = 1E-21
+UC      = -6.19354E-11  VSAT    = 1.176415E5    A0      = 0.8441929
+AGS     = 0.1447245     B0      = 1.149181E-6   B1      = 5E-6
+KETA    = -1.093365E-3  A1      = 3.467482E-4   A2      = 0.4667486
+RDSW    = 3E3           PRWG    = -0.0418549    PRWB    = -0.0212201
+WR      = 1             WINT    = 3.007497E-7   LINT    = 1.040439E-7
+XL      = 1E-7          XW      = 0             DWG     = -2.133809E-8
+DWB     = 1.706031E-8   VOFF    = -0.0801591    NFACTOR = 0.9468597
+CIT     = 0             CDSC    = 2.4E-4        CDSCD   = 0
+CDSCB   = 0             ETA0    = 0.4060383     ETAB    = -0.0633609
+DSUB    = 1             PCLM    = 2.2703293     PDIBLC1 = 0.0279014
+PDIBLC2 = 3.201161E-3   PDIBLCB = -0.057478     DROUT   = 0.1718548
+PSCBE1  = 4.876974E9    PSCBE2  = 5E-10         PVAG    = 0
+DELTA   = 0.01          RSH     = 105.3         MOBMOD  = 1
+PRT     = 0             UTE     = -1.5          KT1     = -0.11
+KT1L    = 0             KT2     = 0.022         UA1     = 4.31E-9
+UB1     = -7.61E-18     UC1     = -5.6E-11      AT      = 3.3E4
+WL      = 0             WLN     = 1             WW      = 0
+WWN     = 1             WWL     = 0             LL      = 0
+LLN     = 1             LW      = 0             LWN     = 1
+LWL     = 0             CAPMOD  = 2             XPART   = 0.5
+CGDO    = 3.12E-10      CGSO    = 3.12E-10      CGBO    = 1E-9
```

```
+CJ       = 7.254264E-4    PB       = 0.9682229      MJ       = 0.4969013
+CJSW     = 2.496599E-10   PBSW     = 0.99           MJSW     = 0.386204
+CJSWG    = 6.4E-11        PBSWG    = 0.99           MJSWG    = 0.386204
+CF       = 0              PVTH0    = 5.98016E-3     PRDSW    = 14.8598424
+PK2      = 3.73981E-3     WKETA    = 7.286716E-4    LKETA    = -4.768569E-3    )
*
```

Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6u wide and 800u long and compare that with the same interconnect if M_1 were used.



$$n_{SQ} = \frac{800\mu}{0.6\mu} = 1333$$

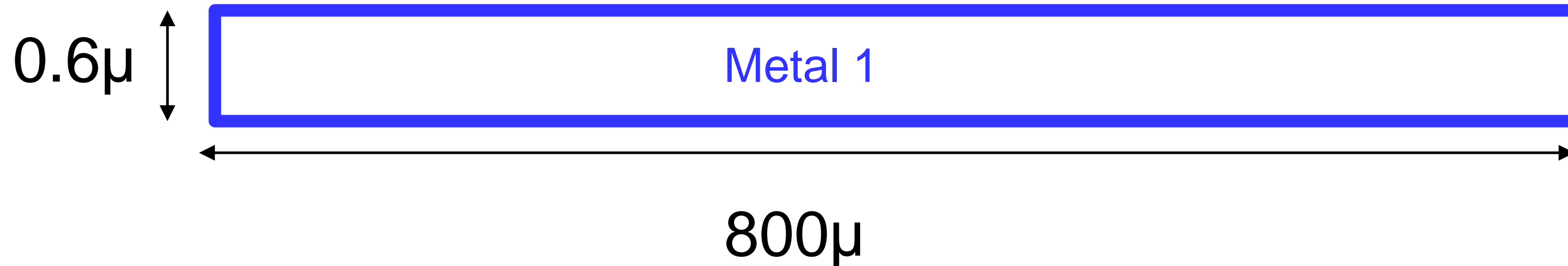
$$A = (0.6\mu)(800\mu) = 480\mu^2$$

$$R_{POLY} = n_{SQ} R_{SH} = 23.5 \bullet 1333 = 31.3K\Omega$$

$$C_{P\text{-}SUB} = A \bullet C_{DPS} = 480\mu^2 \bullet 85aF\mu^{-2} = 40.8fF$$

Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6u wide and 800u long and compare that with the same interconnect if M_1 were used.



$$n_{SQ} = \frac{800\mu}{0.6\mu} = 1333 \qquad A = (0.6\mu)(800\mu) = 480\mu^2$$

$$R_{M1} = n_{SQ} R_{SH} = 0.09 \bullet 1333 = 120\,\Omega$$

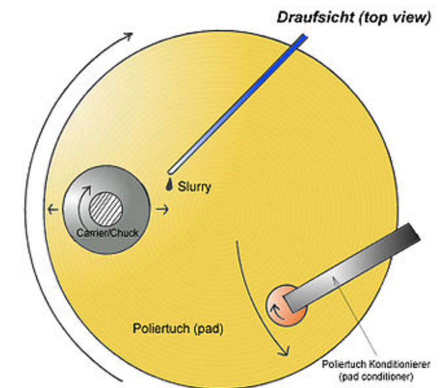
$$C_{M1\text{-}SUB} = A \bullet C_{DM1S} = 480\mu^2 \bullet 27\,aF\mu^{-2} = 13.0\,fF$$

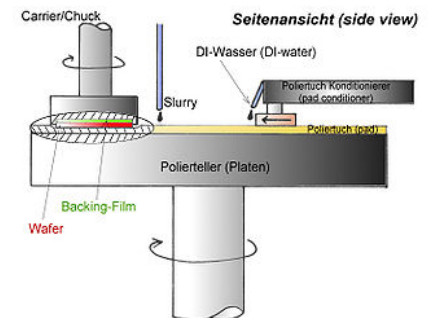
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Ion Implantation
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization

Planarization

- Planarization used to keep surface planar during subsequent processing steps
  - Important for creating good quality layers in subsequent processing steps
  - Mechanically planarized

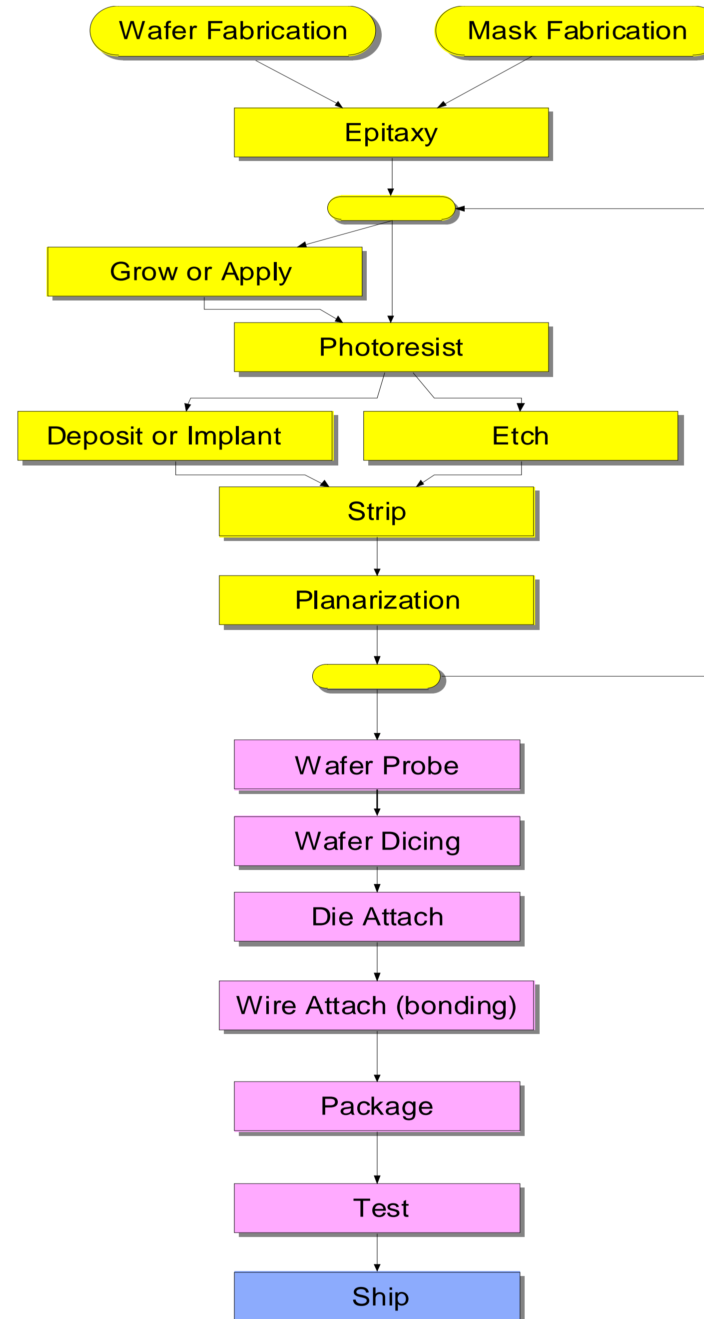




Generic Process Flow

Front End

Back End



Front End Process Integration for Fabrication of ICs

Wafer Fabrication

Mask Fabrication

Epitaxy

Photoresist

Deposit or Implant

Etch

Strip

Planarize

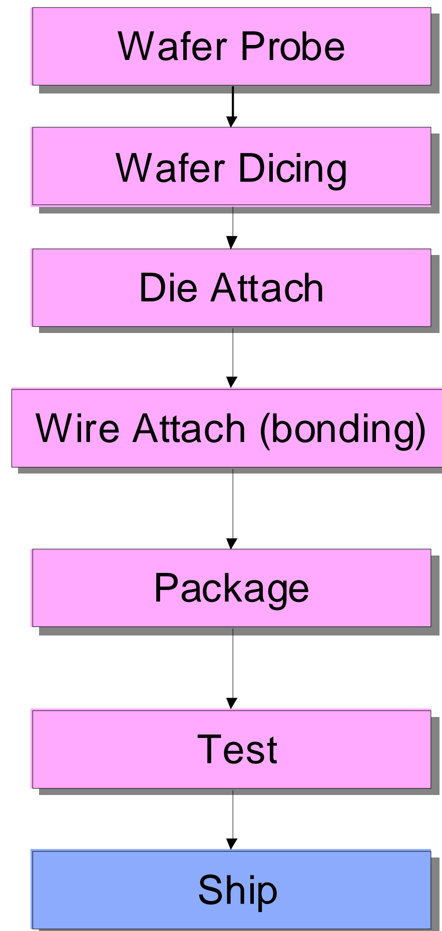
Back End Processing

Once for each mask

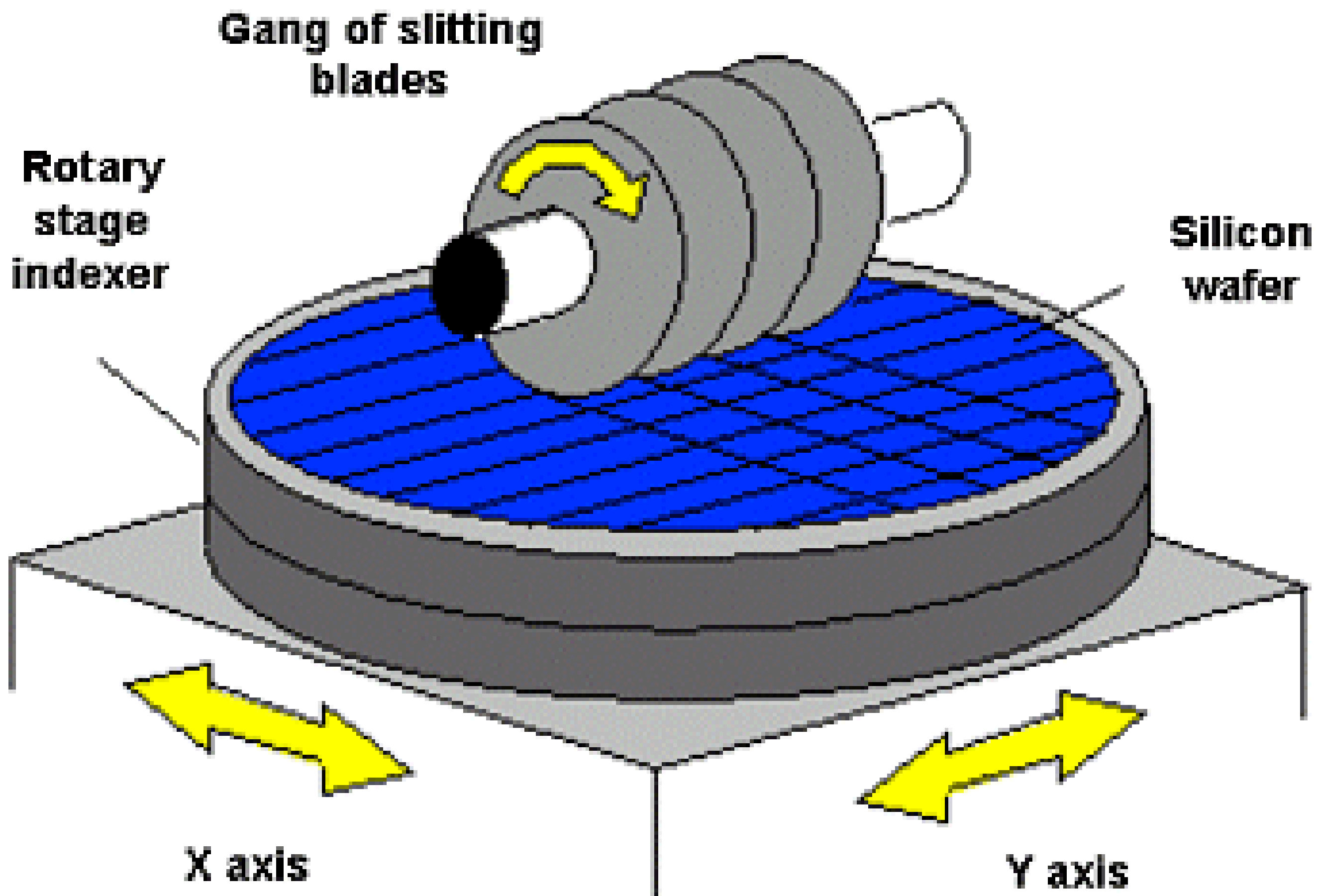
Front-End Process Flow

- Front-end processing steps analogous to a "recipe" for manufacturing an integrated circuit
- Recipes vary from one process to the next but the same basic steps are used throughout the industry
- Details of the recipe are generally considered proprietary

Back-End Process Flow



Wafer Dicing



www.renishaw.com

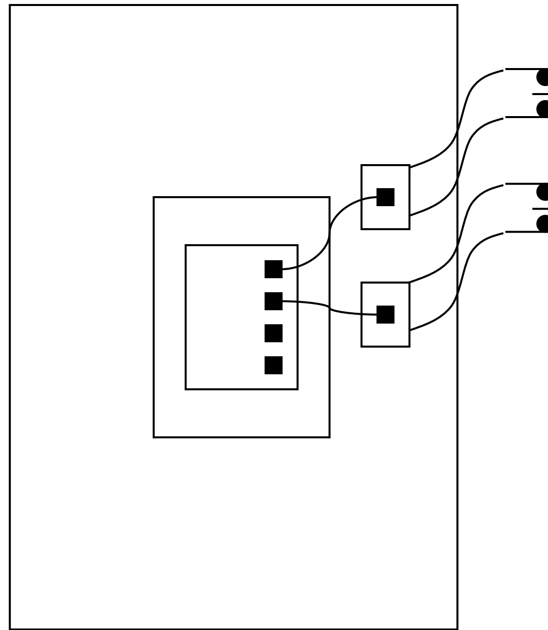
Die Attach

1. Eutectic
2. Pre-form
3. Conductive Epoxy

Electrical Connections (Bonding)

- Wire Bonding
- Bump Bonding

Wire Bonding



Wire – gold or aluminum
25 μ in diameter

Wire Bonding

Excellent Annimation showing process at :

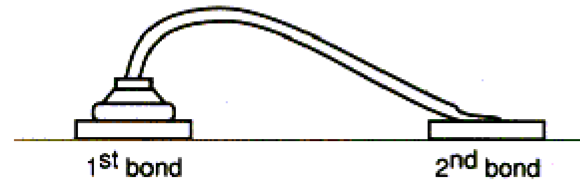
http://www.kns.com/_Flash/CAP_BONDING_CYCLE.swf

Wire Bonding

Ball Bond

Wedge Bond

Ball Bonding Steps



Force

Ultrasonic Vibration

Heat

Force

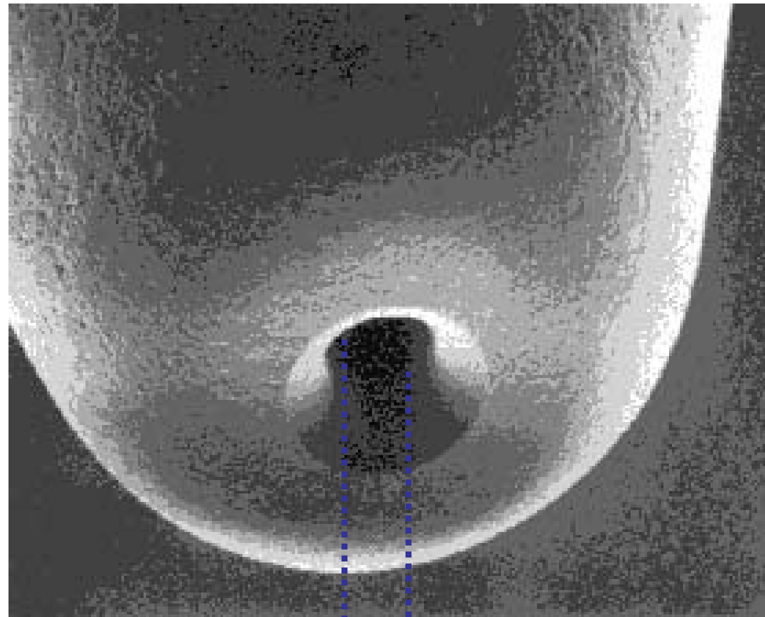
Ultrasonic Vibration

Heat

Clamping the wire

www.kns.com

Ball Bonding Tip

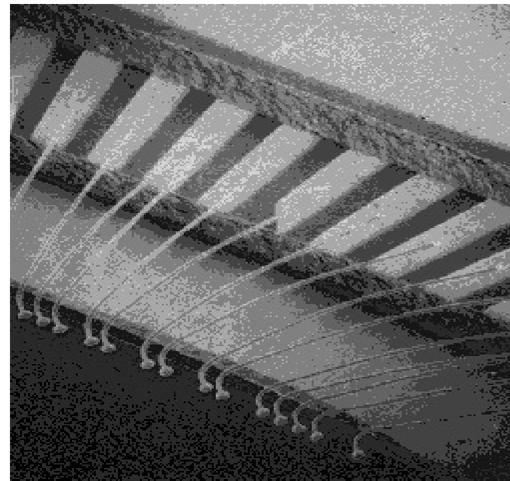


Approx 25µ

Wire Bonding

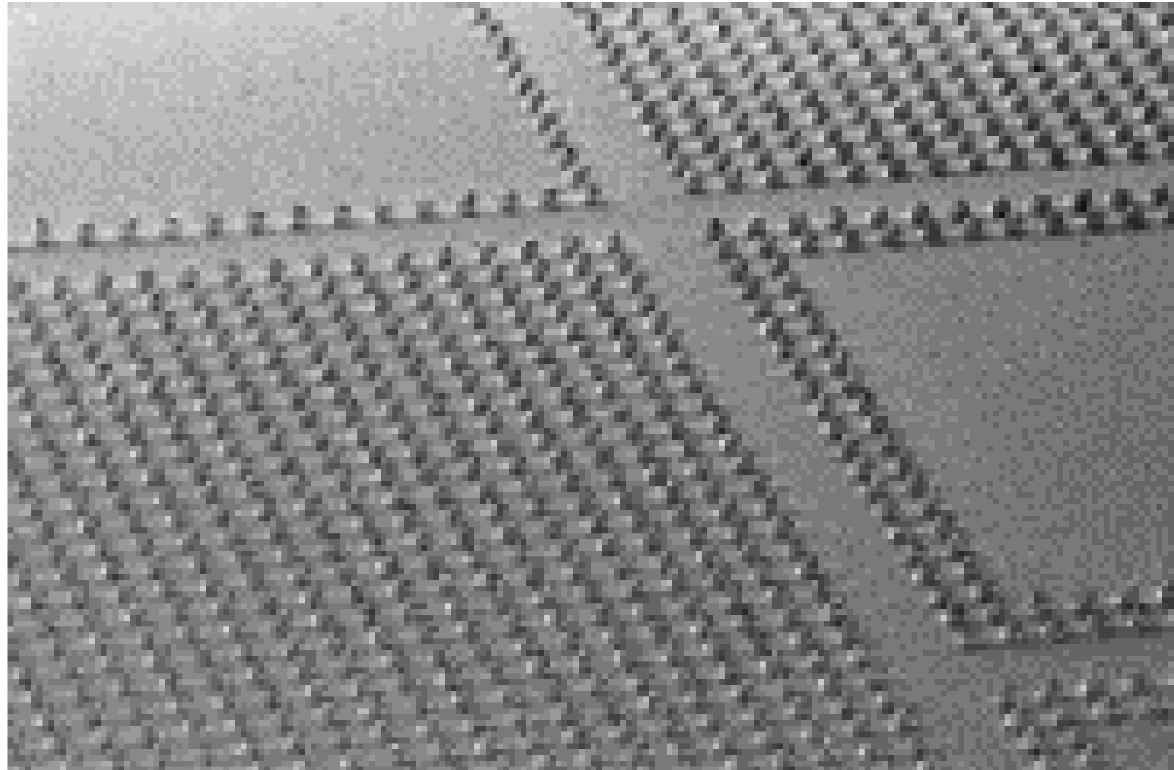
Ball Bond

Termination Bond



Ball Bond Photograph

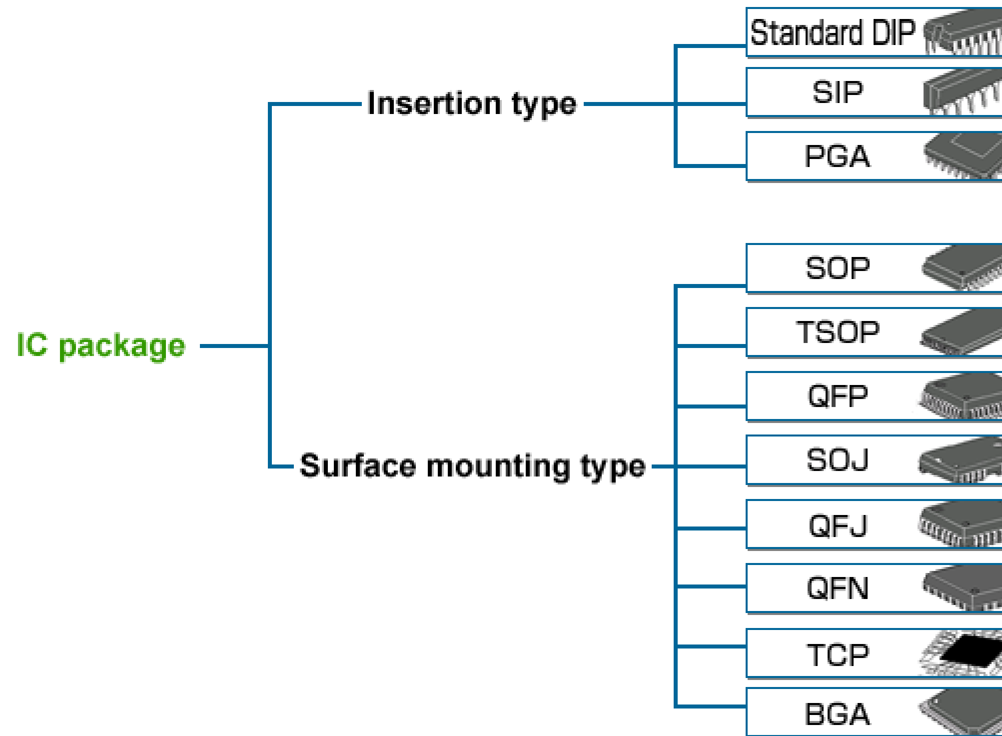
Bump Bonding



Packaging

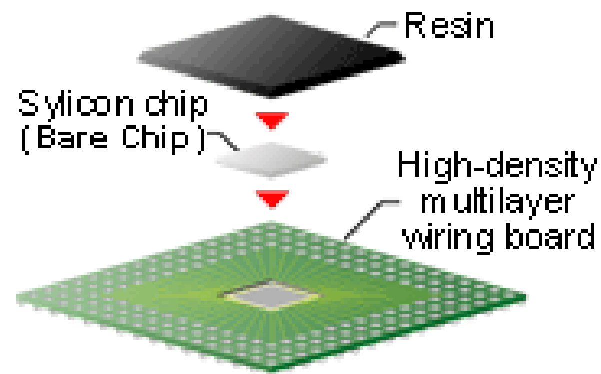
1. Many variants in packages now available
2. Considerable development ongoing on developing packaging technology
3. Cost can vary from few cents to tens of dollars
4. Must minimize product loss after packaged
5. Choice of package for a product is serious business
6. Designer invariably needs to know packaging plans and package models

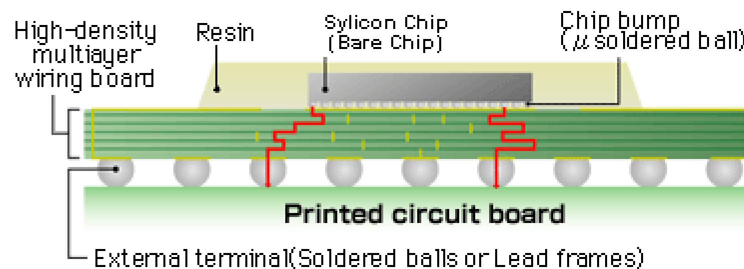
Packaging



www.necel.com

Packaging



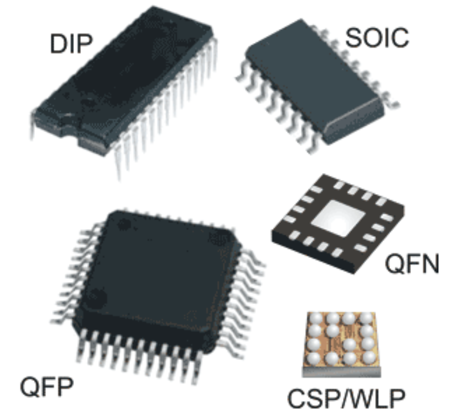


www.necel.com

Pin Pitch Varies with Package Technology

All measurements are nominal in [mm].

Name	Pin pitch	Size	Height
DIP or DIL	2.54		
SOIC-16	1.27	3.9 x 10	1.72
SSOP	0.635		
TSSOP54-II	0.8	12.7 x 22.22	~1
PLCC44	1.27		
PQ208[1]	0.50	28 x 28	3.4
TQFP64	0.40	7 x 7	1.0
TQFP144[2]	0.50	20 x 20	1.0
128PQFP	0.50	23.23 x 14.0	3.15



http://www.electroiq.com/index/display/packaging-article-display/234467/articles/advanced-packaging/volume-14/issue-8/features/the-back-end-process/materials-and-methods-for-ic-package-assemblies.htm

From Wikipedia, Sept 20, 2010

http://en.wikipedia.org/wiki/List_of_chip_carriers

Many standard packages available today:

http://www.interfacebus.com/Design_Pack_types.html

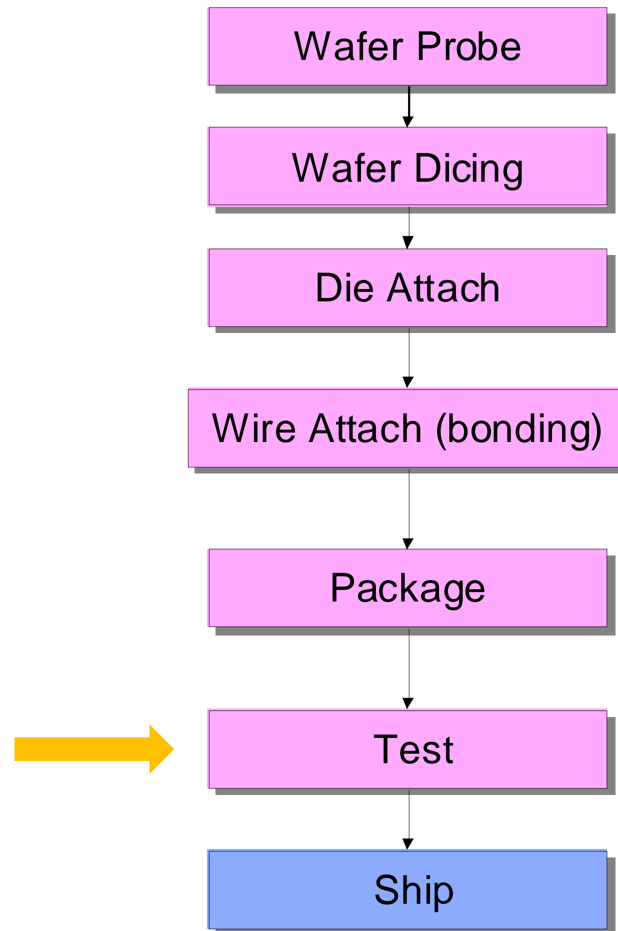
BCC: Bump Chip Carrier
BGA: Ball Grid Array; BGA graphic
BQFP: Bumpered Quad Flat Pack
CABGA/SSBGA: Chip Array/Small Scale Ball Grid Array
CBGA: Ceramic Ball Grid Array
CFP: Ceramic Flat Pack
CPGA: Ceramic Pin Grid Array, **CPGA Graphic**
CQFP: Ceramic Quad Flat Pack, **CQFP Graphic**
TBD: Ceramic Lead-Less Chip Carrier
DFN: Dual Flat Pack, No Lead
DLCC: Dual Lead-Less Chip Carrier (Ceramic)
ETQFP: Extra Thin Quad Flat Package
FBGA: Fine-pitch Ball Grid Array
fpBGA: Fine Pitch Ball Grid Array
HSBGA: Heat Slug Ball Grid Array
JLCC: J-Leaded Chip Carrier (Ceramic) **J-Lead Picture**
LBGA: Low-Profile Ball Grid Array
LCC: Leaded Chip Carrier **LCC Graphic**
LCC: Leaded Chip Carrier **Un-formed LCC Graphic**
LCCC: Leaded Ceramic Chip Carrier;
LFBGA: Low-Profile, Fine-Pitch Ball Grid Array
LGA: Land Grid Array, **LGA uP** [Pins are on the Motherboard, not the socket]
LLCC: Leadless Leaded Chip Carrier **LLCC Graphic**
LQFP: Low Profile Quad Flat Package
MCMBGA: Multi Chip Module Ball Grid Array
MCMCABGA: Multi Chip Module-Chip Array Ball Grid Array
MLCC: Micro Lead-frame Chip Carrier

PBGA: Plastic Ball Grid Array
PLCC: Plastic Leaded Chip Carrier
PQFD: Plastic Quad Flat Pack
PQFP: Plastic Quad Flat Pack
PSOP: Plastic Small-Outline Package PSOP graphic
QFP: Quad Flatpack **QFP Graphics**
QSOP: Quarter Size Outline Package [Quarter Pitch Small Outline Package]
SBGA: Super BGA - above 500 Pin count
SOIC: Small Outline IC
SO Flat Pack: Small Outline Flat Pack IC
SOJ: Small-Outline Package [J-Lead]; **J-Lead Picture**
SOP: Small-Outline Package; SOP IC, Socket
SSOP: Shrink Small-Outline Package
TBGA: Thin Ball Grid Array
TQFP: Thin Quad Flat Pack TQFP Graphic
TSOP: Thin Small-Outline Package
TSSOP: Thin Shrink Small-Outline Package
TVSOP: Thin Very Small-Outline Package
VQFB: Very-thin Quad Flat Pack

Considerable activity today and for years to come on improving packaging technology

- Multiple die in a package
- Three-dimensional chip stacking
- Multiple levels of interconnect in stacks
- Through silicon via technology
- Power and heat management
- Cost driven and cost constrained

Back-End Process Flow



Testing of Integrated Circuits

Most integrated circuits are tested twice

- Wafer Probe Testing
  - Quick test for functionality
  - Usually does not include much parametric testing
  - Relatively fast and low cost test
  - Package costs often quite large
  - Critical to avoid packaging defective parts
- Packaged Part Testing
  - Testing costs for packaged parts can be high
  - Extensive parametric tests done at package level for many parts
  - Data sheet parametrics with Max and Min values are usually tested on all Ics
  - Data sheet parametrics with Typ values are seldom tested
  - Occasionally require testing at two or more temperatures but this is costly
  - Critical to avoid packaging defective parts

End of Lecture 10