IC Fabrication Technology
Part IV
- Back-end Processes
Devices in Semiconductor Processes
Quiz 10

What is the major reason contacts of metal to poly are not allowed in the gate region of a transistor?
And the number is ....
And the number is ....
Quiz 10

What is the major reason contacts of metal to poly are not allowed in the gate region of a transistor?

Solution: Pin-holes will degrade yield
• Contacts usually of a fixed size
  – All etches reach bottom at about the same time
  – Multiple contacts widely used
  – Contacts not allowed to Poly on thin oxide in most processes
  – Dog-bone often needed for minimum-length devices
Metalization

- Aluminum widely used for interconnect
- Copper finding some applications
- Must not exceed maximum current density – around 1ma/u
- Ohmic Drop must be managed
- Parasitic Capacitances must be managed
- Interconnects from high to low level metals require connections to each level of metal
- Stacked vias permissible in some processes
Interconnect Layers May Vary in Thickness or Be Mostly Uniform

**FIG 4.30** Interconnect geometry

<table>
<thead>
<tr>
<th>Layer</th>
<th>$t$ (nm)</th>
<th>$w$ (nm)</th>
<th>$s$ (nm)</th>
<th>AR</th>
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<tbody>
<tr>
<td>6</td>
<td>1720</td>
<td>860</td>
<td>860</td>
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<td></td>
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<td>5</td>
<td>1600</td>
<td>800</td>
<td>800</td>
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<td>1000</td>
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<tr>
<td>4</td>
<td>1080</td>
<td>540</td>
<td>540</td>
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<tr>
<td></td>
<td>700</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>700</td>
<td>320</td>
<td>320</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>700</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>700</td>
<td>320</td>
<td>320</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>700</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>1</td>
<td>480</td>
<td>250</td>
<td>250</td>
<td>1.9</td>
</tr>
<tr>
<td></td>
<td>800</td>
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**FIG 4.31** Layer stack for 6-metal Intel 180 nm process

12.5μ
Interconnects

- Metal is preferred interconnect
  - Because conductivity is high
- Parasitic capacitances and resistances of concern in all interconnects
- Polysilicon used for short interconnects
  - Silicided to reduce resistance
  - Unsilicided when used as resistors
- Diffusion used for short interconnects
  - Parasitic capacitances are high
Interconnects

• Metal is preferred interconnect
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• Parasitic capacitances and resistances of concern in all interconnects
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The “Number of Squares” approach to resistance determination in thin films

\[ N_S = 21 \]

\[ L / W = 21 \]

\[ R = R \ N_S \]
Review from Last Time

Capacitance in Interconnects

\[ C = C_D A \]

\( C_D \) is the capacitance density and \( A \) is the area of the overlap
Consider Resistance and Capacitance Parameters

Review from Last Time

**PROCESS PARAMETERS**

<table>
<thead>
<tr>
<th></th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>PLY2 HR</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>Sheet Resistance</td>
<td>83.5</td>
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<td>23.5</td>
<td>999</td>
<td>44.2</td>
<td>0.09</td>
<td>0.10</td>
<td>ohms/sq</td>
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<td>64.9</td>
<td>149.7</td>
<td>17.3</td>
<td></td>
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<td>0.97</td>
<td>ohms</td>
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<tr>
<td>Gate Oxide Thickness</td>
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<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>angstrom</td>
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**PROCESS PARAMETERS**

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<th>N_W</th>
<th>UNITS</th>
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<td>0.05</td>
<td>824</td>
<td>816</td>
<td>ohms/sq</td>
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<tr>
<td>Contact Resistance</td>
<td>0.79</td>
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<td>ohms</td>
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**COMMENTS**: N\POLY is N-well under polysilicon.

**CAPACITANCE PARAMETERS**

<table>
<thead>
<tr>
<th></th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>N_W</th>
<th>UNITS</th>
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<tr>
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<td>731</td>
<td>84</td>
<td>27</td>
<td>12</td>
<td>7</td>
<td>37</td>
<td>aF/um^2</td>
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<td>Area (N+active)</td>
<td>2434</td>
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<td>35</td>
<td>16</td>
<td>11</td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (P+active)</td>
<td>2335</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
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<tr>
<td>Area (poly)</td>
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<td>938</td>
<td>56</td>
<td>15</td>
<td>9</td>
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<td>aF/um^2</td>
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<td>aF/um^2</td>
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<tr>
<td>Area (metal1)</td>
<td></td>
<td></td>
<td>31</td>
<td>13</td>
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<td></td>
<td>aF/um^2</td>
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<tr>
<td>Area (metal2)</td>
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<td>aF/um^2</td>
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<td>Fringe (substrate)</td>
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<td>238</td>
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<td>49</td>
<td>33</td>
<td>23</td>
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<td>aF/um</td>
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<tr>
<td>Fringe (poly)</td>
<td></td>
<td></td>
<td></td>
<td>59</td>
<td>38</td>
<td>28</td>
<td></td>
<td>aF/um</td>
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<tr>
<td>Fringe (metal1)</td>
<td></td>
<td></td>
<td></td>
<td>51</td>
<td>34</td>
<td></td>
<td></td>
<td>aF/um</td>
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<tr>
<td>Fringe (metal2)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>52</td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
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<tr>
<td>Overlap (N+active)</td>
<td></td>
<td></td>
<td></td>
<td>232</td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
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<tr>
<td>Overlap (P+active)</td>
<td></td>
<td></td>
<td></td>
<td>312</td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
</tbody>
</table>
IC Fabrication Technology

- Crystal Preparation
- Masking
- Photolithographic Process
- Deposition
- Etching
- Diffusion
- Ion Implantation
- Oxidation
- Epitaxy
- Polysilicon
- Contacts, Interconnect and Metalization
- Planarization
Planarization

- Planarization used to keep surface planar during subsequent processing steps
  - Important for creating good quality layers in subsequent processing steps
  - Mechanically planarized
Generic Process Flow
Front End Process Integration for Fabrication of ICs

- Wafer Fabrication
- Mask Fabrication
- Epitaxy
- Photoresist
- Deposit or Implant
- Etch
- Strip
- Planarize

Back End Processing

Once for each mask
Front-End Process Flow

- Front-end processing steps analogous to a “recipe” for manufacturing an integrated circuit
- Recipes vary from one process to the next but the same basic steps are used throughout the industry
- Details of the recipe are generally considered proprietary
Back-End Process Flow

1. Wafer Probe
2. Wafer Dicing
3. Die Attach
4. Wire Attach (bonding)
5. Package
6. Test
7. Ship
Wafer Dicing
Die Attach

1. Eutectic
2. Pre-form
3. Conductive Epoxy
Electrical Connections (Bonding)

- Wire Bonding
- Bump Bonding
Wire Bonding

Wire – gold or aluminum
25 μ in diameter
Wire Bonding

Excellent Animation showing process at:

http://www.kns.com/_Flash/CAP_BONDING_CYCLE.swf
Wire Bonding

Ball Bond

Wedge Bond
Ball Bonding Steps
Ball Bonding Tip

Approx 25µ
Wire Bonding

Ball Bond

Termination Bond

Ball Bond Photograph
Bump Bonding
End of Lecture 11