EE 330 Fall 2016 Seating

1. Brandon Baxter
   Zachary Bennett
   Steven Warren
   
2. Xiang Li
   Yi Qiu
   Benjamin Gisler
   David Clark

3. Benjamin Engebrect
   Brian Weber
   Austin Yurchik
   Sarah Sebastian

4. Steve Ukpan
   Jose Candelario
   Sarah Huber
   Dean Vanever

5. Shengxin Mao
   Yuxuan Yuan
   Li Qian
   Chenhang Xu
   
6. Christopher Little
   Robert Slezak
   
7. Liang Zhang
   
8. Jakub Hladik
   Timothy Lindquist
   Jacob Johnson
   William Henthorn
   Daniel Griffen

9. Benjamin Zickefoose
   Karla Beas
   Aurelien Chanel
   Travis Merrifield
   Joshua Pachl

10. Matthew Martinez
    Amna Aftab
    Matthew Rottinghaus
    Eric Middleton

11. Milan Patel
    Bailey Akers
    James Kluesner
    Alexander Christenson
    Nathaniel Summitt

12. Jiangning Xiong
    Sang Uk Park
    Jie-Hui Yan
    Abdulmagied Ibrahim
    Jinan Li

13. Apurba Kumar Das
    
14. Liang Zhang
    
15. Shengxin Mao
    
16. Christopher Little
    
17. Robert Slezak
    
18. Liang Zhang
    
19. Apurba Kumar Das
    
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60. Liang Zhang
EE 330
Lecture 11

Back-end Processes (wrap up)

Semiconductor Processes

Devices in Semiconductor Processes

- Resistors
- Diodes
Review from Last Lecture

Back-End Process Flow

- Wafer Probe
- Wafer Dicing
- Die Attach
- Wire Attach (bonding)
- Package
- Test
- Ship
Wafer Dicing

Review from Last Lecture
Die Attach

1. Eutectic
2. Pre-form
3. Conductive Epoxy
Electrical Connections (Bonding)

- Wire Bonding
- Bump Bonding
Packaging

1. Many variants in packages now available
2. Considerable development ongoing on developing packaging technology
3. Cost can vary from few cents to tens of dollars
4. Must minimize product loss after packaged
5. Choice of package for a product is serious business
6. Designer invariably needs to know packaging plans and package models
Packaging

- IC package
  - Insertion type
    - Standard DIP
      - SIP
      - PGA
  - Surface mounting type
    - SOP
    - TSOP
    - QFP
    - SOJ
    - QFJ
    - QFN
    - TCP
    - BGA

www.necel.com
Packaging

Resin

Silicon chip (Bare Chip)

High-density multilayer wiring board

Printed circuit board

External terminal (Soldered balls or Lead frames)

Chip bump (μ-soldered ball)

Resin

Silicon Chip (Bare Chip)

High-density multilayer wiring board
Pin Pitch Varies with Package Technology

All measurements are nominal in [mm].

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin pitch</th>
<th>Size</th>
<th>Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP or DIL</td>
<td>2.54</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SOIC-16</td>
<td>1.27</td>
<td>3.9 x 10</td>
<td>1.72</td>
</tr>
<tr>
<td>SSOP</td>
<td>0.635</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSSOP54-II</td>
<td>0.8</td>
<td>12.7 x 22.22</td>
<td>~1</td>
</tr>
<tr>
<td>PLCC44</td>
<td>1.27</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PQ208[1]</td>
<td>0.50</td>
<td>28 x 28</td>
<td>3.4</td>
</tr>
<tr>
<td>TQFP64</td>
<td>0.40</td>
<td>7 x 7</td>
<td>1.0</td>
</tr>
<tr>
<td>TQFP144[2]</td>
<td>0.50</td>
<td>20 x 20</td>
<td>1.0</td>
</tr>
<tr>
<td>128PQFP</td>
<td>0.50</td>
<td>23.23 x 14.0</td>
<td>3.15</td>
</tr>
</tbody>
</table>

Many standard packages available today:


BCC: Bump Chip Carrier
BGA: Ball Grid Array, BGA graphic
BQFP: Bumpered Quad Flat Pack
CABGA/SSBGA: Chip Array/Small Scale Ball Grid Array
CBGA: Ceramic Ball Grid Array
CFP: Ceramic Flat Pack
CPGA: Ceramic Pin Grid Array, CPGA Graphic
CQFP: Ceramic Quad Flat Pack, CQFP Graphic
TBD: Ceramic Lead-Less Chip Carrier
DFN: Dual Flat Pack, No Lead
DLCC: Dual Lead-Less Chip Carrier (Ceramic)
ETQFP: Extra Thin Quad Flat Package
FBGA: Fine-pitch Ball Grid Array
fPBG: Fine Pitch Ball Grid Array
HSBGA: Heat Slug Ball Grid Array
JLCC: J-Leaded Chip Carrier (Ceramic) J-Lead Picture
LBGA: Low-Profile Ball Grid Array
LCC: Leaded Chip Carrier LCC Graphic
LCC: Leadless Chip Carrier Un-formed LCC Graphic
LCCC: Leadless Ceramic Chip Carrier;
LFBGA: Low-Profile, Fine-Pitch Ball Grid Array
LGA: Land Grid Array, LGA up [Pins are on the Motherboard, not the socket]
LLCC: Leadless Leaded Chip Carrier LLCC Graphic
LQFP: Low Profile Quad Flat Package
MCMBGA: Multi Chip Module Ball Grid Array
MCMCABGA: Multi Chip Module-Chip Array Ball Grid Array
MLCC: Micro Lead-frame Chip Carrier
PBGA: Plastic Ball Grid Array
PLCC: Plastic Leaded Chip Carrier
PQFD: Plastic Quad Flat Pack
PQFP: Plastic Quad Flat Pack
PSOP: Plastic Small-Outline Package PSOP graphic
QFP: Quad Flatpack QFP Graphics
QSOP: Quarter Size Outline Package [Quarter Pitch Small Outline Package]
SBGA: Super BGA - above 500 Pin count
SOIC: Small Outline IC
SOF Flat Pack: Small Outline Flat Pack IC
S0J: Small-Outline Package [J-Lead], J-Lead Picture
SOP: Small-Outline Package; SOP IC, Socket
SSOP: Shrink Small-Outline Package
TBGA: Thin Ball Grid Array
TQFP: Thin Quad Flat Pack TQFP Graphic
TSOP: Thin Small-Outline Package
TSSOP: Thin Shrink Small-Outline Package
TVSOP: Thin Very Small-Outline Package
VQFB: Very-thin Quad Flat Pack
Considerable activity today and for years to come on improving packaging technology

- Multiple die in a package
- Three-dimensional chip stacking
- Multiple levels of interconnect in stacks
- Through silicon via technology
- Power and heat management
- Cost driven and cost constrained
The following few slides come from a John Lau presentation

TSV Interposer: The Most Cost-Effective Integrator for 3D IC Integration

John H. Lau
Electronics & Optoelectronics Research Laboratories
Industrial Technology Research Institute (ITRI)
Chutung, Hsinchu, Taiwan 310, R.O.C.
886-3591-3390, johnlau@itri.org.tw
2.5D IC Integration with Passive Interposer
TSV passive interposer supporting high-power chips (e.g., microprocessor and logic) on its top side and low-power chips (e.g., memory) on its bottom side.

Special underfills are needed between the Cu-filled interposer and all the chips. Ordinary underfills are needed between the interposer and the organic substrate.
Back-End Process Flow

1. Wafer Probe
2. Wafer Dicing
3. Die Attach
4. Wire Attach (bonding)
5. Package
6. Test
7. Ship
Testing of Integrated Circuits

Most integrated circuits are tested twice

- **Wafer Probe Testing**
  - Quick test for functionality
  - Usually does not include much parametric testing
  - Relatively fast and low cost test
  - Package costs often quite large
  - Critical to avoid packaging defective parts

- **Packaged Part Testing**
  - Testing costs for packaged parts can be high
  - Extensive parametric tests done at package level for many parts
  - Data sheet parametrics with Max and Min values are usually tested on all Ics
  - Data sheet parametrics with Typ values are seldom tested
  - Occasionally require testing at two or more temperatures but this is costly
  - Critical to avoid packaging defective parts
Basic Semiconductor Processes

MOS (Metal Oxide Semiconductor)

1. NMOS  n-ch
2. PMOS  p-ch
3. CMOS  n-ch & p-ch
   • Basic Device: MOSFET
   • Niche Device: MESFET
   • Other Devices: Diode
                 BJT
                 Resistors
                 Capacitors
                 Schottky Diode
Basic Semiconductor Processes

Bipolar

1. T²L
2. ECL
3. I²L
4. Linear ICs
   - Basic Device: BJT (Bipolar Junction Transistor)
   - Niche Devices: HBJT (Heterojunction Bipolar Transistor)
     HBT
   - Other Devices: Diode
     Resistor
     Capacitor
     Schottky Diode
     JFET (Junction Field Effect Transistor)
Basic Semiconductor Processes

Other Processes

• Thin and Thick Film Processes
  – Basic Device: Resistor
• BiMOS or BiCMOS
  – Combines both MOS & Bipolar Processes
  – Basic Devices: MOSFET & BJT
• SiGe
  – BJT with HBT implementation
• SiGe / MOS
  – Combines HBT & MOSFET technology
• SOI / SOS (Silicon on Insulator / Silicon on Sapphire)
• Twin-Well & Twin Tub CMOS
  – Very similar to basic CMOS but more optimal transistor char.
Devices in Semiconductor Processes

- **Standard CMOS Process**
  - MOS Transistors
    - n-channel
    - p-channel
  - Capacitors
  - Resistors
  - Diodes
  - BJT (decent in some processes)
    - npn
    - pnp
  - JFET (in some processes)
    - n-channel
    - p-channel

- **Standard Bipolar Process**
  - BJT
    - npn
    - pnp
  - JFET
    - n-channel
    - p-channel
  - Diodes
  - Resistors
  - Capacitors

- **Niche Devices**
  - Photodetectors (photodiodes, phototransistors, photoresistors)
  - MESFET
  - HBT
  - Schottky Diode (not Shockley)
  - MEM Devices
  - TRIAC/SCR
  - ....
Basic Devices

• Standard CMOS Process
  – MOS Transistors
    • n-channel
    • p-channel
  – Capacitors
  – Resistors
  – Diodes
  – BJT (in some processes)
    • npn
    • pnp
  – JFET (in some processes)
    • n-channel
    • p-channel

• Niche Devices
  – Photodetectors
  – MESFET
  – Schottky Diode (not Shockley)
  – MEM Devices
    – Triac/SCR
    – ....

Primary Consideration in This Course

Some Consideration in This Course
Basic Devices and Device Models

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT
Basic Devices and Device Models

Resistor

• Diode
• Capacitor
• MOSFET
• BJT

Resistors were discussed when considering interconnects so will only be briefly reviewed here.
Resistors

• Generally thin-film devices
• Almost any thin-film layer can be used as a resistor
  – Diffused resistors
  – Poly Resistors
  – Metal Resistors
  – “Thin-film” adders (SiCr or NiCr)
• Subject to process variations, gradient effects and local random variations
• Often temperature and voltage dependent
  – Ambient temperature
  – Local Heating
• Nonlinearities often a cause of distortion when used in circuits
• Trimming possible resistors
  – Laser, links, switches
Resistor Model

Model:

\[ R = \frac{V}{I} \]
**Resistivity**

- Volumetric measure of conduction capability of a material

\[ \rho = \frac{AR}{L} \]

for homogeneous material, \( \rho \perp A, R, L \)

Area is \( A \)

units: ohm cm
Sheet Resistance

\[ R_{\square} = \frac{RW}{L} \quad (\text{for } d \ll w, d \ll L) \quad \text{units: ohms/} \cdot \]

for homogeneous materials, \( R \) is independent of \( W, L, R \)
Relationship between $\rho$ and $R_{\square}$

\[ R_{\square} = \frac{RW}{L} \]

\[ \rho = \frac{AR}{L} \]

\[ \rho = \frac{A}{W} R_{\square} = \frac{Wd}{W} R_{\square} = d \times R_{\square} \]

Number of squares, $N_S$, often used instead of $L / W$ in determining resistance of film resistors

\[ R = R_{\square} N_S \]
Example 1

\[ R = ? \]
Example 1

\[ \frac{L}{W} = N_s \]
Example 1

\[ R = ? \]
Example 1

\[ R = ? \]

\[ N_S = 8.4 \]

\[ R = R_s (8.4) \]
Corners in Film Resistors

Rule of Thumb: .55 squares for each corner
Example 2

Determine $R$ if $R = 100 \, \Omega$
Example 2

\[ N_s = 17.1 \]
\[ R = (17.1) \, R \]
\[ R = 1710 \, \Omega \]
Resistivity of Materials used in Semiconductor Processing

- Cu: $1.7E-6 \ \Omega \text{cm}$
- Al: $2.7E-4 \ \Omega \text{cm}$
- Gold: $2.4E-6 \ \Omega \text{cm}$
- Platinum: $3.0E-6 \ \Omega \text{cm}$
- Polysilicon: $1E-2 \text{ to } 1E4 \ \Omega \text{cm}$*
- n-Si: $0.25 \text{ to } 5 \ \Omega \text{cm}$*
- intrinsic Si: $2.5E5 \ \Omega \text{cm}$
- SiO$_2$: $E14 \ \Omega \text{cm}$

* But fixed in a given process
Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon

Dopant:
- Arsenic
- Boron
- Phosphorus

Impurity Concentration:
1e15 (cm⁻³)

Mobility:
1358.6941377260254 [cm²/V·s]

Resistivity:
4.590746148183427 [Ω-cm]

Calculations are for a silicon substrate.
Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon

Depant:
- Arsenic
- Boron
- Phosphorus

Impurity Concentration:
1e15 (cm⁻³)

Mobility:
461.9540345952693 [cm²/V·s]

Resistivity:
13.511075756839005 [Ω·cm]

Calculations are for a silicon substrate.
Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon

Dopant:
- Arsenic
- Boron
- Phosphorus

Impurity Concentration:

Mobility:

Resistivity:

Calculations are for a silicon substrate.

http://www.cleanroom.byu.edu/ResistivityCal.phtml
Temperature Coefficients

Used for indicating temperature sensitivity of resistors & capacitors

**For a resistor:**

\[
TCR = \left( 1 \frac{dR}{R \, dT} \right)_{\text{op. temp}} \times 10^6 \text{ ppm/°C}
\]

This diff eqn can easily be solved if TCR is a constant

\[
R(T_2) = R(T_1) e^{\frac{T_2 - T_1}{10^6} TCR}
\]

\[
R(T_2) \approx R(T_1) \left[ 1 + (T_2 - T_1) \frac{TCR}{10^6} \right]
\]

Identical Expressions for Capacitors
Voltage Coefficients

Used for indicating voltage sensitivity of resistors & capacitors

For a resistor:

$$\text{VCR} = \left( \frac{1}{R} \frac{dR}{dV} \right)_{\text{ref voltage}} \cdot 10^6 \text{ ppm/V}$$

This diff eqn can easily be solved if VCR is a constant

$$R(V_2) = R(V_1) e^{\frac{V_2-V_1}{10^6} \text{VCR}}$$

$$R(V_2) \approx R(V_1) \left[ 1 + \left(V_2 - V_1\right)\frac{\text{VCR}}{10^6} \right]$$

Identical Expressions for Capacitors
Temperature and Voltage Coefficients

- Temperature and voltage coefficients often quite large for diffused resistors
- Temperature and voltage coefficients often quite small for poly and metal resistors
<table>
<thead>
<tr>
<th>Type of layer</th>
<th>Sheet Resistance $\Omega/\square$</th>
<th>Accuracy %</th>
<th>Temperature Coefficient ppm/°C</th>
<th>Voltage Coefficient ppm/V</th>
</tr>
</thead>
<tbody>
<tr>
<td>n + diff</td>
<td>30 - 50</td>
<td>20 - 40</td>
<td>200 - 1K</td>
<td>50 - 300</td>
</tr>
<tr>
<td>p + diff</td>
<td>50 - 150</td>
<td>20 - 40</td>
<td>200 - 1K</td>
<td>50 - 300</td>
</tr>
<tr>
<td>n - well</td>
<td>2K - 4K</td>
<td>15 - 30</td>
<td>5K</td>
<td>10K</td>
</tr>
<tr>
<td>p - well</td>
<td>3K - 6K</td>
<td>15 - 30</td>
<td>5K</td>
<td>10K</td>
</tr>
<tr>
<td>pinched n - well</td>
<td>6K - 10K</td>
<td>25 - 40</td>
<td>10K</td>
<td>20K</td>
</tr>
<tr>
<td>pinched p - well</td>
<td>9K - 13K</td>
<td>25 - 40</td>
<td>10K</td>
<td>20K</td>
</tr>
<tr>
<td>first poly</td>
<td>20 - 40</td>
<td>25 - 40</td>
<td>500 - 1500</td>
<td>20 - 200</td>
</tr>
<tr>
<td>second poly</td>
<td>15 - 40</td>
<td>25 - 40</td>
<td>500 - 1500</td>
<td>20 - 200</td>
</tr>
</tbody>
</table>

From:F. Maloberti : Design of CMOS Analog Integrated Circuits - “Resistors, Capacitors, Switches”
Example: Determine the percent change in resistance of a 5K Polysilicon resistor as the temperature increases from 30°C to 60°C if the TCR is constant and equal to 1500 ppm/°C

\[
R(T_2) \approx R(T_1) \left[ 1 + (T_2 - T_1) \frac{TCR}{10^6} \right]
\]

\[
R(T_2) \approx R(T_1) \left[ 1 + (30^\circ C) \frac{1500}{10^6} \right]
\]

\[
R(T_2) \approx R(T_1) [1 + .045]
\]

\[
R(T_2) \approx R(T_1) [1.045]
\]

Thus the resistor increases by 4.5%
Basic Devices and Device Models

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT
**Periodic Table of the Elements**

![Periodic Table Image](http://www.dayah.com/periodic/Images/periodic%20table.png)
<table>
<thead>
<tr>
<th>IIIA</th>
<th>IVA</th>
<th>VA</th>
<th>VIA</th>
<th>VIIA</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>5</td>
<td>6</td>
<td>7</td>
<td>8</td>
</tr>
<tr>
<td>B</td>
<td>C</td>
<td>N</td>
<td>O</td>
<td>F</td>
</tr>
<tr>
<td>Boron</td>
<td>Carbon</td>
<td>Nitrogen</td>
<td>Oxygen</td>
<td>Fluorine</td>
</tr>
<tr>
<td>10.811</td>
<td>12.0107</td>
<td>14.00674</td>
<td>15.9994</td>
<td>18.9984032</td>
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<tr>
<td></td>
<td>13</td>
<td>14</td>
<td>15</td>
<td>16</td>
</tr>
<tr>
<td>Al</td>
<td>Si</td>
<td>P</td>
<td>S</td>
<td>Cl</td>
</tr>
<tr>
<td>Aluminium</td>
<td>Silicon</td>
<td>Phosphorus</td>
<td>Sulfur</td>
<td>Chlorine</td>
</tr>
<tr>
<td>26.981538</td>
<td>28.0855</td>
<td>30.973761</td>
<td>32.066</td>
<td>35.453</td>
</tr>
<tr>
<td></td>
<td>31</td>
<td>32</td>
<td>33</td>
<td>34</td>
</tr>
<tr>
<td>Ga</td>
<td>Ge</td>
<td>As</td>
<td>Se</td>
<td>Br</td>
</tr>
<tr>
<td>Gallium</td>
<td>Germanium</td>
<td>Arsenic</td>
<td>Selenium</td>
<td>Bromine</td>
</tr>
<tr>
<td>69.723</td>
<td>72.64</td>
<td>74.92160</td>
<td>78.96</td>
<td>79.904</td>
</tr>
<tr>
<td></td>
<td>49</td>
<td>50</td>
<td>51</td>
<td>52</td>
</tr>
<tr>
<td>In</td>
<td>Sn</td>
<td>Sb</td>
<td>Te</td>
<td>I</td>
</tr>
<tr>
<td>Indium</td>
<td>Tin</td>
<td>Antimony</td>
<td>Tellurium</td>
<td>Iodine</td>
</tr>
<tr>
<td>114.818</td>
<td>118.710</td>
<td>121.760</td>
<td>127.60</td>
<td>126.90447</td>
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<td></td>
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<td>84</td>
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<tr>
<td>Tl</td>
<td>Pb</td>
<td>Bi</td>
<td>Po</td>
<td>At</td>
</tr>
<tr>
<td>Thallium</td>
<td>Lead</td>
<td>Bismuth</td>
<td>Polonium</td>
<td>Astatine</td>
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<tr>
<td>204.3833</td>
<td>207.2</td>
<td>208.98038</td>
<td>(209)</td>
<td>(210)</td>
</tr>
</tbody>
</table>
All elements in group IV have 4 valence-band electrons.
Only 3 Valence-band Electrons

Serves as an “acceptor” of electrons
Acts as a p-type impurity when used as a silicon dopant

All elements in group III have 3 valence-band electrons
The Atom of Boron (B)

Serves as an “donor” of electrons
Acts as an \textit{n-type} impurity when used as a silicon dopant
All elements in group V have 5 valence-band electrons
The Atom of Phosphorus (P)
5  
B  
Boron 10.811  
1s² 2s² 2p¹

14  
Si  
Silicon 28.0855  
[Ne]3s² 3p²

15  
P  
Phosphorus 30.973762  
[Ne]3s² 3p³

33  
As  
Arsenic 74.92160  
[Ar]3d¹⁰ 4s² 4p³

51  
Sb  
Antimony 121.760  
[Kr]4d¹⁰ 5s² 5p³
Silicon Dopants in Semiconductor Processes

**B** (Boron) widely used a dopant for creating p-type regions

**P** (Phosphorus) widely used a dopant for creating n-type regions
(bulk doping, diffuses fast)

**As** (Arsenic) widely used a dopant for creating n-type regions
(Active region doping, diffuses slower)
End of Lecture 11