Exam 1  Friday Sept 22

- Students may bring 1 page of notes
- Next weeks HW assignment due on Wed Sept 20 at beginning of class
- No 5:00 p.m extension so solutions can be posted
- Those with special accommodation needs, please send me an email message or contact me so arrangements can be made
- Review session – Thursday Sept 21  6:30  Rm 1011 Coover
Back-end Processing

Semiconductor Processes

Devices in Semiconductor Processes

- Resistors
- Diodes
Review from Last Lecture

Patterning of Copper

Dual-Damascene Process

Copper Deposited on Surface

CMP Target
Resistance in Interconnects

The "Number of Squares" approach to resistance determination in thin films

\[ R = R_\square \left[ \frac{L}{W} \right] \]

Review from Last Lecture

The number of squares, \( N_S \), is 21.

\[ L / W = 21 \]

\[ R = R_\square N_S \]
Capacitance in Interconnects

Equivalent Circuit

\[ C_{12} = CD_{12} A_5 \]
\[ C_{1S} = CD_{1S} (A_1 + A_2 + A_5) \]
\[ C_{2S} = CD_{2S} (A_3 + A_4) \]
IC Fabrication Technology

• Crystal Preparation
• Masking
• Photolithographic Process
• Deposition
• Etching
• Diffusion
• Ion Implantation
• Oxidation
• Epitaxy
• Polysilicon
• Contacts, Interconnect and Metalization
• Planarization
Planarization

- Planarization used to keep surface planar during subsequent processing steps
  - Important for creating good quality layers in subsequent processing steps
  - Mechanically planarized
Generic Process Flow
Front End Process Integration for Fabrication of ICs

- Wafer Fabrication
- Mask Fabrication
- Epitaxy
- Photoresist
- Deposit or Implant
- Etch
- Strip
- Planarize

Back End Processing

Once for each mask
Front-End Process Flow

• Front-end processing steps analogous to a “recipe” for manufacturing an integrated circuit
• Recipes vary from one process to the next but the same basic steps are used throughout the industry
• Details of the recipe are generally considered proprietary
Back-End Process Flow

- Wafer Probe
- Wafer Dicing
- Die Attach
- Wire Attach (bonding)
- Package
- Test
- Ship
Wafer Dicing

Gang of slitng blades

Rotary stage indexer

Silicon wafer

X axis

Y axis

www.renishaw.com
Die Attach

1. Eutectic
2. Pre-form
3. Conductive Epoxy
Electrical Connections (Bonding)

- Wire Bonding
- Bump Bonding
Wire Bonding

Wire – gold or aluminum
25 μ in diameter
Wire Bonding

Excellent Animation showing process at:

http://www.kns.com/_Flash/CAP_BONDING_CYCLE.swf
Wire Bonding

Ball Bond

Wedge Bond
Ball Bonding Steps
Ball Bonding Tip

Approx 25µ
Wire Bonding

Ball Bond

Termination Bond

Ball Bond Photograph
Bump Bonding
Packaging

1. Many variants in packages now available
2. Considerable development ongoing on developing packaging technology
3. Cost can vary from few cents to tens of dollars
4. Must minimize product loss after packaged
5. Choice of package for a product is serious business
6. Designer invariably needs to know packaging plans and package models
Packaging
Pin Pitch Varies with Package Technology

All measurements are nominal in [mm].

<table>
<thead>
<tr>
<th>Name</th>
<th>Pin pitch</th>
<th>Size</th>
<th>Height</th>
</tr>
</thead>
<tbody>
<tr>
<td>DIP or DIL</td>
<td>2.54</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SOIC-16</td>
<td>1.27</td>
<td>3.9 x 10</td>
<td>1.72</td>
</tr>
<tr>
<td>SSOP</td>
<td>0.635</td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSSOP54-II</td>
<td>0.8</td>
<td>12.7 x 22.22</td>
<td>~1</td>
</tr>
<tr>
<td>PLCC44</td>
<td>1.27</td>
<td></td>
<td></td>
</tr>
<tr>
<td>PQ208[^1]</td>
<td>0.50</td>
<td>28 x 28</td>
<td>3.4</td>
</tr>
<tr>
<td>TQFP64</td>
<td>0.40</td>
<td>7 x 7</td>
<td>1.0</td>
</tr>
<tr>
<td>TQFP144[^2]</td>
<td>0.50</td>
<td>20 x 20</td>
<td>1.0</td>
</tr>
<tr>
<td>128PQFP</td>
<td>0.50</td>
<td>23.23 x 14.0</td>
<td>3.15</td>
</tr>
</tbody>
</table>

Many standard packages available today:


BCC: Bump Chip Carrier
BGA: Ball Grid Array, BGA graphic
BQFP: Bumpered Quad Flat Pack
CABGA/SSBGA: Chip Array/Small Scale Ball Grid Array
CBGA: Ceramic Ball Grid Array
CFP: Ceramic Flat Pack
CPGA: Ceramic Pin Grid Array, CPGA Graphic
CQFP: Ceramic Quad Flat Pack, CQFP Graphic
TBD: Ceramic Lead-Less Chip Carrier
DFN: Dual Flat Pack, No Lead
DLCC: Dual Lead-Less Chip Carrier (Ceramic)
ETQFP: Extra Thin Quad Flat Package
FBGA: Fine-pitch Ball Grid Array
fpBGA: Fine Pitch Ball Grid Array
HSBGA: Heat Slug Ball Grid Array
JLCC: J-Leaded Chip Carrier (Ceramic) J-Lead Picture
LBGA: Low-Profile Ball Grid Array
LCC: Leaded Chip Carrier LCC Graphic
LCC: Leadless Chip Carrier Un-formed LCC Graphic
LCCC: Leadless Ceramic Chip Carrier
LFBGA: Low-Profile, Fine-Pitch Ball Grid Array
LGA: Land Grid Array, LGA up [Pins are on the Motherboard, not the socket]
LLCC: Leadless Leadless Chip Carrier LLCC Graphic
LQFP: Low Profile Quad Flat Package
MCMBGA: Multi Chip Module Ball Grid Array
MCMCABGA: Multi Chip Module-Chip Array Ball Grid Array
MLCC: Micro Lead-frame Chip Carrier
PBGA: Plastic Ball Grid Array
PLCC: Plastic Leaded Chip Carrier
PQFD: Plastic Quad Flat Pack
PQFP: Plastic Quad Flat Pack
PSOP: Plastic Small-Outline Package PSOP graphic
QFP: Quad Flatpack QFP Graphics
QSOP: Quarter Size Outline Package [Quarter Pitch Small Outline Package]
SBGA: Super BGA - above 500 Pin count
SOIC: Small Outline IC
SO Flat Pack: Small Outline Flat Pack IC
SOJ: Small-Outline Package [J-Lead], J-Lead Picture
SOP: Small-Outline Package; SOP IC, Socket
SSOP: Shrink Small-Outline Package
TBGA: Thin Ball Grid Array
TQFP: Thin Quad Flat Pack TQFP Graphic
TSOP: Thin Small-Outline Package
TSSOP: Thin Shrink Small-Outline Package
TVSOP: Thin Very Small-Outline Package
VQFB: Very-thin Quad Flat Pack
Considerable activity today and for years to come on improving packaging technology

- Multiple die in a package
- Three-dimensional chip stacking
- Multiple levels of interconnect in stacks
- Through silicon via technology
- Power and heat management
- Cost driven and cost constrained
The following few slides come from a John Lau presentation.

**TSV Interposer: The Most Cost-Effective Integrator for 3D IC Integration**

John H. Lau  
Electronics & Optoelectronics Research Laboratories  
Industrial Technology Research Institute (ITRI)  
Chutung, Hsinchu, Taiwan 310, R.O.C.  
886-3591-3390, johnlau@itri.org.tw
3D IC Integration with Passive Interposer

- Memory
- Micro bump
- TSV
- CPU/Logic
- 3D IC Integration with Passive Interposer
- Micro Bump
- TSV/RDL/IPD
- Passive Interposer
TSV passive interposer supporting high-power chips (e.g., microprocessor and logic) on its top side and low-power chips (e.g., memory) on its bottom side.

Special underfills are needed between the Cu-filled interposer and all the chips. Ordinary underfills are needed between the interposer and the organic substrate.

ASME InterPACK2011-52189 (Lau)
Back-End Process Flow

- Wafer Probe
- Wafer Dicing
- Die Attach
- Wire Attach (bonding)
- Package
- Test
- Ship
Testing of Integrated Circuits

Most integrated circuits are tested twice

- **Wafer Probe Testing**
  - Quick test for functionality
  - Usually does not include much parametric testing
  - Relatively fast and low cost test
  - Package costs often quite large
  - Critical to avoid packaging defective parts

- **Packaged Part Testing**
  - Testing costs for packaged parts can be high
  - Extensive parametric tests done at package level for many parts
  - Data sheet parametrics with Max and Min values are usually tested on all Ics
  - Data sheet parametrics with Typ values are seldom tested
  - Occasionally require testing at two or more temperatures but this is costly
  - Critical to avoid packaging defective parts
Basic Semiconductor Processes

MOS (Metal Oxide Semiconductor)

1. NMOS  n-ch
2. PMOS  p-ch
3. CMOS  n-ch & p-ch
   • Basic Device:  MOSFET
   • Niche Device:  MESFET
   • Other Devices:  Diode
                   BJT
                   Resistors
                   Capacitors
                   Schottky Diode
Basic Semiconductor Processes

Bipolar

1. T^2L
2. ECL
3. I^2L
4. Linear ICs
   – Basic Device: BJT (Bipolar Junction Transistor)
   – Niche Devices: HBJT (Heterojunction Bipolar Transistor)
     HBT
   – Other Devices: Diode
     Resistor
     Capacitor
     Schottky Diode
     JFET (Junction Field Effect Transistor)
Basic Semiconductor Processes

Other Processes

• Thin and Thick Film Processes
  – Basic Device: Resistor

• BiMOS or BiCMOS
  – Combines both MOS & Bipolar Processes
  – Basic Devices: MOSFET & BJT

• SiGe
  – BJT with HBT implementation

• SiGe / MOS
  – Combines HBT & MOSFET technology

• SOI / SOS (Silicon on Insulator / Silicon on Sapphire)

• Twin-Well & Twin Tub CMOS
  – Very similar to basic CMOS but more optimal transistor char.
Devices in Semiconductor Processes

- Standard CMOS Process
  - MOS Transistors
    - n-channel
    - p-channel
  - Capacitors
  - Resistors
  - Diodes
  - BJT (decent in some processes)
    - npn
    - pnp
  - JFET (in some processes)
    - n-channel
    - p-channel

- Standard Bipolar Process
  - BJT
    - npn
    - pnp
  - JFET
    - n-channel
    - p-channel
  - Diodes
  - Resistors
  - Capacitors

- Niche Devices
  - Photodetectors (photodiodes, phototransistors, photoresistors)
  - MESFET
  - HBT
  - Schottky Diode (not Shockley)
  - MEM Devices
  - TRIAC/SCR
  - ....
Basic Devices

• **Standard CMOS Process**
  - MOS Transistors
    • n-channel
    • p-channel
  - Capacitors
  - Resistors
  - Diodes
  - BJT (in some processes)
    • npn
    • pnp
  - JFET (in some processes)
    • n-channel
    • p-channel

• **Niche Devices**
  - Photodetectors
  - MESFET
  - Schottky Diode *(not Shockley)*
  - MEM Devices
  - Triac/SCR
  - ....

Primary Consideration in This Course

Some Consideration in This Course
Basic Devices and Device Models

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT
Basic Devices and Device Models

- Resistor
  - Diode
  - Capacitor
  - MOSFET
  - BJT

Resistors were discussed when considering interconnects so will only be briefly reviewed here.
Resistors

- Generally thin-film devices
- Almost any thin-film layer can be used as a resistor
  - Diffused resistors
  - Poly Resistors
  - Metal Resistors
  - “Thin-film” adders (SiCr or NiCr)
- Subject to process variations, gradient effects and local random variations
- Often temperature and voltage dependent
  - Ambient temperature
  - Local Heating
- Nonlinearities often a cause of distortion when used in circuits
- Trimming possible resistors
  - Laser, links, switches
Resistor Model

Model:

\[ R = \frac{V}{I} \]
Resistivity

• Volumetric measure of conduction capability of a material

\[ \rho = \frac{AR}{L} \]

for homogeneous material, \( \rho \perp A, R, L \)

units: ohm cm
Sheet Resistance

\[ R_{\square} = \frac{R W}{L} \quad \text{ (for } d \ll w, d \ll L) \quad \text{ units: ohms} \]

for homogeneous materials, \( R_{\square} \) is independent of \( W, L, R \)
Relationship between $\rho$ and $R_{\square}$

$R_{\square} = \frac{RW}{L}$

$\rho = \frac{AR}{L}$

$\rho = \frac{A}{W}R_{\square} = \frac{W\cdot d}{W}R_{\square} = d \times R_{\square}$

Number of squares, $N_S$, often used instead of $L / W$ in determining resistance of film resistors

$R = R_{\square} N_S$
Example 1

\[ R = ? \]
Example 1

\[
\frac{L}{W} = N_s
\]
Example 1

\[ R = ? \]
Example 1

$R = \, ?$

$N_S = 8.4$

$R = R_s(8.4)$
Corners in Film Resistors

Rule of Thumb: .55 squares for each corner
Example 2

Determine $R$ if $R_1 = 100 \, \Omega$ /•
### Example 2

\[ N_S = 17.1 \]
\[ R = (17.1) R \]
\[ R = 1710 \, \Omega \]
Resistivity of Materials used in Semiconductor Processing

- Cu: \(1.7E-6 \ \Omega cm\)
- Al: \(2.7E-6 \ \Omega cm\)
- Gold: \(2.4E-6 \ \Omega cm\)
- Platinum: \(3.0E-6 \ \Omega cm\)
- Polysilicon: \(1E-2\) to \(1E4 \ \Omega cm^*\)
- n-Si: typically \(.25\) to \(5 \ \Omega cm^*\) (but larger range possible)
- intrinsic Si: \(2.5E5 \ \Omega cm\)
- SiO\(_2\): \(E14 \ \Omega cm\)

* But fixed in a given process
Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon

Dopant:
- Arsenic
- Boron
- Phosphorus

Impurity Concentration: $1 \times 10^{15}$ cm$^{-3}$

Calculate
Export to CSV

Mobility: 1358.6941377290254 cm$^2$/Vs
Resistivity: 4.580746148183427 $\Omega\cdot$cm

Calculations are for a silicon substrate.
Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon

- **Dopant:**
  - Arsenic
  - Boron
  - Phosphorus

- **Impurity Concentration:**
  - $1 \times 10^{15}$ (cm$^{-3}$)

- **Mobility:**
  - 451.9540345952693 [cm$^2$/V.s]

- **Resistivity:**
  - 13.511075765839005 [ohm-cm]

Calculations are for a silicon substrate.

Graph showing the relationship between impurity concentration and resistivity. The graph is a downward sloping curve, indicating that resistivity decreases as impurity concentration increases.
Resistivity & Mobility Calculator/Graph for Various Doping Concentrations in Silicon

- Dopant: Phosphorus
- Impurity Concentration: $1 \times 10^{15}$ cm$^{-3}$
- Mobility: 1.362 $\times 10^{6}$ [cm$^2$/V-s]
- Resistivity: 4.582 $\times 10^{6}$ [Ohm-cm]

Calculations are for a silicon substrate.
Temperature Coefficients

Used for indicating temperature sensitivity of resistors & capacitors

For a resistor:

\[ TCR = \left( \frac{1}{R} \frac{dR}{dT} \right)_{\text{op. temp}} \cdot 10^6 \text{ ppm/°C} \]

This diff eqn can easily be solved if TCR is a constant

\[ R(T_2) = R(T_1) e^{\frac{T_2 - T_1}{10^6 TCR}} \]

\[ R(T_2) \approx R(T_1) \left[ 1 + (T_2 - T_1) \frac{TCR}{10^6} \right] \]

Identical Expressions for Capacitors
Voltage Coefficients

Used for indicating voltage sensitivity of resistors & capacitors

For a resistor:

\[
VCR = \left( \frac{1}{R} \frac{dR}{dV} \right)_{\text{ref voltage}} \cdot 10^6 \text{ ppm/V}
\]

This diff eqn can easily be solved if VCR is a constant

\[
R(V_2) = R(V_1) e^{\frac{V_2 - V_1}{10^6} VCR}
\]

\[
R(V_2) \approx R(V_1) \left[ 1 + (V_2 - V_1) \frac{VCR}{10^6} \right]
\]

Identical Expressions for Capacitors
Temperature and Voltage Coefficients

• Temperature and voltage coefficients often quite large for diffused resistors
• Temperature and voltage coefficients often quite small for poly and metal resistors
<table>
<thead>
<tr>
<th>Type of layer</th>
<th>Sheet Resistance $\Omega/\square$</th>
<th>Accuracy %</th>
<th>Temperature Coefficient ppm/$^\circ$C</th>
<th>Voltage Coefficient ppm/V</th>
</tr>
</thead>
<tbody>
<tr>
<td>n + diff</td>
<td>30 - 50</td>
<td>20 - 40</td>
<td>200 - 1K</td>
<td>50 - 300</td>
</tr>
<tr>
<td>p + diff</td>
<td>50 - 150</td>
<td>20 - 40</td>
<td>200 - 1K</td>
<td>50 - 300</td>
</tr>
<tr>
<td>n - well</td>
<td>2K - 4K</td>
<td>15 - 30</td>
<td>5K</td>
<td>10K</td>
</tr>
<tr>
<td>p - well</td>
<td>3K - 6K</td>
<td>15 - 30</td>
<td>5K</td>
<td>10K</td>
</tr>
<tr>
<td>pinched n - well</td>
<td>6K - 10K</td>
<td>25 - 40</td>
<td>10K</td>
<td>20K</td>
</tr>
<tr>
<td>pinched p - well</td>
<td>9K - 13K</td>
<td>25 - 40</td>
<td>10K</td>
<td>20K</td>
</tr>
<tr>
<td>first poly</td>
<td>20 - 40</td>
<td>25 - 40</td>
<td>500 - 1500</td>
<td>20 - 200</td>
</tr>
<tr>
<td>second poly</td>
<td>15 - 40</td>
<td>25 - 40</td>
<td>500 - 1500</td>
<td>20 - 200</td>
</tr>
</tbody>
</table>
Example: Determine the percent change in resistance of a 5K Polysilicon resistor as the temperature increases from 30°C to 60°C if the TCR is constant and equal to 1500 ppm/°C

\[
R(T_2) \approx R(T_1) \left[ 1 + (T_2 - T_1) \frac{TCR}{10^6} \right]
\]

\[
R(T_2) \approx R(T_1) \left[ 1 + (30^\circ C) \frac{1500}{10^6} \right]
\]

\[
R(T_2) \approx R(T_1)[1 + .045]
\]

\[
R(T_2) \approx R(T_1)[1.045]
\]

Thus the resistor increases by 4.5%
End of Lecture 11