Copper Interconnects
Resistance and Capacitance in Interconnects
Exam 1 Schedule

Exam 1 will be given on Friday September 18

Format: Open-Book, Open Notes

Exam will be posted at 9:00 a.m. on the class WEB site and will be due at 1:00 p.m. as a .pdf upload on CANVAS

It will be structured to be a 50-minute closed-book closed-notes exam but administered as an open-book, open-notes exam with a 4 hour open interval so reserving the normal lecture period for taking the exam should provide adequate time

Honor System Expected

It is expected that this exam be an individual effort and that students should not have input in any form from anyone else during the 4-hour open interval of the exam except from the course instructor who will be responding to email messages from 11:00 a.m. to 1:00 p.m. on the date of the exam.

Special Accommodations

For anyone with approved special accommodations, the 4-hour open interval should cover extra time allocations but if for any reason this does not meet special accommodation expectations, please contact the instructor by Monday Sept. 14 if alternative accommodations are requested.
Copper Interconnects

Practical methods of realizing copper interconnects took many years to develop.

Copper interconnects widely used in some processes today.
Patterning of Copper

Damascene Process

Contact Opening after SiO₂ etch

Photoresist
Patterning of Copper

Damascene Process

Tungsten (W)

CMP Target

W has excellent conformality when formed from $WF_6$

Applied with CVD $WF_6 + 3H_2 \rightarrow W + 6HF$
Chemical-Mechanical Planarization (CMP)

- Polishing Pad and Wafer Rotate in non-concentric pattern to thin, polish, and planarize surface
- Abrasive/Chemical polishing
- Depth and planarity are critical

Acknowledgement:
http://en.wikipedia.org/wiki/Chemical-mechanical_planarization
Patterning of Copper

Damascene Process
After first CMP Step

W-plug

CMP Target
Patterning of Copper

Damascene Process
After first CMP Step

Oxidation
Patterning of Copper

Damasocene Process

Photoresist Patterned with Metal Mask Defines Trench
Patterning of Copper

Damascene Process

Shallow Trench after Etch

W-plug
Patterning of Copper

Damasocene Process

(BARRIER METAL ADDED BEFORE COPPER TO CONTAIN THE COPPER ATOMS)
Patterning of Copper

Damascone Process

W-plug

Copper Deposition
Copper is deposited or electroplated (Barrier Metal Used for Electroplating Seed)
Patterning of Copper

Damascone Process

After Second CMP Step

W-plug

Copper

CMP Target
Patterning of Copper

Dual-Damascene Process

Shallow Trench Defined in PR with Metal Mask
Patterning of Copper

Dual-Damascene Process

Shallow Trench After Etch

Photoresist
Patterning of Copper

Dual-Damascene Process

Via Defined in PR with Via Mask

Photoresist
Patterning of Copper

Dual-Damascene Process

Via Etch Defines Contact Region

Photoresist

(Barrier Metal added before copper but not shown)
Patterning of Copper

Dual-Damascene Process

Copper Deposited on Surface

Copper is deposited or electroplated (Barrier Metal Used for Electroplating Seed)
Patterning of Copper

Dual-Damascene Process

Copper Deposited on Surface

CMP Target
Patterning of Copper

Dual-Damascene Process

Copper Via

Copper Interconnect

CMP Target
Patterning of Copper

Both Damascene Processes Realize Same Structure

**Damascene Process**
- Two Dielectric Deposition Steps
- Two CMP Steps
- Two Metal Deposition Steps
- Two Dielectric Etches
- W-Plug

**Dual-Damascene Process**
- One Dielectric Deposition Steps
- One CMP Steps
- One Metal Deposition Steps
- Two Dielectric Etches
- Via formed with metal step
Multiple Level Interconnects

3-rd level metal connection to n-active without stacked vias
Multiple Level Interconnects

3-rd level metal connection to n-active with stacked vias
Interconnect Layers May Vary in Thickness or Be Mostly Uniform

**FIG 4.30** Interconnect geometry

<table>
<thead>
<tr>
<th>Layer</th>
<th>t (nm)</th>
<th>w (nm)</th>
<th>s (nm)</th>
<th>AR</th>
</tr>
</thead>
<tbody>
<tr>
<td>6</td>
<td>1720</td>
<td>860</td>
<td>860</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>1000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>1600</td>
<td>800</td>
<td>800</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>1000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>1080</td>
<td>540</td>
<td>540</td>
<td>2.0</td>
</tr>
<tr>
<td></td>
<td>700</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>700</td>
<td>320</td>
<td>320</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>700</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>700</td>
<td>320</td>
<td>320</td>
<td>2.2</td>
</tr>
<tr>
<td></td>
<td>700</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>480</td>
<td>250</td>
<td>250</td>
<td>1.9</td>
</tr>
<tr>
<td></td>
<td>800</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**FIG 4.31** Layer stack for 6-metal Intel 180 nm process

12.5μ
Interconnects

- Metal is preferred interconnect
  - Because conductivity is high
- Parasitic capacitances and resistances of concern in all interconnects
- Polysilicon used for short interconnects
  - Silicided to reduce resistance
  - Unsilicided when used as resistors
- Diffusion used for short interconnects
  - Parasitic capacitances are high
Interconnects

• Metal is preferred interconnect
  – Because conductivity is high

Parasitic capacitances and resistances of concern in all interconnects

• Polysilicon used for short interconnects
  – Silicided to reduce resistance
  – Unsilicided when used as resistors

• Diffusion used for short interconnects
  – Parasitic capacitances are high
Resistance in Interconnects

\[ R = \rho \frac{L}{A} \]

where:
- \( R \) is the resistance
- \( \rho \) is the resistivity of the material
- \( L \) is the length of the interconnect
- \( A \) is the cross-sectional area of the interconnect

The diagram shows a rectangular interconnect with dimensions L and W, and a cross-sectional area A, with resistivity \( \rho \) leading to resistance R.
Resistance in Interconnects

\[ R = \frac{L}{A} \rho \]

\( \rho \) independent of geometry and characteristic of the process
Resistance in Interconnects

H << W and H << L in most processes
Interconnect behaves as a “thin” film
Sheet resistance often used instead of conductivity to characterize film

\[ R = \frac{L}{A} \rho = \frac{L}{W} \left[ \frac{\rho}{H} \right] \]

\[ R_\square = \frac{\rho}{H} \quad \text{and} \quad R = R_\square \left[ \frac{L}{W} \right] \]
Resistance in Interconnects

The “Number of Squares” approach to resistance determination in thin films

\[ R = R_{\square} \frac{L}{W} \]

\[ N_S = 21 \]

\[ L / W = 21 \]

\[ R = R_{\square} N_S \]
Resistance in Interconnects

 Fractions of squares can be represented by their fraction.

 Corners contribute about .55 squares.

 The “squares” approach is not exact but is good enough for calculating resistance in almost all applications.

 In this example:

 $$N_S = 12 + .55 + .7 = 13.25$$

 $$R = R \ bullet 13.25$$
Example:

The layout of a film resistor with electrodes A and B is shown. If the sheet resistance of the film is 40 Ω/□, determine the resistance between nodes A and B.
Solution

\[ N_S = 9 + 9 + 3 + 2(\cdot 55) = 22.1 \]

\[ R_{AB} = R_{\square N_S} = 40 \times 22.1 = 884 \Omega \]
Resistance in Interconnects
(can be used to build resistors!)

- Serpentine often used when large resistance required
- Polysilicon or diffusion often used for resistor creation
- Effective at managing the aspect ratio of large resistors
- May include hundreds or even thousands of squares
Resistance in Interconnects
(can be used to build resistors!)

Area requirements determined by both minimum width and minimum spacing design rules
Capacitance in Interconnects

\[ C = C_D A \]

\( C_D \) is the capacitance density and \( A \) is the area of the overlap

(actually there is also a small fringe capacitance that has been neglected)
Capacitance in Interconnects

\[ C = C_D A \]

fringe capacitances denoted by \( C_{F1}, C_{F2}, C_{F3} \) and \( C_{F4} \)

\[ C_F = C_{F1} + C_{F2} + C_{F3} + C_{F2} \] is usually small compared to \( C \)
Capacitance in Interconnects

$$C_{12} = CD_{12} A_5$$

$$C_{1S} = CD_{1S} (A_1 + A_2 + A_5)$$

$$C_{2S} = CD_{2S} (A_3 + A_4)$$
Example

Two metal layers, Metal 1 and Metal 2, are shown. Both are above field oxide. Determine the capacitance between Metal 1 and Metal 2. Assume the process has capacitance densities from M₁ to substrate of .05fF/μm², from M₁ to M₂ of .07fF/μm² and from M₂ to substrate of .025fF/μm².
Example

Solution

\[ A_{C_1C_2} = (20\mu)^2 = 400\mu^2 \]

The capacitance density from \( M_1 \) to \( M_2 \) is \( 0.07 \text{fF}/\mu^2 \)

\[ C_{12} = A_{C_1C_2} \cdot C_{D12} = 400\mu^2 \cdot 0.07\text{fF}/\mu^2 = 28\text{fF} \]
Capacitance and Resistance in Interconnects

• See MOSIS WEB site for process parameters that characterize parasitic resistances and capacitances

www.mosis.org
MOSIS WAFER ACCEPTANCE TESTS

RUN: T6AU
TECHNOLOGY: SCN05

VENDOR: AMIS
FEATURE SIZE: 0.5 microns

Run type: SKD

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: American Microsystems, Inc. C5

<table>
<thead>
<tr>
<th>TRANSISTOR PARAMETERS</th>
<th>W/L</th>
<th>N-CHANNEL</th>
<th>P-CHANNEL</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>MINIMUM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vth</td>
<td>3.0/0.6</td>
<td>0.79</td>
<td>-0.92</td>
<td>volts</td>
</tr>
<tr>
<td>SHORT</td>
<td>20.0/0.6</td>
<td>446</td>
<td>-239</td>
<td>uA/um</td>
</tr>
<tr>
<td>Idss</td>
<td></td>
<td>0.68</td>
<td>-0.90</td>
<td>volts</td>
</tr>
<tr>
<td>Vth</td>
<td></td>
<td>10.0</td>
<td>-10.0</td>
<td>volts</td>
</tr>
<tr>
<td>WIDE</td>
<td>20.0/0.6</td>
<td>&lt; 2.5</td>
<td>&lt; 2.5</td>
<td>pA/um</td>
</tr>
<tr>
<td>LARGF</td>
<td>50/50</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vth</td>
<td></td>
<td>0.68</td>
<td>-0.95</td>
<td>volts</td>
</tr>
<tr>
<td>Vjbd</td>
<td></td>
<td>10.9</td>
<td>-11.6</td>
<td>volts</td>
</tr>
<tr>
<td>Ijkl</td>
<td>&lt;50.0</td>
<td>&lt;50.0</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>Gamma</td>
<td>0.48</td>
<td>0.58</td>
<td>V^0.5</td>
<td></td>
</tr>
<tr>
<td>K' (Uo*Cox/2)</td>
<td>56.4</td>
<td>-18.2</td>
<td>uA/V^2</td>
<td></td>
</tr>
<tr>
<td>Low-field Mobility</td>
<td>463.87</td>
<td>149.69</td>
<td>cm^2/V*s</td>
<td></td>
</tr>
</tbody>
</table>

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameter XL in your SPICE model card.

<table>
<thead>
<tr>
<th>Design Technology</th>
<th>XL (um)</th>
<th>XW (um)</th>
</tr>
</thead>
<tbody>
<tr>
<td>--------------------</td>
<td>---------</td>
<td>---------</td>
</tr>
<tr>
<td>-------------------</td>
<td>---------</td>
<td>---------</td>
</tr>
<tr>
<td>Process Parameters</td>
<td>N+</td>
<td>P+</td>
</tr>
<tr>
<td>-------------------------</td>
<td>-----</td>
<td>-----</td>
</tr>
<tr>
<td>Sheet Resistance</td>
<td>83.5</td>
<td>105.3</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>64.9</td>
<td>149.7</td>
</tr>
<tr>
<td>Gate Oxide Thickness</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Process Parameters</th>
<th>M3</th>
<th>N\PLY</th>
<th>N_W</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>0.05</td>
<td>824</td>
<td>816</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>0.79</td>
<td></td>
<td></td>
<td>ohms</td>
</tr>
</tbody>
</table>

**Comments:** N\POLY is N-well under polysilicon.

<table>
<thead>
<tr>
<th>Capacitance Parameters</th>
<th>N+</th>
<th>P+</th>
<th>Poly</th>
<th>Poly2</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>N_W</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (substrate)</td>
<td>425</td>
<td>731</td>
<td>84</td>
<td></td>
<td>27</td>
<td>12</td>
<td>7</td>
<td>37</td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (N+active)</td>
<td>2434</td>
<td></td>
<td></td>
<td></td>
<td>35</td>
<td>16</td>
<td>11</td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (P+active)</td>
<td>2335</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (poly)</td>
<td>938</td>
<td>56</td>
<td>15</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (poly2)</td>
<td>49</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal1)</td>
<td></td>
<td>31</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal2)</td>
<td></td>
<td>35</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Fringe (substrate)</td>
<td>344</td>
<td>238</td>
<td>49</td>
<td>33</td>
<td>23</td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (poly)</td>
<td>59</td>
<td>38</td>
<td>28</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal1)</td>
<td>51</td>
<td>34</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal2)</td>
<td>52</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Overlap (N+active)</td>
<td>232</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Overlap (P+active)</td>
<td>312</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Circuit Parameters</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverters</td>
<td>K</td>
</tr>
<tr>
<td>Vinv</td>
<td>1.0</td>
</tr>
<tr>
<td>Vinv</td>
<td>1.5</td>
</tr>
<tr>
<td>Vol (100 uA)</td>
<td>2.0</td>
</tr>
</tbody>
</table>
Voh (100 uA) 2.0 4.85 volts
Vinv 2.0 2.46 volts
Gain 2.0 -19.72

Ring Oscillator Freq.
DIV256 (31-stg, 5.0V) 95.31 MHz
D256_WIDE (31-stg, 5.0V) 147.94 MHz

Ring Oscillator Power
DIV256 (31-stg, 5.0V) 0.49 uW/MHz/gate
D256_WIDE (31-stg, 5.0V) 1.01 uW/MHz/gate

COMMENTS: SUBMICRON

☐ T6AU SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jan 11/07
* LOT: T6AU
* Temperature_parameters=Default

.PROCESS CMOSN NMS (LEVEL = 49)
.VERSION = 3.1
TNOM = 27
TOX = 1.42E-8

XJ = 1.5E-7
NCH = 1.7E17
VTH0 = 0.629035

K1 = 0.8976376
K2 = -0.09255
K3 = 24.0984767

K3B = -8.2369696
W0 = 1.041146E-8
NLX = 1E-9

DVTOW = 0
DVT1W = 0
DVT2W = 0

DVT0 = 2.7123969
DVT1 = 0.4232931
DVT2 = -0.1403765

U0 = 451.2322004
UA = 3.091785E-13
UB = 1.702517E-18

UC = 1.22401E-11
VSAT = 1.715884E5
A0 = 0.6580918

AGS = 0.130484
B0 = 2.446405E-6
B1 = 5E-6

KETA = -3.043349E-3
A1 = 8.18159E-7
A2 = 0.3363058

RDSW = 1.367055E3
PRWG = 0.0328586
PRWB = 0.0104806

WR = 1
WINT = 2.443677E-7
LINT = 6.999776E-8

XL = 1E-7
XW = 0

DWB = 3.676235E-8
VOFF = -1.493503E-4
NFACTOR = 1.0354201

CIT = 0
CDSC = 2.4E-4
CDSCD = 0

CDSCB = 0
ETA0 = 2.342963E-3
ETAB = -1.5324E-4

DSUB = 0.0764123
PCLM = 2.5941582
PDIBLC1 = 0.8187825

PDIBLC2 = 2.366707E-3
PDIBLCB = -0.0431505
DROUT = 0.9919348

PSCBE1 = 6.611774E8
PSCBE2 = 3.238266E-4
PVAG = 0

DELTA = 0.01
RSH = 83.5
MOMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -0.11
+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+WLN = 0 WLN = 1 WW = 0
+WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.32E-10 CGSO = 2.32E-10 CGBO = 1E-9
+CJ = 4.282017E-4 PB = 0.9317787 MJ = 0.4495867
+CJSW = 3.034055E-10 PBSW = 0.8 MJSW = 0.1713852
+CJSGW = 1.64E-10 PBSWG = 0.8 MJSWG = 0.1713852
+CF = 0 VTH0 = 0.0520855 PRDSW = 112.8875816
+PK2 = -0.0289036 WKETA = -0.0237483 LKETA = 1.728324E-3 )
* .MODEL CMOSP PMOS ( LEVEL = 49
+VERSION = 3.1 TNOM = 27 TOX = 1.42E-8
+XJ = 1.5E-7 NCH = 1.7E17 VTH0 = -0.9232867
+K1 = 0.5464347 K2 = 8.119291E-3 K3 = 5.1623206
+K3B = -0.8373484 W0 = 1.30945E-8 NLX = 5.772187E-8
+DVTOW = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 2.0973823 DVT1 = 0.5356454 DVT2 = -0.1185455
+U0 = 220.5922586 UA = 3.144939E-9 UB = 1E-21
+UC = -6.19354E-11 VSAT = 1.176415E5 A0 = 0.8441929
+AGS = 0.1447245 B0 = 1.149181E-6 B1 = 5E-6
+KETA = -1.093365E-3 A1 = 3.467482E-4 A2 = 0.4667486
+RDSW = 3E3 PRWG = -0.0418549 PRWB = -0.0212201
+WR = 1 WINT = 3.007497E-7 LINT = 1.040439E-7
+XL = 1E-7 WX = 0 DWG = -2.133809E-8
+DWB = 1.706031E-8 VOFF = -0.0801591 NFACTOR = 0.9468597
+CI = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 0.4060383 ETAB = -0.0633609
+DUB = 1 PCLM = 2.2703293 PDIBLC1 = 0.0279014
+PDIBLC2 = 3.201161E-3 PDIBLCB = -0.057478 DROUT = 0.1718548
+PSCBE1 = 4.876974E9 PSCBE2 = 5E-10 PVAG = 0
+DELTA = 0.01 RS = 105.3 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -0.11
+K1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+WLN = 0 WLN = 1 WW = 0
+WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 3.12E-10 CGSO = 3.12E-10 CGBO = 1E-9
+CJ     = 7.254264E-4   PB     = 0.9682229   MJ     = 0.4969013
+CJSW   = 2.496599E-10  PBSW   = 0.99     MJSW   = 0.386204
+CJSWG  = 6.4E-11       PBSWG  = 0.99     MJSWG  = 0.386204
+CF     = 0             PVTH0  = 5.98016E-3 PRDSW  = 14.8598424
+PK2    = 3.73981E-3    WKETA  = 7.286716E-4 LKETA  = -4.768569E-3  
*
MOSIS WAFER ACCEPTANCE TESTS

RUN: T4BK (MM_NON-EPIT-THK-MTL)
TECHNOLOGY: SCN018

VENDOR: TSMC
FEATURE SIZE: 0.18 microns

INTRODUCTION: This report contains the lot average results obtained by MOSIS from measurements of MOSIS test structures on each wafer of this fabrication lot. SPICE parameters obtained from similar measurements on a selected wafer are also attached.

COMMENTS: DSCN0M018_TSMC

<table>
<thead>
<tr>
<th>TRANSISTOR PARAMETERS</th>
<th>W/L</th>
<th>N-CHANNEL</th>
<th>P-CHANNEL</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>MINIMUM</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vth</td>
<td>0.27/0.18</td>
<td>0.50</td>
<td>-0.53</td>
<td>volts</td>
</tr>
<tr>
<td>SHORT</td>
<td>20.0/0.18</td>
<td>571</td>
<td>-266</td>
<td>uA/um</td>
</tr>
<tr>
<td>Idss</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vth</td>
<td>0.51</td>
<td>-0.53</td>
<td>volts</td>
<td></td>
</tr>
<tr>
<td>Vpt</td>
<td>4.7</td>
<td>-5.5</td>
<td>volts</td>
<td></td>
</tr>
<tr>
<td>WIDE</td>
<td>20.0/0.18</td>
<td>22.0</td>
<td>-5.6</td>
<td>pA/um</td>
</tr>
<tr>
<td>Ids0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LARGE</td>
<td>50/50</td>
<td>0.42</td>
<td>-0.41</td>
<td>volts</td>
</tr>
<tr>
<td>Vth</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vjbd</td>
<td>3.1</td>
<td>-4.1</td>
<td>volts</td>
<td></td>
</tr>
<tr>
<td>Ijlk</td>
<td>&lt;50.0</td>
<td>&lt;50.0</td>
<td>pA</td>
<td></td>
</tr>
<tr>
<td>K' (Uo*Cox/2)</td>
<td>171.8</td>
<td>-36.3</td>
<td>uA/V^2</td>
<td></td>
</tr>
<tr>
<td>Low-field Mobility</td>
<td>398.02</td>
<td>84.10</td>
<td>cm^2/V*s</td>
<td></td>
</tr>
</tbody>
</table>

COMMENTS: Poly bias varies with design technology. To account for mask bias use the appropriate value for the parameters XL and XW in your SPECTRE model card.

<table>
<thead>
<tr>
<th>FOX TRANSISTORS</th>
<th>GATE</th>
<th>N+ACTIVE</th>
<th>P+ACTIVE</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vth</td>
<td>Poly</td>
<td>&gt;6.6</td>
<td>&lt;-6.6</td>
<td>volts</td>
</tr>
<tr>
<td>PROCESS PARAMETERS</td>
<td>M3</td>
<td>POLY_HRI</td>
<td>M4</td>
<td>M5</td>
</tr>
<tr>
<td>-------------------</td>
<td>----</td>
<td>----------</td>
<td>----</td>
<td>----</td>
</tr>
<tr>
<td>Sheet Resistance</td>
<td>0.08</td>
<td>991.5</td>
<td>0.08</td>
<td>0.08</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>8.97</td>
<td>14.09</td>
<td>18.84</td>
<td>21.44</td>
</tr>
</tbody>
</table>

**COMMENTS:** BLK is silicide block.

<table>
<thead>
<tr>
<th>CAPACITANCE PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
<th>R_W</th>
<th>D_N_W</th>
<th>M5P</th>
<th>N_W</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (substrate)</td>
<td>998</td>
<td>1152</td>
<td>103</td>
<td>39</td>
<td>19</td>
<td>13</td>
<td>9</td>
<td>8</td>
<td>3</td>
<td>129</td>
<td>127</td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (N+active)</td>
<td>8566</td>
<td>54</td>
<td>21</td>
<td>14</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (P+active)</td>
<td>8324</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (poly)</td>
<td>64</td>
<td>18</td>
<td>10</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal1)</td>
<td>44</td>
<td>16</td>
<td>10</td>
<td>7</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal2)</td>
<td>38</td>
<td>15</td>
<td>9</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal3)</td>
<td>40</td>
<td>15</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal4)</td>
<td>37</td>
<td>14</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal5)</td>
<td>36</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1003</td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (r well)</td>
<td>987</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (d well)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>574</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (no well)</td>
<td>139</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Fringe (substrate)</td>
<td>244</td>
<td>201</td>
<td>18</td>
<td>61</td>
<td>55</td>
<td>43</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (poly)</td>
<td>69</td>
<td>39</td>
<td>24</td>
<td>21</td>
<td>19</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal1)</td>
<td>61</td>
<td>35</td>
<td>23</td>
<td>21</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal2)</td>
<td>54</td>
<td>37</td>
<td>27</td>
<td>24</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal3)</td>
<td>56</td>
<td>34</td>
<td>31</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal4)</td>
<td>58</td>
<td>40</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal5)</td>
<td>61</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Overlap (P+active)</td>
<td>652</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
</tbody>
</table>
T4BK SPICE BSIM3 VERSION 3.1 PARAMETERS

SPICE 3f5 Level 8, Star-HSPICE Level 49, UTMOST Level 8

* DATE: Jan 21/05
* LOT: T4BK
* WAF: 3004

* Temperature parameters=Default

.MODEL CMOS NNMOS 
.VERSION = 3.1  
TNOM = 27  
TOX = 4E-9
+XJ = 1E-7  
NCH = 2.3549E17  
VTH0 = 0.3662648
+K1 = 0.5802748  
K2 = 3.124029E-3  
K3 = 1E-3
+K3B = 3.3886871  
W0 = 1E-7  
NLX = 1.766159E-7
+DVT0W = 0  
DVT1W = 0  
DVT2W = 0
+DVT0 = 1.2312416  
DVT1 = 0.3849841  
DVT2 = 0.0161351
+U0 = 265.1889031  
UA = -1.506402E-9  
UB = 2.489393E-18
+UC = 5.621884E-11  
VSAT = 1.017932E5  
A0 = 2
+AGS = 0.4543117  
B0 = 3.433489E-7  
B1 = 5E-6
+KETA = -0.0127714  
A1 = 1.158074E-3  
A2 = 1
+RDSW = 136.5582806  
PRWG = 0.5  
PRWB = -0.2
+WR = 1  
WINT = 0  
LINT = 1.702415E-8
+XL = 0  
XW = -1E-8  
DWG = -4.211574E-9
+DWB = 1.107719E-8  
VOFF = -0.0948017  
NFACTOR = 2.1860065
+BIT = 0  
COSC = 2.4E-4  
CDSDC = 0
+CDSCB = 0  
ETA0 = 3.355516E-3  
ETAB = 6.028975E-5
+DSUB = 0.0214781  
PCLM = 0.6602119  
PDIBLC1 = 0.1605325
+PDIBLC2 = 3.287142E-3  
PDSIBLCB = -0.1  
DROUT = 0.7917811
+PSCBE1 = 6.420235E9  
PSCBE2 = 4.122516E-9  
PVAG = 0.0347169
+DELTAp = 0.01  
RSH = 6.6  
MOBMOD = 1
+PRT = 0  
UTE = -1.5  
KT1 = -0.11
+KTL = 0  
KT2 = 0.022  
UA1 = 4.31E-9
+UB1 = -7.61E-18  
UC1 = -5.6E-11  
AT = 3.3E4
+WIL = 0  
WLN = 1  
WW = 0
+WNN = 1  
WML = 0  
LL = 0
+LLN = 1  
LW = 0  
LWN = 1
+LWL = 0  
CAPMOD = 2  
XPART = 0.5
+CGD = 8.06E-10  
CGSO = 8.06E-10  
CGBO = 1E-12
+CJ = 9.895609E-4  
PB = 0.8  
MJ = 0.3736889
+CJSW = 2.393608E-10  
PBSW = 0.8  
MJSW = 0.1537892
+CJSWG = 3.3E-10  
PBSWG = 0.8  
MJSGW = 0.1537892
+CF = 0  
PVTH0 = -1.73163E-3  
PRDSW = -1.4173554
+PK2 = 1.600729E-3  
WKETA = 1.601517E-3  
LKETA = -3.255127E-3
+PU0 = 5.2024473  
PUA = 1.584315E-12  
PUB = 7.446142E-25
+PVSAT = 1.686297E3  
PETA0 = 1.001594E-4  
PKETA = -2.039532E-3 )
.MODEL CMOS PMOS (LEVEL = 49)
+VERSION = 3.1
+XJ = 1E-7
+K1 = 0.5895473
+K3B = 13.8642028
+DVT0 = 0
+U0 = 103.0478426
+UC = -1E-10
+AGS = 0.3295499
+KETA = 0.0296157
+RDSW = 306.5789827
+WR = 1
+XL = 0
+DWB = -9.34648E-11
+CIT = 0
+CDSCB = 0
+DSUB = 1.094521E-3
+PDIBLC2 = -3.255915E-6
+PSCBE1 = 4.881933E10
+DELT A = 0.01
+PRT = 0
+KT1L = 0
+UB1 = -7.61E-18
+WLN = 0
+WLN = 1
+LLN = 1
+LWL = 0
+CGD0 = 6.52E-10
+CJ = 1.157423E-3
+CJSW = 1.902456E-10
+CJSWG = 4.22E-10
+CF = 0
+PK2 = 2.190431E-3
+PU0 = -0.9769623
+PVSAT = -50
LEVEL = 49
TOX = 4E-9
NCH = 4.1589E17
VTH0 = -0.3708038
K2 = 0.0235946
W0 = 1E-6
NLX = 1.517201E-7
DVT1W = 0
DVT2 = 0.1
UA = 1.049312E-9
VSAT = 1.645114E5
B0 = 5.207699E-7
A1 = 0.4449009
UB = 2.545758E-21
VTH0 = -0.3708038
A0 = 1.627879
B1 = 1.370868E-6
A2 = 0.3
PRW = 0.5
LINT = 2.761033E-8
VOFF = -0.0867009
CDSC = 2.4E-4
ETA = 1.018318E-3
NFACTOR = 2
CDSCD = 0
ETA0 = -3.206319E-4
PDIBLC1 = 2.394169E-3
DROU T = 0
PSCBE2 = 5E-10
PVAG = 2.0932623
RSH = 7.5
MODMOD = 1
UTE = -1.5
KT1 = -0.11
KT2 = 0.022
UA1 = 4.31E-9
UC1 = -5.6E-11
AT = 3.3E4
WLN = 1
WWL = 0
LL = 0
LWN = 1
CAPMOD = 2
XPART = 0.5
CGSO = 6.52E-10
PB = 0.8444261
PJ = 0.4063933
PBSW = 0.8
MJSW = 0.3550788
PBSWG = 0.8
MJSWG = 0.3550788
PVTH0 = 1.4398E-3
PRDSW = 0.5073407
WKETA = 0.0442978
LKETA = -2.936093E-3
PUA = -4.34529E-11
PUB = 1E-21
PETA0 = 1.002762E-4
PKETA = -6.740436E-3 )

*
Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6\(\mu\) wide and 800\(\mu\) long and compare that with the same interconnect if \(M_1\) were used. Consider both 0.5\(\mu\) and 0.18\(\mu\) processes.

\[
R_{\text{POLY}} = n_{\text{SQ}} R_{\text{SH}}
\]

\[
C_{\text{P-SUB}} = A \cdot C_{\text{DPS}}
\]

\[
R_{\text{SH}} = ?
\]

\[
C_{\text{DPS}} = ?
\]
For 0.5\(\mu\) process

\[
R_{SH} = 23.5 \Omega/\square
\]

\[
C_{DPS} = 84 \text{ aF}/\mu^2
\]

<table>
<thead>
<tr>
<th>FOX TRANSISTORS</th>
<th>GATE</th>
<th>N+ACTIVE</th>
<th>P+ACTIVE</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vth</td>
<td>Poly</td>
<td>&gt;15.0</td>
<td>&lt;-15.0</td>
<td>volts</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2 HR</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>83.5</td>
<td>105.3</td>
<td>23.5</td>
<td>999</td>
<td>44.2</td>
<td>0.09</td>
<td>0.10</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>64.9</td>
<td>149.7</td>
<td>17.3</td>
<td>29.2</td>
<td>0.97</td>
<td></td>
<td></td>
<td>ohms</td>
</tr>
<tr>
<td>Gate Oxide Thickness</td>
<td>142</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>angstrom</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>M3</th>
<th>N(\backslash)PLY</th>
<th>N_W</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>0.05</td>
<td>824</td>
<td>816</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>0.79</td>
<td></td>
<td></td>
<td>ohms</td>
</tr>
</tbody>
</table>

**COMMENTS:** N\(\backslash\)POLY is N-well under polysilicon.

<table>
<thead>
<tr>
<th>CAPACITANCE PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>N_W</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (substrate)</td>
<td>425</td>
<td>731</td>
<td>84</td>
<td>27</td>
<td>12</td>
<td>7</td>
<td>37</td>
<td></td>
<td>aF/\mu m^2</td>
</tr>
<tr>
<td>Area (N+active)</td>
<td>2434</td>
<td></td>
<td>35</td>
<td>16</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
<td>aF/\mu m^2</td>
</tr>
<tr>
<td>Area (P+active)</td>
<td>2335</td>
<td></td>
<td></td>
<td>938</td>
<td>56</td>
<td>15</td>
<td>9</td>
<td></td>
<td>aF/\mu m^2</td>
</tr>
<tr>
<td>Area (poly)</td>
<td>49</td>
<td></td>
<td>938</td>
<td>56</td>
<td>15</td>
<td>9</td>
<td></td>
<td></td>
<td>aF/\mu m^2</td>
</tr>
<tr>
<td>Area (poly2)</td>
<td>31</td>
<td></td>
<td>56</td>
<td>56</td>
<td>15</td>
<td>9</td>
<td></td>
<td></td>
<td>aF/\mu m^2</td>
</tr>
<tr>
<td>Area (metal1)</td>
<td>35</td>
<td></td>
<td></td>
<td>31</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td>aF/\mu m^2</td>
</tr>
<tr>
<td>Area (metal2)</td>
<td></td>
<td></td>
<td></td>
<td>35</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/\mu m^2</td>
</tr>
<tr>
<td>Fringe (substrate)</td>
<td>344</td>
<td>238</td>
<td></td>
<td>49</td>
<td>33</td>
<td>23</td>
<td></td>
<td></td>
<td>aF/\mu m</td>
</tr>
<tr>
<td>Fringe (poly)</td>
<td>59</td>
<td>38</td>
<td>56</td>
<td>59</td>
<td>38</td>
<td>28</td>
<td></td>
<td></td>
<td>aF/\mu m</td>
</tr>
<tr>
<td>Fringe (metal1)</td>
<td>51</td>
<td>34</td>
<td>56</td>
<td>51</td>
<td>34</td>
<td>28</td>
<td></td>
<td></td>
<td>aF/\mu m</td>
</tr>
<tr>
<td>Fringe (metal2)</td>
<td></td>
<td>52</td>
<td></td>
<td>51</td>
<td>34</td>
<td>28</td>
<td></td>
<td></td>
<td>aF/\mu m</td>
</tr>
<tr>
<td>Overlap (N+active)</td>
<td>232</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/\mu m</td>
</tr>
<tr>
<td>Overlap (P+active)</td>
<td>312</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/\mu m</td>
</tr>
</tbody>
</table>

**CIRCUIT PARAMETERS**  

<table>
<thead>
<tr>
<th>Inverters</th>
<th>K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vinv</td>
<td>1.0</td>
</tr>
<tr>
<td>Vinv</td>
<td>1.5</td>
</tr>
<tr>
<td>Vol (100 uA)</td>
<td>2.0</td>
</tr>
</tbody>
</table>
Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6\(\mu\) wide and 800\(\mu\) long and compare that with the same interconnect if \(M_1\) were used.

\[ n_{sq} = \frac{800\mu}{0.6\mu} = 1333 \]

\[ A = (0.6\mu)(800\mu) = 480\mu^2 \]

\[ R_{POLY} = n_{sq} R_{SH} = 23.5 \cdot 1333 = 31.3\, K\Omega \]

\[ C_{P-SUB} = A \cdot C_{DPS} = 480\mu^2 \cdot 84aF\mu^{-2} = 40.3fF \]
For 0.18μ process

<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>N+BLK</th>
<th>PLY+BLK</th>
<th>M1</th>
<th>M2</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>6.6</td>
<td>7.5</td>
<td><strong>7.7</strong></td>
<td>61.0</td>
<td>317.1</td>
<td>0.08</td>
<td>0.08</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>10.1</td>
<td>10.6</td>
<td>9.3</td>
<td></td>
<td></td>
<td>4.18</td>
<td>ohms</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>M3</th>
<th>POLY_HRI</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
<th>N_W</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>0.08</td>
<td>991.5</td>
<td>0.08</td>
<td>0.08</td>
<td>0.01</td>
<td>941</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>8.97</td>
<td>14.09</td>
<td>18.84</td>
<td>21.44</td>
<td></td>
<td></td>
<td>ohms</td>
</tr>
</tbody>
</table>

COMMENTS: BLK is silicide block.

<table>
<thead>
<tr>
<th>CAPACITANCE PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
<th>R_W</th>
<th>D_N_W</th>
<th>M5P</th>
<th>N_W</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (substrate)</td>
<td>998</td>
<td>1152</td>
<td><strong>103</strong></td>
<td>39</td>
<td>19</td>
<td>13</td>
<td>9</td>
<td>8</td>
<td>3</td>
<td>129</td>
<td>127</td>
<td>aF/um^2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Area (N+active)</td>
<td>8566</td>
<td>54</td>
<td>21</td>
<td>14</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Area (P+active)</td>
<td>8324</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (poly)</td>
<td>64</td>
<td>18</td>
<td>10</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (metal1)</td>
<td>44</td>
<td>16</td>
<td>10</td>
<td>7</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (metal2)</td>
<td>38</td>
<td>15</td>
<td>9</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (metal3)</td>
<td>40</td>
<td>15</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (metal4)</td>
<td>37</td>
<td>14</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (metal5)</td>
<td>36</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1003</td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (r well)</td>
<td>987</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (d well)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>574</td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (no well)</td>
<td>139</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Fringe (substrate)</td>
<td>244</td>
<td>201</td>
<td>18</td>
<td>61</td>
<td>55</td>
<td>43</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Fringe (poly)</td>
<td>69</td>
<td>39</td>
<td>29</td>
<td>24</td>
<td>21</td>
<td>19</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Fringe (metal1)</td>
<td>61</td>
<td>35</td>
<td>23</td>
<td>21</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Fringe (metal2)</td>
<td>54</td>
<td>37</td>
<td>27</td>
<td>24</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Fringe (metal3)</td>
<td>56</td>
<td>34</td>
<td>31</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Fringe (metal4)</td>
<td>58</td>
<td>40</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Fringe (metal5)</td>
<td>61</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Overlap (P+active)</td>
<td>652</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
</tbody>
</table>

\[ R_{SH} = 7.7\Omega/\square \]

\[ C_{DPS} = 103 \text{ aF/μm}^2 \]
Determine the resistance and capacitance of a Poly interconnect that is 0.6\(\mu\) wide and 800\(\mu\) long and compare that with the same interconnect if \(M_1\) were used.

\[
n_{SQ} = \frac{800\mu}{0.6\mu} = 1333
\]

\[
A = (0.6\mu)(800\mu) = 480\mu^2
\]

\[
R_{POLY} = n_{SQ} R_{SH} = 7.7 \cdot 1333 = 10.3K\Omega
\]

\[
C_{P-SUB} = A \cdot C_{DPS} = 480\mu^2 \cdot 103aF\mu^{-2} = 49.4fF
\]
Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6µ wide and 800µ long and compare that with the same interconnect if $M_1$ were used. Do this for both a 0.5µ and a 0.18µ process.
For 0.5μ process

<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2 HR</th>
<th>POLY2 M1</th>
<th>M2</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>83.5</td>
<td>105.3</td>
<td>23.5</td>
<td>999</td>
<td>44.2</td>
<td>0.09</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>64.9</td>
<td>149.7</td>
<td>17.3</td>
<td>29.2</td>
<td>0.97</td>
<td></td>
<td>ohms</td>
</tr>
<tr>
<td>Gate Oxide Thickness</td>
<td>142</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>angstrom</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>M3</th>
<th>N\PLY</th>
<th>N_W</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>0.05</td>
<td>824</td>
<td>816</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>0.79</td>
<td></td>
<td></td>
<td>ohms</td>
</tr>
</tbody>
</table>

**Comments:** N\PLY is N-well under polysilicon.

<table>
<thead>
<tr>
<th>CAPACITANCE PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>N_W</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (substrate)</td>
<td>425</td>
<td>731</td>
<td>84</td>
<td></td>
<td>27</td>
<td>12</td>
<td>7</td>
<td>37</td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (N+active)</td>
<td>2434</td>
<td></td>
<td>35</td>
<td>16</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (P+active)</td>
<td>2335</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (poly)</td>
<td>938</td>
<td>56</td>
<td>15</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (poly2)</td>
<td>49</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal1)</td>
<td>31</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Area (metal2)</td>
<td>35</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
</tr>
<tr>
<td>Fringe (substrate)</td>
<td>344</td>
<td>238</td>
<td>49</td>
<td>33</td>
<td>23</td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (poly)</td>
<td>59</td>
<td>38</td>
<td>28</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal1)</td>
<td>51</td>
<td>34</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Fringe (metal2)</td>
<td>52</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Overlap (N+active)</td>
<td>232</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
<tr>
<td>Overlap (P+active)</td>
<td>312</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
</tr>
</tbody>
</table>

**Circuit Parameters**

<table>
<thead>
<tr>
<th>Inverters</th>
<th>K</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vinv</td>
<td>1.0</td>
</tr>
<tr>
<td>Vinv</td>
<td>1.5</td>
</tr>
<tr>
<td>Vol (100 uA)</td>
<td>2.0</td>
</tr>
</tbody>
</table>
Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6µ wide and 800µ long and compare that with the same interconnect if M₁ were used.

\[ n_{sq} = \frac{800\mu}{0.6\mu} = 1333 \]

\[ A = (0.6\mu)(800\mu) = 480\mu^2 \]

\[ R_{M1} = n_{sq} R_{SH} = 0.09 \cdot 1333 = 120\Omega \]

\[ C_{M1-SUB} = A \cdot C_{DM1S} = 480\mu^2 \cdot 27aF\mu^{-2} = 13.0fF \]
For 0.18\mu process

<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>N+BLK</th>
<th>PLY+BLK</th>
<th>M1</th>
<th>M2</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>6.6</td>
<td>7.5</td>
<td>7.7</td>
<td>61.0</td>
<td>317.1</td>
<td>0.08</td>
<td>0.08</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>10.1</td>
<td>10.6</td>
<td>9.3</td>
<td></td>
<td></td>
<td>4.18</td>
<td></td>
<td>ohms</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>PROCESS PARAMETERS</th>
<th>M3</th>
<th>POLY_HRI</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
<th>N_W</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>0.08</td>
<td>991.5</td>
<td>0.08</td>
<td>0.08</td>
<td>0.01</td>
<td>941</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>8.97</td>
<td>14.09</td>
<td>18.84</td>
<td>21.44</td>
<td></td>
<td></td>
<td>ohms</td>
</tr>
</tbody>
</table>

COMMENTS: BLK is silicide block.

<table>
<thead>
<tr>
<th>CAPACITANCE PARAMETERS</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>M4</th>
<th>M5</th>
<th>M6</th>
<th>R_W</th>
<th>D_N_W</th>
<th>M5P</th>
<th>N_W</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (substrate)</td>
<td>998</td>
<td>1152</td>
<td>103</td>
<td>39</td>
<td>19</td>
<td>13</td>
<td>9</td>
<td>8</td>
<td>3</td>
<td>129</td>
<td>127</td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (N+active)</td>
<td>8566</td>
<td>54</td>
<td>21</td>
<td>14</td>
<td>11</td>
<td>10</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (P+active)</td>
<td>8324</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (poly)</td>
<td>64</td>
<td>18</td>
<td>10</td>
<td>7</td>
<td>6</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (metal1)</td>
<td>44</td>
<td>16</td>
<td>10</td>
<td>7</td>
<td>5</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (metal2)</td>
<td>38</td>
<td>15</td>
<td>9</td>
<td>7</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (metal3)</td>
<td>40</td>
<td>15</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (metal4)</td>
<td>37</td>
<td>14</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (metal5)</td>
<td>36</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1003</td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (r well)</td>
<td>987</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (d well)</td>
<td></td>
<td>574</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Area (no well)</td>
<td>139</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um^2</td>
<td></td>
</tr>
<tr>
<td>Fringe (substrate)</td>
<td>244</td>
<td>201</td>
<td>18</td>
<td>61</td>
<td>55</td>
<td>43</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Fringe (poly)</td>
<td>69</td>
<td>39</td>
<td>29</td>
<td>24</td>
<td>21</td>
<td>19</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Fringe (metal1)</td>
<td>61</td>
<td>35</td>
<td>23</td>
<td>21</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Fringe (metal2)</td>
<td>54</td>
<td>37</td>
<td>27</td>
<td>24</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Fringe (metal3)</td>
<td>56</td>
<td>34</td>
<td>31</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Fringe (metal4)</td>
<td>58</td>
<td>40</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Fringe (metal5)</td>
<td>61</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
<tr>
<td>Overlap (P+active)</td>
<td>652</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/um</td>
<td></td>
</tr>
</tbody>
</table>

\( R_{SH} = 0.08 \Omega/\square \)

\( C_{DPS} = 39 \text{ aF/}\mu^2 \)
Example

Determine the resistance and capacitance of a Poly interconnect that is 0.6\( \mu \) wide and 800\( \mu \) long and compare that with the same interconnect if M\(_1\) were used.

For 0.18\( \mu \) process

\[ n_{sq} = \frac{800\mu}{0.6\mu} = 1333 \]

\[ A = (0.6\mu)(800\mu) = 480\mu^2 \]

\[ R_{M1} = n_{SQ} R_{SH} = 0.08 \cdot 1333 = 107\Omega \]

\[ C_{M1-SUB} = A \cdot C_{DM1S} = 480\mu^2 \cdot 39aF\mu^{-2} = 18.7fF \]
Example

Compare the resistance and capacitance of a n+ diffusion interconnect that is 0.6μ wide and 800μ long with what would be obtained with a Poly and a M1 interconnect. Assume a 0.5μ process.

\[ R_{Diff} = n_{SQ} R_{SH} \]

\[ C_{Diff-SUB} = A \cdot C_{D\_Diff-SUB} \]

\[ R_{SH} = ? \]

\[ C_{D\_Diff-SUB} = ? \]
**For 0.5μ process**

### Process Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2 HR</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sheet Resistance</td>
<td>83.5</td>
<td>105.3</td>
<td>23.5</td>
<td>999</td>
<td>44.2</td>
<td>0.09</td>
<td>0.10</td>
<td>ohms/sq</td>
</tr>
<tr>
<td>Contact Resistance</td>
<td>64.9</td>
<td>149.7</td>
<td>17.3</td>
<td></td>
<td>29.2</td>
<td>0.97</td>
<td></td>
<td>ohms</td>
</tr>
<tr>
<td>Gate Oxide Thickness</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>angstrom</td>
</tr>
</tbody>
</table>

### Capacitance Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>N+</th>
<th>P+</th>
<th>POLY</th>
<th>POLY2</th>
<th>M1</th>
<th>M2</th>
<th>M3</th>
<th>N_W</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area (substrate)</td>
<td>425</td>
<td>731</td>
<td>84</td>
<td></td>
<td>27</td>
<td>12</td>
<td>7</td>
<td>37</td>
<td>aF/μm^2</td>
</tr>
<tr>
<td>Area (N+active)</td>
<td>2434</td>
<td>35</td>
<td>16</td>
<td>11</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/μm^2</td>
</tr>
<tr>
<td>Area (P+active)</td>
<td>2335</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/μm^2</td>
</tr>
<tr>
<td>Area (poly)</td>
<td>938</td>
<td>56</td>
<td>15</td>
<td>9</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/μm^2</td>
</tr>
<tr>
<td>Area (poly2)</td>
<td>49</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/μm^2</td>
</tr>
<tr>
<td>Area (metal1)</td>
<td>31</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/μm^2</td>
</tr>
<tr>
<td>Area (metal2)</td>
<td>35</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/μm^2</td>
</tr>
<tr>
<td>Fringe (substrate)</td>
<td>344</td>
<td>238</td>
<td>49</td>
<td>33</td>
<td>23</td>
<td></td>
<td></td>
<td></td>
<td>aF/μm</td>
</tr>
<tr>
<td>Fringe (poly)</td>
<td>59</td>
<td>38</td>
<td>28</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/μm</td>
</tr>
<tr>
<td>Fringe (metal1)</td>
<td>51</td>
<td>34</td>
<td>34</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/μm</td>
</tr>
<tr>
<td>Fringe (metal2)</td>
<td>52</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/μm</td>
</tr>
<tr>
<td>Overlap (N+active)</td>
<td>232</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/μm</td>
</tr>
<tr>
<td>Overlap (P+active)</td>
<td>312</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>aF/μm</td>
</tr>
</tbody>
</table>

### Circuit Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>K</th>
<th>Vol (100 uA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Inverters</td>
<td>1.0</td>
<td>2.02 volts</td>
</tr>
<tr>
<td>Vinv</td>
<td>1.5</td>
<td>2.28 volts</td>
</tr>
<tr>
<td>Vol (100 uA)</td>
<td>2.0</td>
<td>0.13 volts</td>
</tr>
</tbody>
</table>

**R_{SH}=83.5\,\Omega/☐**

**C_{DPS}=425\,\text{af}/\mu^2**
Example

Compare the resistance and capacitance of a n+ diffusion interconnect that is 0.6\(\mu\) wide and 800\(\mu\) long with what would be obtained with a Poly and a M\(_1\) interconnect. Assume a 0.5\(\mu\) process.

\[ n_{SQ} = \frac{800\mu}{0.6\mu} = 1333 \]

\[ A = (0.6\mu)(800\mu) = 480\mu^2 \]

\[ R_{n+}^{\text{SQ SH}} = 83.5 \cdot 1333 = 111K\Omega \]

\[ C_{n+\text{-SUB}} = A \cdot C_{Dn+S} = 480\mu^2 \cdot 425aF\mu^{-2} = 204fF \]
Stay Safe and Stay Healthy!
End of Lecture 11