Devices in Semiconductor Processes

- Diodes
Guest Lecture:

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NAND Memory: Operation, Testing and Challenges
Agenda

- Types of Memory
- Flash Memory Cells
- Program, Erase, Read Operations
- 2D to 3D NAND
- Basic Device Physics
- Technical Issues with 3D NAND

September 23, 2016
Micron’s Core Memory Technologies

Types of Semiconductor Memory

- **Volatile**
  - DRAM

- **Non-Volatile**
  - NAND Flash
  - NOR Flash

Volatile – loses data when power is removed (within milliseconds)
Non-volatile – retains data when power is removed (for years)
# Leading-Edge Technology Status

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Images are not to scale

September 23, 2016
Flash Memory Cell

- Single FET with dual gate
- Electrically isolated **floating gate** is the storage element
- Electrons added to or removed from the floating gate shift the $V_t$ of the cell to store a 1 or a 0
- Two types: NAND and NOR
  - NAND – Better array efficiency, lower cost per die for mass-storage
  - NOR – Faster read/write speeds for code storage and execution
NAND vs NOR – Physical Comparison

NAND
Serial layout

NOR
Parallel layout
Basic NAND Flash Operation

• The operation of the NAND Flash cell depends on two basic electrical concepts:
  – Capacitive division
  – Fowler-Nordheim tunneling
Capacitive Division

- If you have capacitors in series, a voltage applied to one node will be distributed across the intermediate nodes
  \[ V_2 = V_1 \times \frac{C_1}{C_1 + C_2} \]

Diagram:
- \( C_1 = 4 \text{pF} \) and \( C_2 = 1 \text{pF} \)
- \( V_1 = 10 \text{V} \) and \( V_2 = 8 \text{V} \)
Fowler-Nordheim Tunneling

- By setting up a large potential difference across an insulator, you can decrease the effective width of the energy barrier, and increase the probability that an electron will tunnel through the insulator.
NAND Flash Operation – Program

• Store a 0 to a cell
  – Inject electrons onto floating gate through F-N tunneling
NAND Flash Operation – Erase

• Store a 1 to a cell
  – Remove electrons from the floating gate through F-N tunneling
NAND Flash Operation – Read

- By storing electrons on the floating gate, we can change the effective threshold voltage ($V_T$)
- FET conducts current if $V_{GS} > V_T$

- To read the cell, apply a voltage ($V_{Read}$) to the rowline
  - $(V_T < V_{Read}) \Rightarrow$ Current, logic ‘1’
  - $(V_T > V_{Read}) \Rightarrow$ No current, logic ‘0’
NAND Read Operation

1. Precharge bitline and unselected wordlines
2. Drive selected wordline and connect string to bitline
3. Sense current
Vt Distributions

- **Single-Level Cell (SLC)**
  - ‘1’
  - ‘0’

- **Multi-Level Cell (MLC)**
  - ‘11’
  - ‘10’
  - ‘01’
  - ‘00’

Can be extended further to 3 bits per cell (TLC) with 8 distinct states.
The NAND String

- Notice that it has n doping on the source and drain that is repeated across a horizontal plane.
Moving to 3D NAND – Change to the Channel

- Elimination of Pwell/Atub
- Loss of LDD (Lightly Doped Drain) – Pillar
- Vertical Stacking of Cell’s
- Device Physics Change

1. With n-LDD (2D)
2. No LDD, P-type channel
3. No LDD, N-type thin channel
How does the Channel Conduct with No LDD?

With All E fields the channel can be formed in the pillar and thus conduct effectively.

Fringe Fields allow for E Field to activate area between cells.
Challenges with the Channel – Erase Verify Example

Fringe Fields are too weak to create a channel in the space between Cells. AKA, my Space Vt is too high to activate with 1V.

The result is a non-conductive channel even though my Vt’s of my cell’s are lower than the Gate Voltage.
What goes into designing a Flash memory chip?

• Core memory array

Lots of other circuitry:

  ▪ Sense amplifiers and digital registers to read and store the contents of the memory array

  ▪ Command and address decoders to select which location to read/write, and which operation to perform

  ▪ Bandgap reference to generate a voltage reference that is stable across temperature and supply voltage

  ▪ Charge pumps to generate voltages above or below the supply voltages for the chip

  ▪ Voltage regulators to regulate the precise voltages required to read/write the array

  ▪ Thermometer to adjust voltages as needed vs. temperature

  ▪ DACs and ADCs for converting internal signals between analog and digital domains

  ▪ Current sources/mirrors to be used for providing reference currents to key circuits throughout the chip

  ▪ Microcontroller and digital control logic to control the read/write algorithms for the array

  ▪ I/O drivers for communicating with the outside world

  ▪ High speed datapath for sending data back and forth between the Chip I/Os and memory array
Questions?
## Periodic Table of the Elements

![Periodic Table](http://www.dayah.com/periodic/Images/periodic%20table.png)
Review from Last Lecture

Boron (B): 1s^2 2s^2 2p^1

Silicon (Si): [Ne]3s^2 3p^2

Phosphorus (P): 2s^2 2p^3

Arsenic (As): [Ar]3d^{10} 4s^2 4p^3

Antimony (Sb): [Kr]4d^{10} 5s^2 5p^3
Review from Last Lecture

Silicon Dopants in Semiconductor Processes

**B** (Boron) widely used a dopant for creating p-type regions

**P** (Phosphorus) widely used a dopant for creating n-type regions  
(bulk doping, diffuses fast)

**As** (Arsenic) widely used a dopant for creating n-type regions  
(Active region doping, diffuses slower)
Diodes (pn junctions)

Depletion region created that is ionized but void of carriers
pn Junctions

If doping levels identical, depletion region extends equally into n-type and p-type regions.
**pn Junctions**

Extends farther into p-type region if p-doping lower than n-doping

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Physical Boundary
Separating n-type and p-type regions
pn Junctions

Physical Boundary Separating n-type and p-type regions

Extends farther into n-type region if n-doping lower than p-doping
• Positive voltages across the p to n junction are referred to forward bias
• Negative voltages across the p to n junction are referred to reverse bias
• As forward bias increases, depletion region thins and current starts to flow
• Current grows very rapidly as forward bias increases
• Current is very small under reverse bias
pn Junctions

Anode

Cathode

Circuit Symbol

$V_D$

$I_D$

Anode

Cathode

Circuit Symbol
pn Junctions

- As forward bias increases, depletion region thins and current starts to flow
- Current grows very rapidly as forward bias increases

Simple Diode Model:

- $V_D = 0$, $I_D > 0$
- $V_D < 0$, $I_D = 0$

Simple model often referred to as the “Ideal” diode model
pn junction serves as a rectifier passing current in one direction and blocking it in the other direction.
Rectifier Application:

\[ V_{IN} = V_M \sin(\omega t) \]

Simple Diode Model:
I-V characteristics of pn junction
(signal or rectifier diode)

Improved Diode Model:

![Diode schematic]

Diode Equation

\[ I_D = I_S \left( e^{\frac{V_d}{V_t}} - 1 \right) \]

What is \( V_t \) at room temp?

\( V_t \) is about 26mV at room temp

\[ I_S \text{ in the 10fA to 100fA range} \]

\[ V_t = \frac{kT}{q} \]

\[ k = 1.3806504(24) \times 10^{-23} \text{JK}^{-1} \]

\[ q = -1.602176487(40) \times 10^{-19} \text{C} \]

\[ \frac{k}{q} = 8.62 \times 10^{-5} \text{VK}^{-1} \]

Diode equation due to William Schockley, inventor of BJT

In 1919, William Henry Eccles coined the term \textit{diode}

In 1940, Russell Ohl “stumbled upon” the p-n junction diode
I-V characteristics of pn junction
(signal or rectifier diode)

Improved Diode Model:

\[ I_D = I_S \left( e^{\frac{V_d}{V_t}} - 1 \right) \]

**Diode Equation**

**Simplification of Diode Equation:**

- **Under reverse bias** \((V_d<0)\), \(I_D \approx -I_S \frac{V_d}{V_t}\)
- **Under forward bias** \((V_d>0)\), \(I_D = I_S e^{\frac{V_d}{V_t}}\)

**Diode Equation or forward bias simplification** is unwieldy to work with analytically

**I_S** in the 10fA to 100fA range

\[ V_t = \frac{kT}{q} \]

- \(k= 1.3806504(24) \times 10^{-23} \text{JK}^{-1}\)
- \(q = -1.602176487(40) \times 10^{-19} \text{C}\)
- \(k/q=8.62 \times 10^{-5} \text{VK}^{-1}\)

\(V_t\) is about 26mV at room temp

Simplification essentially identical model except for \(V_d\) very close to 0
I-V characteristics of pn junction
(signal or rectifier diode)

Improved Diode Model:

Diode Equation

\[ I_D = I_S \left( e^{\frac{V_d}{V_t}} - 1 \right) \]

\( I_S \) often in the 10fA to 100fA range
\( I_S \) proportional to junction area

V\(_t\) is about 26mV at room temp

Simplification of Diode Equation:

Under reverse bias,

\[ I_D \approx -I_S \frac{V_d}{V_t} \]

Under forward bias,

\[ I_D = I_S e^{\frac{V_d}{V_t}} \]

How much error is introduced using the simplification for \( V_d > 0.5V \)?

\[ \varepsilon = \frac{I_S \left( e^{\frac{V_d}{V_t}} - 1 \right) - I_S e^{\frac{V_d}{V_t}}}{I_S \left( e^{\frac{V_d}{V_t}} - 1 \right)} \]

\[ \varepsilon < \frac{1}{e^{0.5}} = 4.4 \times 10^{-9} \]

How much error is introduced using the simplification for \( V_d < -0.5V \)?

\[ \varepsilon < e^{-0.5} e^{0.026} = 4.4 \times 10^{-9} \]

Simplification almost never introduces any significant error
Will you impress your colleagues or your boss if you use the more exact diode equation when \( V_d < -0.5V \) or \( V_d > +0.5V \)?

Will your colleagues or your boss be unimpressed if you use the more exact diode equation when \( V_d < -0.5V \) or \( V_d > +0.5V \)?
**Diode Equation:**

(good enough for most applications)

\[
I = \begin{cases} 
J_S A e^{\frac{V}{n V_T}} & \text{if } V > 0 \\
0 & \text{if } V < 0 
\end{cases}
\]

Note: \( I_S = J_S A \)

- **\( J_S \)** = Sat Current Density (in the 1aA/u^2 to 1fA/u^2 range)
- **\( A \)** = Junction Cross Section Area
- **\( V_T \)** = \( kT/q \)  \( (k/q=1.381 \times 10^{-23} \text{V} \cdot \text{C}/\text{°K}/1.6\times10^{-19} \text{C}=8.62\times10^{-5} \text{V}/\text{°K}) \)
- \( n \) is approximately 1
pn Junctions

Diode Equation:
\[ I = \begin{cases} J_S Ae^{\frac{V}{nV_T}} & V > 0 \\ 0 & V < 0 \end{cases} \]

\( J_S \) is strongly temperature dependent

With \( n=1 \), for \( V>0 \),

\[ I(T) = \left( J_{SX} \left[ T^m e^{\frac{-V_{G0}}{V_t}} \right] \right) \ Ae^{\frac{V_D}{V_t}} \]

Typical values for key parameters: \( J_{SX}=0.5A/\mu^2 \), \( V_{G0}=1.17V \), \( m=2.3 \)
pn Junctions

Example:

\[ I(T) = \left( J_{SX} \left[ T^m e^{\frac{-V_{ao}}{V_t}} \right] \right) Ae^\frac{V_D}{V_t} \]

What percent change in \( I_S \) will occur for a 1°C change in temperature at room temperature?

\[
\frac{\Delta I_S}{I_S} = \left( J_{SX} \left[ T^m_{T_2} e^{\frac{-V_{ao}}{V_{T_2}}} \right] \right) Ae^{\frac{V_2}{V_t}} \left( J_{SX} \left[ T^m_{T_1} e^{\frac{-V_{ao}}{V_{T_1}}} \right] \right) Ae^{\frac{-V_{ao}}{V_{T_1}}} - \left( J_{SX} \left[ T^m_{T_1} e^{\frac{-V_{ao}}{V_{T_1}}} \right] \right) Ae^{\frac{-V_{ao}}{V_{T_1}}} = \left( T^m_{T_2} e^{\frac{-V_{ao}}{V_{T_2}}} \right) - \left( T^m_{T_1} e^{\frac{-V_{ao}}{V_{T_1}}} \right)
\]

\[
\Delta I_S = \left( 1.240 \times 10^{-15} \right) - \left( 1.025 \times 10^{-15} \right) = 21\%
\]
End of Lecture 12