EE 330
Lecture 14

Devices in Semiconductor Processes

• MOSFETs
Use of Piecewise Models for Nonlinear Devices when Analyzing Electronic Circuits

Process:

1. Guess state of the device
2. Analyze circuit
3. Verify State
4. Repeat steps 1 to 3 if verification fails

Observations:

- Analysis generally simplified dramatically (particularly if piecewise model is linear)
- Approach applicable to wide variety of nonlinear devices
- Closed-form solutions give insight into performance of circuit
- Usually much faster than solving the nonlinear circuit directly
- Wrong guesses in the state of the device do not compromise solution (verification will fail)
- Helps to Guess Right the first time
Basic Devices and Device Models

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT
n-Channel MOSFET Operation and Model

Review from Last Lecture

Model in Cutoff Region

\[ I_D = 0 \]
\[ I_G = 0 \]
\[ I_B = 0 \]
Review from Last Lecture

**n-Channel MOSFET Operation and Model**

Critical value of $V_{GS}$ that creates inversion layer termed threshold voltage, $V_T$.

Increase $V_{GS}$ more

Inversion layer forms in channel

Inversion layer will support current flow from D to S

Channel behaves as thin-film resistor

$I_D R_{CH} = V_{DS}$

$I_G = 0$

$I_B = 0$
Triode Region of Operation

For $V_{DS}$ small

$$R_{CH} = \frac{L}{W} \frac{1}{(V_{GS} - V_T) \mu C_{OX}}$$

$$I_D = \mu C_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

$I_G = I_B = 0$

Behaves as a resistor between drain and source

Model in Deep Triode Region
For $V_{DS}$ small

$$R_{CH} = \frac{L}{W} \frac{1}{(V_{GS} - V_T)\mu C_{OX}}$$

Resistor is controlled by the voltage $V_{GS}$
Termed a “Voltage Controlled Resistor” (VCR)
n-Channel MOSFET Operation and Model

Increase $V_{GS}$ more

Inversion layer in channel thickens

$R_{CH}$ will decrease

Termed “ohmic” or “triode” region of operation

$I_D R_{CH} = V_{DS}$

$I_G = 0$

$I_B = 0$
n-Channel MOSFET Operation and Model

Increase $V_{DS}$

Inversion layer thins near drain

$I_D$ no longer linearly dependent upon $V_{DS}$

Still termed “ohmic” or “triode” region of operation

$I_D = \text{?}$

$I_G = 0$

$I_B = 0$
Triode Region of Operation

For $V_{DS}$ larger

$$R_{CH} = \frac{L}{W} \left( \frac{1}{V_{GS} - V_T} \right) \cdot \mu C_{OX}$$

$$I_D = \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}$$

$$I_G = I_B = 0$$

Model in Triode Region
n-Channel MOSFET Operation and Model

Increase $V_{DS}$ even more

Inversion layer disappears near drain

Termed “saturation” region of operation

Saturation first occurs when $V_{DS} = V_{GS} - V_T$

$I_D = \cdot$

$I_G = 0$

$I_B = 0$
Saturation Region of Operation

For $V_{DS}$ at onset of saturation

$I_D = \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}$

or equivalently

$I_D = \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{GS} - V_T}{2} \right) (V_{GS} - V_T)$

or equivalently

$I_D = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_T)^2$

$I_G = I_B = 0$
n-Channel MOSFET Operation and Model

Increase $V_{DS}$ even more (beyond $V_{GS} - V_T$)

Nothing much changes!!
Termed “saturation” region of operation

$I_D = ?$
$I_G = 0$
$I_B = 0$
Saturation Region of Operation

For $V_{DS}$ in Saturation

$$I_D = \frac{\mu C_{OX} W}{2L} (V_{GS} - V_T)^2$$

$I_G = I_B = 0$

Model in Saturation Region
Model Summary

\[ I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} < V_{GS} - V_T \\
\mu C_{OX} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T 
\end{cases} \]

\[ I_G = I_B = 0 \]

This is a piecewise model (not piecewise linear though)

Note: This is the third model we have introduced for the MOSFET

(Deep triode special case of triode where \( V_{DS} \) is small)

\[ R_{CH} = \frac{L}{W \left( V_{GS} - V_T \right) \mu C_{OX}} \]
Model Summary

\[ I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{OX} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases} \]

\[ I_G = I_B = 0 \]

Observations about this model (developed for \( V_{BS} = 0 \)):

\[ I_D = f_1 \left( V_{GS}, V_{DS} \right) \]

\[ I_G = f_2 \left( V_{GS}, V_{DS} \right) \]

\[ I_B = f_3 \left( V_{GS}, V_{DS} \right) \]

This is a nonlinear model characterized by the functions \( f_1, f_2, \) and \( f_3 \) where we have assumed that the port voltages \( V_{GS} \) and \( V_{DS} \) are the independent variables and the drain currents are the dependent variables.
General Nonlinear Model

\[ I_1 = f_1(V_1, V_2) \]
\[ I_2 = f_2(V_1, V_2) \]

\( I_1 \) and \( I_2 \) are 3-dimensional relationships which are often difficult to visualize.

Two-dimensional representation of 3-dimensional relationships
Graphical Representation of MOS Model

\[ I_D = \begin{cases} 
0 & \mu C_{ox} \frac{W}{L} 
\left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T \\
& V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T 
\end{cases} \]

\[ I_G = I_B = 0 \]
PMOS and NMOS Models

- Functional form identical, sign changes and parameter values different
- Will give details about p-channel model later
Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T=1V$ and $\mu C_{OX}=100\mu A V^{-2}$

Solution:

Since $V_{GS}>V_T$, $M_1$ is operating in either saturation or triode region

Strategy will be to guess region of operation, solve, and then verify region
Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T=1V$ and $\mu C_{OX}=100\mu AV^{-2}$

Solution:

Guess $M_1$ in saturation

\[
5V = I_D 10K + V_{OUT} \\
I_D = \frac{\mu C_{OX} W}{2L} (3-V_T)^2
\]

Required verification: $V_{DS} > V_{GS} - V_T$

Can eliminate $I_D$ between these 2 equations to obtain $V_{OUT}$
Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T=1\text{V}$ and $\mu C_{OX}=100\mu\text{AV}^{-2}$

Guess $M_1$ in saturation

\[
5V = I_D 10K + V_{OUT}
\]

\[
I_D = \frac{\mu C_{OX}W}{2L}(3-V_T)^2
\]

\[
V_{OUT} = 5V - 10K \left[ \frac{100\mu\text{AV}^{-2}210\mu}{2 \cdot 2\mu}(2\text{V})^2 \right]
\]

\[
V_{OUT} = 5V - 10K \left[ \frac{100\mu\text{AV}^{-2}210\mu}{2 \cdot 2\mu}(2\text{V})^2 \right]
\]

\[
V_{OUT} = -5V
\]

Verification: $V_{DS}=V_{OUT}$

-5 $>\ ?$ 2V - - 0 No! So verification fails and Guess of region is invalid
Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T=1V$ and $\mu C_{OX}=100\mu AV^{-2}$

Guess $M_1$ in triode

\[
5V = I_D 10K + V_{OUT}
\]

\[
I_D = \frac{\mu C_{OX} W}{L} \left( 3 - V_T - \frac{V_{DS}}{2} \right) V_{DS}
\]

\[
V_{OUT} = 5V - 10K \left[ \frac{100\mu AV^{-2} 2^{10} \mu}{2\mu} \left( 2V - \frac{V_{OUT}}{2} \right) V_{OUT} \right]
\]

Solving for $V_{OUT}$, obtain

\[
V_{OUT} = 0.515V
\]

Verification: $V_{DS} = V_{OUT}$

\[
0.515 < ? 2V \quad - \quad 0 \quad \text{Yes!}
\]

So verification succeeds and triode region is valid

\[
V_{OUT} = 0.515V
\]
Limitations of Existing Models

Logic Gate

Switch-Level Models

Simple square-law Model

Voltage Amplifier

Switch-Level Models

Simple square-law Model

Voltage Gain

Input/Output Relationship
Model Extensions

Projections intersect $-V_{DS}$ axis at same point, termed Early Voltage

Typical values from -20V to -200V

Usually use parameter $\lambda$ instead of $V_A$ in MOS model
Model Extensions

Existing Model

Slope is not 0

Actual Device
Model Extensions

\[ I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, \quad V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS}) & V_{GS} \geq V_T, \quad V_{DS} \geq V_{GS} - V_T 
\end{cases} \]

Note: This introduces small discontinuity (not shown) in model at SAT/Triode transition.
Further Model Extensions

Existing model does not depend upon the bulk voltage!

Observe that changing the bulk voltage will change the electric field in the channel region!
Further Model Extensions

Existing model does not depend upon the bulk voltage!

Observe that changing the bulk voltage will change the electric field in the channel region!

Changing the bulk voltage will change the thickness of the inversion layer
Changing the bulk voltage will change the threshold voltage of the device

\[
V_T = V_{T0} + \gamma \left( \sqrt{\phi} - V_{BS} - \sqrt{\phi} \right)
\]
Typical Effects of Bulk on Threshold Voltage for n-channel Device

\[ V_T = V_{T0} + \gamma \left( \sqrt{\phi} - V_{BS} - \sqrt{\phi} \right) \]

\[ \gamma \approx 0.4V^{1/2} \quad \phi \approx 0.6V \]

- Bulk-Diffusion Generally Reverse Biased \((V_{BS} < 0\) or at least less than 0.3V\)) for n-channel
- Shift in threshold voltage with bulk voltage can be substantial
- Often \(V_{BS}=0\)
Typical Effects of Bulk on Threshold Voltage for n-channel Device

\[ V_T = V_{T0} + \gamma \left( \sqrt{\phi} - V_{BS} - \sqrt{\phi} \right) \]

\[ \gamma \approx 0.4V^{\frac{1}{2}} \quad \phi \approx 0.6V \]

\[ \Delta V = \gamma \left( \sqrt{\phi} - V_{BS} - \sqrt{\phi} \right) \]

\[ \Delta V_T \approx 0.4 \left( \sqrt{0.6} - (-5) - \sqrt{0.6} \right) = 0.64V \]
Typical Effects of Bulk on Threshold Voltage for p-channel Device

\[ V_T = V_{T0} - \gamma \left( \sqrt{\phi + V_{BS}} - \sqrt{\phi} \right) \]

\[ \gamma \triangleq 0.4V^{\frac{1}{2}} \quad \phi \triangleq 0.6V \]

Bulk-Diffusion Generally Reverse Biased \((V_{BS} > 0\) or at least greater than \(-0.3V)\)

for n-channel

Same functional form as for n-channel devices but \(V_{T0}\) is now negative and the magnitude of \(V_T\) still increases with the magnitude of the reverse bias
Model Extension Summary

\[ I_G = 0 \]
\[ I_B = 0 \]

\[ I_d = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{OX} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 \cdot (1 + \lambda V_{DS}) & \text{if } V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases} \]

\[ V_T = V_{T0} + \gamma \left( \sqrt{\phi} - V_{BS} - \sqrt{\phi} \right) \]

Model Parameters: \{\mu, C_{OX}, V_{T0}, \phi, \gamma, \lambda\}

Design Parameters: \{W, L\} but only one degree of freedom W/L
Most analog circuits operate in the saturation region
(basic VVR operates in triode and is an exception)

Most digital circuits operate in triode and cutoff regions and switch between these two with Boolean inputs
Model Extension (short devices)

\[
I_d = \begin{cases} 
0 & V_{gs} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{gs} - V_T - \frac{V_{ds}}{2} \right) V_{ds} & V_{gs} \geq V_T, V_{ds} < V_{gs} - V_T \\
\mu C_{ox} \frac{W}{2L} (V_{gs} - V_T)^2 & V_{gs} \geq V_T, V_{ds} \geq V_{gs} - V_T 
\end{cases}
\]

As the channel length becomes very short, velocity saturation will occur in the channel and this will occur with electric fields around 2V/u. So, if a gate length is around 1u, then voltages up to 2V can be applied without velocity saturation. But, if gate length decreases and voltages are kept high, velocity saturation will occur

\[
I_d = \begin{cases} 
0 & V_{gs} \leq V_T \\
\theta_2 \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)^{\alpha} V_{ds} & V_{gs} \geq V_T, V_{ds} < \theta_1 (V_{gs} - V_T)^{\alpha} \\
\theta_2 \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)^{\alpha} & V_{gs} \geq V_T, V_{ds} \geq \theta_1 (V_{gs} - V_T)^{\alpha} 
\end{cases}
\]

\(\alpha\) is the velocity saturation index, \(2 \geq \alpha \geq 1\)
Model Extension (short devices)

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^a V_{DS} & V_{GS} \geq V_T, V_{DS} < \theta_1 (V_{GS} - V_T)^2 \\
\theta_2 \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^a & V_{GS} \geq V_T, V_{DS} \geq \theta_1 (V_{GS} - V_T)^2 
\end{cases}
\]

\( \alpha \) is the velocity saturation index, \( 2 \geq \alpha \geq 1 \)

No longer a square-law model (some term it an \( \alpha \)-power model)

For long devices, \( \alpha = 2 \)

Channel length modulation (\( \lambda \)) and bulk effects can be added to the velocity Saturation as well

Degrading of \( \alpha \) is not an attractive limitation of the MOSFET
Model Extension (BSIM model)

```
.MODEL CMOSN NMOS ( 
+VERSION = 3.1 TNUM = 27 LEVEL = 49
+XJ = 1.5E-7 NCH = 1.7E17 TOX = 1.42E-8
+K1 = 0.8976376 K2 = -0.09255 VTH0 = 0.629035
+K3B = -8.2369696 W0 = 1.041146E-8 K3 = 24.0984767
+DVTOW = 0 DVT1W = 0 NLX = 1E-9
+DVT0 = 2.7123969 DVT1 = 0.4232931 DVT2W = 0
+U0 = 451.2322004 UA = 3.091785E-13 DVT2 = -0.1403765
+UC = 1.22401E-11 VSAT = 1.715884E5 UB = 1.702517E-18
+AGS = 0.130484 BO = 2.446405E-6 A0 = 0.6580918
+KETA = -3.043349E-3 A1 = 8.18159E-7 B1 = 5E-6
+RDSW = 1.367055E3 PRWG = 0.0328586 A2 = 0.3363058
+WR = 1 WINT = 2.443677E-7 PRWB = 0.0104806
+XL = 1E-7 XW = 0 LINT = 6.999776E-8
+DWB = 3.676235E-8 VOFF = -1.493503E-4 DWG = -1.256454E-8
+CID = 0 CDSC = 2.4E-4 NFACTOR = 1.0354201
+CDSCB = 0 CDSCS = 0
+DSUB = 0.0764123 ETA0 = 2.342963E-3 CDSCD = 0
+PDIBLC2 = 2.366707E-3 PDIBLCB = -0.0431505
+PSCBE1 = 6.611774E8 PSCBE2 = 3.238266E-4
+PRT = 0 UTE = -1.5 KT1 = -0.11
+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+WL = 0 WLN = 1 WW = 0
+WLN = 1 WLL = 0 LL = 0
+LN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.32E-10 CGSO = 2.32E-10
+DJ = 4.282017E-4 PB = 0.93117787 MJ = 0.4495867
+CSW = 3.034055E-10 PBSW = 0.8 MJSW = 0.1713852
+CJSWG = 1.64E-10 PBSWG = 0.8 MJSWG = 0.1713852
+CF = 0 PVTH0 = 0.0520855 PRDSW = 112.8875816
+PK2 = -0.0289036 WKETA = -0.0237483 LKETA = 1.728324E-3 )
```
Model Errors with Different W/L Values

Binning models can improve model accuracy
BSIM Binning Model

- Bin on device sizes
- multiple BSIM models!

With 32 bins, this model has 3040 model parameters!
Model Changes with Process Variations

(n-ch characteristics shown)

Corner models can improve model accuracy
BSIM Corner Models with Binning

- Often 4 corners in addition to nominal TT, FF, FS, SF, and SS

- bin on device sizes

With 32 size bins and 4 corners, this model has 15,200 model parameters!
How many models of the MOSFET do we have?

Switch-level model (2)

Square-law model

Square-law model (with $\lambda$ and bulk additions)

$\alpha$-law model (with $\lambda$ and bulk additions)

BSIM model

BSIM model (with binning extensions)

BSIM model (with binning extensions and process corners)
The Modeling Challenge

Difficult to obtain analytical functions that accurately fit actual devices over bias, size, and process variations.

\[
\begin{align*}
I_D &= f_1(V_{GS}, V_{DS}) \\
I_G &= f_2(V_{GS}, V_{DS}) \\
I_B &= f_3(V_{GS}, V_{DS})
\end{align*}
\]
End of Lecture 14