EE 330
Lecture 15

Devices in Semiconductor Processes
the MOS Transistor
A CMOS Process Flow
Review from Last Time

Fringe Capacitors

\[ C = \frac{\varepsilon A}{d} \]

A is the area where the two plates are parallel

Only a single layer is needed to make fringe capacitors
Capacitance

Junction Capacitor

\[ C = \frac{C_{j0} A}{\left(1 - \frac{V_D}{\phi_B}\right)^n} \quad \text{for} \quad V_{FB} < \frac{\phi_B}{2} \]

Voltage dependence is substantial

\[ \phi_B \approx 0.6 \text{V} \quad n \approx 0.5 \]
Review from Last Time

n-Channel MOSFET

Source
Gate

L

W

Drain

Bulk

L_{EFF}
Apply small $V_{GS}$
$(V_{DS}$ and $V_{BS}$ assumed to be small)
Depletion region electrically induced in channel
Termed “cutoff” region of operation

$ID=0$
$IG=0$
$IB=0$
Critical value of $V_{GS}$ that creates inversion layer termed threshold voltage, $V_T$.

Inversion layer forms in channel
Inversion layer will support current flow from D to S
Channel behaves as thin-film resistor

Increase $V_{GS}$ more

$V_{DS}$ and $V_{BS}$ small

$IDR_{CH}=V_{DS}$
$I_G=0$
$I_B=0$
Review from Last Time

Triode Region of Operation

For $V_{DS}$ small

$$R_{CH} = \frac{L}{W} \frac{1}{(V_{GS} - V_T)\mu C_{OX}}$$

$$I_D = \mu C_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

$$I_G = I_B = 0$$
n-Channel MOSFET Operation and Model

Increase $V_{DS}$

Inversion layer thins near drain

$I_D$ no longer linearly dependent upon $V_{DS}$

Still termed "ohmic" or "triode" region of operation

$I_D = \text{?}$

$I_G = 0$

$I_B = 0$
Triode Region of Operation

For $V_{DS}$ larger

$$R_{CH} = \frac{L}{W (V_{GS} - V_T) \mu C_{OX}}$$

$$I_D = \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS}$$

$$I_G = I_B = 0$$
n-Channel MOSFET Operation and Model

Increase $V_{DS}$ even more

Inversion layer disappears near drain

Termed “saturation” region of operation

Saturation first occurs when $V_{DS} = V_{GS} - V_T$

$I_D = ?$

$I_G = 0$

$I_B = 0$
Saturation Region of Operation

For $V_{DS}$ at saturation

\[ I_D = \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \]

or equivalently

\[ I_D = \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{GS} - V_T}{2} \right) (V_{GS} - V_T) \]

or equivalently

\[ I_D = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_T)^2 \]

\[ I_G = I_B = 0 \]
n-Channel MOSFET Operation and Model

Increase $V_{DS}$ even more (beyond $V_{GS} - V_T$)

Nothing much changes !!
Termed “saturation” region of operation

$I_D = ?$
$I_G = 0$
$I_B = 0$
Saturation Region of Operation

For $V_{DS}$ in Saturation

$$I_D = \frac{\mu C_{OX} W}{2L} \left(V_{GS} - V_T\right)^2$$

$I_G = I_B = 0$
Model Summary

\[ I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} > V_T \text{ or } V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & \text{if } V_{GS} > V_T \text{ and } V_{DS} \geq V_{GS} - V_T
\end{cases} \]

\[ V_{BS} = 0 \]

Note: This is the third model we have introduced for the MOSFET.
Graphical Interpretation of MOS Model

\[ I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) V_{DS} & V_{GS} > V_T \\
\mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} > V_T \quad V_{DS} \geq V_{GS} - V_T 
\end{cases} \]
Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T=1V$ and $\mu C_{OX}=100\mu A V^{-2}$

Solution:

Since $V_{GS}>V_T$, $M_1$ is operating in either saturation or triode region
Strategy will be to guess region of operation, solve, and then verify region
Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T=1$V and $\mu C_{OX}=100\mu A V^{-2}$

Solution:

Guess $M_1$ in saturation

\[
5V = I_D 10k + V_{OUT}
\]

\[
I_D = \frac{\mu C_{OX} W}{2L} (2-V_T)^2
\]

Required verification: $V_{DS}>V_{GS}-V_T$

Can eliminate $I_D$ between these 2 equations to obtain $V_{OUT}$
Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T = 1V$ and $\mu C_{OX} = 100 \mu A V^{-2}$

Guess $M_1$ in saturation

\[
\begin{aligned}
5V &= I_D 10K + V_{OUT} \\
I_D &= \frac{\mu C_{OX} W}{2L} (3 - V_T)^2
\end{aligned}
\]

\[
V_{OUT} = 5V - 10K \left[ \frac{100 \mu A V^{-2} 10 \mu}{2 \cdot 2 \mu} (2V)^2 \right]
\]

\[
V_{OUT} = 5V - 10K \left[ \frac{100 \mu A V^{-2} 10 \mu}{2 \cdot 2 \mu} (2V)^2 \right]
\]

\[
V_{OUT} = -5V
\]

Verification: $V_{DS} = V_{OUT}$

-5 >? 2V - - 0 No! So verification fails and Guess of region is invalid
Example: Determine the output voltage for the following circuit using the square-law model of the MOSFET. Assume $V_T=1V$ and $\mu C_{OX}=100\mu A V^{-2}$

Guess $M_1$ in triode

\[
5V = I_D \cdot 10K + V_{OUT}
\]

\[
I_D = \frac{\mu C_{OX} W}{L} \left( 3 - V_T - \frac{V_{DS}}{2} \right) V_{DS}
\]

\[
V_{OUT} = 5V - 10K \left[ \frac{100\mu A V^{-2}}{2\mu} \left( 2V - \frac{V_{OUT}}{2} \right) V_{OUT} \right]
\]

\[
V_{OUT} = 5V - 5 \left( 2V - \frac{V_{OUT}}{2} \right) V_{OUT}
\]

Solving for $V_{OUT}$, obtain

\[
V_{OUT} = 0.515V
\]

Verification: $V_{DS} = V_{OUT}$

$0.515 < 2V \Rightarrow 0$ Yes! So verification succeeds and triode region is invalid

\[
V_{OUT} = 0.515V
\]
Model Extensions

Existing Model

Slope is not 0
Model Extensions

\[ I_d = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} > V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 \cdot (1 + \lambda V_{DS}) & \text{if } V_{GS} > V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases} \]
Further Model Extensions

Existing model does not depend upon the bulk voltage!

Observe that changing the bulk voltage will change the electric field in the channel region!
Further Model Extensions

Existing model does not depend upon the bulk voltage!

Observe that changing the bulk voltage will change the electric field in the channel region!

Changing the bulk voltage will change the thickness of the inversion layer.

Changing the bulk voltage will change the threshold voltage of the device.

\[ V_T = V_{T0} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right) \]
Typical Effects of Bulk on Threshold Voltage for n-channel Device

\[ V_T = V_{T0} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right) \]

\[ \gamma \approx 0.4V^{1/2} \quad \phi \approx 0.6V \]

Bulk-Diffusion Generally Reverse Biased \((V_{BS} < 0 \text{ or at least less than 0.3V})\) for n-channel
Shift in threshold voltage with bulk voltage can be substantial
Often \(V_{BS}=0\)
Typical Effects of Bulk on Threshold Voltage for n-channel Device

\[ V_T = V_{T0} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right) \]

\[ \gamma \approx 0.4V^{\frac{1}{2}} \quad \phi \approx 0.6V \]

\[ \Delta V = \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right) \]

\[ \Delta V_T \approx 0.4 \left( \sqrt{0.6} - 5 - \sqrt{0.6} \right) = 0.64V \]
Typical Effects of Bulk on Threshold Voltage for p-channel Device

\[ V_T = V_{T0} - \gamma \left( \sqrt{\phi} + V_{BS} - \sqrt{\phi} \right) \]

\[ \gamma \approx 0.4V^{\frac{1}{2}} \quad \phi \approx 0.6V \]

Bulk-Diffusion Generally Reverse Biased (\( V_{BS} > 0 \) or at least greater than -0.3V) for n-channel

Same functional form as for n-channel devices but \( V_{T0} \) is now negative and the magnitude of \( V_T \) still increases with the magnitude of the reverse bias
Model Parameters: \( \{ \mu, C_{Ox}, V_{T0}, \phi, \gamma, \lambda \} \)

Design Parameters: \( \{ W, L \} \) but only one degree of freedom \( W/L \)
Model Extension (short devices)

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left(V_{GS} - V_T\right)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases}
\]

As the channel length becomes very short, velocity saturation will occur in the channel and this will occur with electric fields around 2V/u. So, if a gate length is around 1u, then voltages up to 2V can be applied without velocity saturation. But, if gate length decreases and voltages are kept high, velocity saturation will occur

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_T\right)^\alpha V_{DS} & V_{GS} \geq V_T, V_{DS} < \theta_1 \left(V_{GS} - V_T\right)^\alpha \\
\theta_2 \mu C_{ox} \frac{W}{L} \left(V_{GS} - V_T\right)^\alpha & V_{GS} \geq V_T, V_{DS} \geq \theta_1 \left(V_{GS} - V_T\right)^\alpha 
\end{cases}
\]

\(\alpha\) is the velocity saturation index, \(2 \geq \alpha \geq 1\)
Model Extension (short devices)

\[
I_D = \begin{cases} 
0 & V_{gs} \leq V_T \\
\frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)^\frac{\alpha}{2} V_{ds} & V_{gs} \geq V_T, V_{ds} < \theta_1 (V_{gs} - V_T)^\frac{\alpha}{2} \\
\theta_3 \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)^\alpha & V_{gs} \geq V_T, V_{ds} \geq \theta_1 (V_{gs} - V_T)^\frac{\alpha}{2}
\end{cases}
\]

\(\alpha\) is the velocity saturation index, \(2 \geq \alpha \geq 1\)

No longer a square-law model (some term it an \(\alpha\)-power model)

For long devices, \(\alpha=2\)

Channel length modulation (\(\lambda\)) and bulk effects can be added to the velocity Saturation as well

Degrading of \(\alpha\) is not an attractive limitation of the MOSFET
Model Extension (BSIM model)

.MOSTLM NMOS ( 
+VERSION = 3.1  TNOM = 27  LEVEL = 49
+KJ = 1.5E-7  NCH = 1.7E17  TOX = 1.42E-8
+K1 = 0.8976376  K2 = -0.09255  VTH0 = 0.629035
+K3B = 8.2369696  W0 = 1.041146E-8  K3 = 24.0984767
+DVTOW = 0  DVT1W = 0  NLX = 1E-9
+DVT0 = 2.7123969  DVT1 = 0.4232931  DVT2 = -0.1403765
+U0 = 451.2322004  UA = 3.091785E-13  UB = 1.702517E-18
+UC = 1.22401E-11  VSAT = 1.715884E5  A0 = 0.6580918
+AQS = 0.130484  B0 = 2.446405E-6  B1 = 5E-6
+KETA = -3.043349E-3  A1 = 8.18159E-7  A2 = 0.3363058
+RDSW = 1.367055E3  PRWG = 0.328586  PRWB = 0.0104806
+WR = 1  WINT = 2.443677E-7  LINT = 6.999776E-8
+XL = 1E-7  XW = 0  DWG = -1.256454E-8
+DWB = 3.676235E-8  VOFF = -1.493303E-4  NFACOR = 1.0354201
+CT = 0  CDSC = 2.4E-4  CDSCD = 0
+CDSCB = 0  ETA0 = 2.342963E-3  ETAB = -1.5324E-4
+DSUB = 0.0764123  PCLM = 2.5941582  PDIBLC1 = 0.8187825
+PDIBLC2 = 2.366707E-3  PDIBLCB = -0.0431505  DROUT = 0.9919348
+PSCBE1 = 6.611774E8  PSCBE2 = 3.238266E-4  PVAG = 0
+FRT = 0  UTE = -1.5  KT1 = -0.11
+KTL = 0  KT2 = 0.022  UA1 = 4.31E-9
+UB1 = -7.61E-18  UC1 = -5.6E-11  AT = 3.3E4
+WL = 0  WLN = 1  WW = 0
+WNN = 1  WWL = 0  LL = 0
+ILN = 1  LW = 0  LWN = 1
+IWL = 0  CAPMOD = 2  XPART = 0.5
+CGDO = 2.32E-10  CGSO = 2.32E-10  CGBO = 1E-9
+CJ = 4.282017E-4  PB = 0.9317787  MJ = 0.4495867
+CJJSW = 3.034055E-10  PBSW = 0.8  MJJSW = 0.1713852
+CJJSWG = 1.64E-10  PBSWG = 0.8  MJJSWG = 0.1713852
+CF = 0  FVTH0 = 0.0520655  PRDSW = 112.6675816
+FK2 = -0.0289036  WKETA = -0.0237483  LKETA = 1.728324E-3 )
Model Extension (BSIM model)

Binning Models - multiple BSIM models!

```
.MODEL CMOSN NMOS 
+VERSION = 3.1 
TNOM = 27 
LEVEL = 49
+KX = 1.5E-7 
K3B = -8.2369696 
+K1 = 0.8976376 
W0 = 1.041146E-8 
+K2 = -0.09255 
NLX = 1E-9 
+DVTOW = 0 
DVT1W = 0 
DVT2W = 0 
+DVT0 = 2.7123969 
DVT1 = 0.4232931 
DVT2 = -0.1403765 
+U0 = 451.2322004 
UA = 3.091785E-13 
+UC = 1.22401E-11 
UB = 1.702517E-18 
+AGS = -0.130484 
VSAT = 1.715884E5 
A0 = 0.6580918
+KETA = -3.043349E-3 
B0 = 2.446405E-6 
A1 = 8.18159E-7 
+RDSW = 1.367055E3 
B1 = 5E-6 
PRWG = 0.0328586 
+WK = 1 
PRWB = 0.0104806 
+WINT = 2.443677E-7 
LINT = 6.999776E-8 
+XL = 1E-7 
DWG = -1.256454E-8 
+DWB = 3.676235E-8 
VOFF = -1.493003E-4 
NFACTOR = 1.0354201 
+CIT = 0 
CDSC = 2.4E-4 
+CDSCB = 0 
CDSCD = 0 
+DSUB = 0.0764123 
ETA0 = 2.342963E-3 
+Etab = -1.5324E-4 
+PDIBLC2 = 2.366707E-3 
PCLM = 2.5941582 
+PDIBLCB = -0.0431505 
PDIBLC1 = 0.8187825 
+RST = 6.611774E8 
PDIBLCE2 = 3.238266E-4 
PSCBE1 = 0
+PSCBE2 = 3.611774E-8 
PSCBE4 = 0
+RST = 0 
UTE = -1.5 
KT1 = -0.11 
+KT1L = 0 
KT2 = 0.022 
UA1 = 4.31E-9 
+UB1 = -7.61E-18 
UC1 = -5.6E-11 
+AT = 3.3E4 
WL = 0 
WL = 1 
WW = 0 
+WLN = 1 
WWL = 0 
+LL = 0 
+LIN = 1 
LW = 0 
LWN = 1 
+LWL = 0 
CAPMOD = 2 
+XPART = 0.5 
+CGDO = 2.32E-10 
CGSO = 2.32E-10 
CGBO = 1E-9 
+CJ = 4.282017E-4 
PBJ = 0.9317787 
MJ = 0.4495867 
+CJJSW = 3.034555E-10 
PBJ = 0.8 
MJJSW = 0.1713852 
+CJJSWG = 1.64E-10 
PBJ = 0.8 
MJJSWG = 0.1713852 
+CF = 0 
FVTH0 = 0.0520855 
FRDSW = 112.8675616 
+FK2 = -0.0289036 
WKETA = -0.0237483 
LKETA = 1.728324E-3 
) 
```
How many models of the MOSFET do we have?

Switch-level model (2)

Square-law model (with $\lambda$ and bulk additions)

$\alpha$-law model (with $\lambda$ and bulk additions)

BSIM model (with binning extensions)
Square-Law Model

\[ I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} > V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & V_{GS} > V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases} \]
Switch-Level Models

Switch-level model including gate capacitance and drain resistance

\[ C_{GS} \] and \[ R_{SW} \] dependent upon device sizes and process

For minimum-sized devices in a 0.5\( \mu \) process

\[ C_{GS} \approx 1.5fF \quad R_{sw} \approx \begin{cases} 2K\Omega & n\text{-channel} \\ 6K\Omega & p\text{-channel} \end{cases} \]

Considerable emphasis will be placed upon device sizing to manage \( C_{GS} \) and \( R_{SW} \)
Extended Square-Law Model

\[ I_G = 0 \]
\[ I_B = 0 \]

\[
I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} \geq V_T \land V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 \cdot \left(1 + \lambda V_{DS} \right) & \text{if } V_{GS} \geq V_T \land V_{DS} \geq V_{GS} - V_T 
\end{cases}
\]

\[
V_T = V_{T0} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right)
\]

Model Parameters : \{\mu, C_{OX}, V_{T0}, \phi, \gamma, \lambda\}

Design Parameters : \{W, L\}  but only one degree of freedom \(W/L\)
Short-Channel Model

\[
I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^\alpha V_{DS} & \text{if } V_{GS} \geq V_T, \ V_{DS} < \theta_1 (V_{GS} - V_T)^\alpha \\
\theta_2 \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^\alpha & \text{if } V_{GS} \geq V_T, \ V_{DS} \geq \theta_1 (V_{GS} - V_T)^\alpha
\end{cases}
\]

\(\alpha\) is the velocity saturation index, \(2 \geq \alpha \geq 1\)

Channel length modulation (\(\lambda\)) and bulk effects can be added to the velocity Saturation as well.
BSIM model

.MODEL CMOSN NMOS

+VERSION = 3.1

+TNOM = 27
+LEVEL = 49
+TOX = 1.42E-8
+KX = 1.5E-7
+K1 = 0.8976376
+K2 = -0.09255
+K3 = 24.0984767
+K3B = -8.2369696
+W0 = 1.041146E-8
+NLX = 1E-9
+DVTOW = 0
+DVT0 = 2.7123969
+DVT1 = 0.4232931
+DVT2 = -0.1403765
+U0 = 451.2322004
+UA = 3.091785E-13
+UB = 1.702517E-18
+UC = 1.22401E-11
+VSAT = 1.715884E5
+A0 = 0.6580918
+AGS = -0.130484
+B0 = 2.446405E-6
+B1 = 5E-6
+KETA = -3.043349E-3
+A1 = 8.18159E-7
+A2 = 0.3363058
+RDSW = 1.367055E3
+PRWG = 0.0328586
+PRWB = 0.0104806
+WR = 1
+WINT = 2.443677E-7
+LINT = 6.99977E-8
+XL = 1E-7
+DWG = -1.256454E-8
+DWB = 3.676235E-8
+VOFF = -1.493303E-4
+NFACTOR = 1.0354201
+CDSC = 2.4E-4
+CDSCD = 0
+CDSCB = 0
+ETA0 = 2.342963E-3
+E TAB = -1.5324E-4
+DUB = 0.0764123
+PCLM = 2.5941582
+PDIBLC1 = 0.8187825
+PDIBLC2 = 2.366707E-3
+PDIBLCB = -0.0431505
+DROUT = 0.9919348
+PSBCE1 = 6.611774E8
+PSBCE2 = 3.238256E-4
+PVAG = 0
+FRT = 0
+UTE = -1.5
+KT1 = -0.11
+KT1L = 0
+KT2 = 0.022
+UA1 = 4.31E-9
+UB1 = -7.61E-18
+UC1 = -5.6E-11
+AT = 3.3E4
+WLN = 0
+WLN = 0
+WW = 0
+WLN = 1
+WL = 0
+WWL = 0
+LL = 0
+ILN = 1
+LW = 0
+LWN = 1
+LWL = 0
+CAPMOD = 2
+XPART = 0.5
+CGDO = 2.32E-10
+CGSO = 2.32E-10
+CGBO = 1E-9
+CJ = 4.282017E-4
+PB = 0.9317787
+MJ = 0.4495867
+CJSW = 3.034055E-10
+PBSW = 0.8
+MJSW = 0.1713852
+CJSGW = 1.64E-10
+PBSWG = 0.8
+MJSWG = 0.1713852
+CF = 0
+FVTHO = 0.0520855
+FRDSW = 112.8875816
+F2K = -0.0289036
+WKETA = -0.0237483
+LKETA = 1.728324E-3

*
BSIM Binning Model
- multiple BSIM models!

.MODEL CMOSN NMOS (LEVEL = 49)
+VERSION = 3.1
+XJ = 1.5E-7
+K1 = 0.8976376
+K3B = -8.2369696
+DVTOW = 0
+DVT0 = 2.7123969
+U0 = 451.2322004
+UC = 1.22401E-11
+AGS = -0.130484
+KETA = -3.043349E-3
+RDSW = 1.367055E3
+WR = 1
+XL = 1E-7
+DWB = 3.676235E-8
+CIT = 0
+CDSCB = 0
+DSUB = 0.0764123
+PDIBLC2 = 2.366707E-3
+PSCBE1 = 6.611774E8
+FRT = 0
+KT1L = 0
+UB1 = -7.61E-18
+WL = 0
+WWN = 1
+LLN = 1
+LWL = 0
+CGDO = 2.32E-10
+CJ = 4.282017E-4
+CJSW = 3.034055E-10
+CJSWG = 1.64E-10
+CF = 0
+FK2 = -0.0289036

*
End of Lecture 15