EE 330
Lecture 15

MOSFET Modeling
CMOS Process Flow
Basic Devices and Device Models

- Resistor
- Diode
- Capacitor
- MOSFET
- BJT
Review from Last Lecture
Graphical Representation of MOS Model

$$I_D = \left\{ \begin{array}{ll} 0 & \quad V_{GS} \leq V_T \\ \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \quad V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\ \mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & \quad V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T \end{array} \right.$$  

$$I_G = I_B = 0$$
Review from Last Lecture

Model Extensions

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS}) & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases}
\]

Note: This introduces small discontinuity (not shown) in model at SAT/Triode transition
Typical Effects of Bulk on Threshold Voltage for n-channel Device

\[
V_T = V_{T0} + \gamma (\sqrt{\phi} - V_{BS} - \sqrt{\phi})
\]

\[
\gamma \approx 0.4V^{\frac{1}{2}} \quad \phi \approx 0.6V
\]

- Bulk-Diffusion Generally Reverse Biased (\(V_{BS} < 0\) or at least less than 0.3V) for n-channel
- Shift in threshold voltage with bulk voltage can be substantial
- Often \(V_{BS}=0\)
Review from Last Lecture

Model Extension Summary

\[ I_G = 0 \]
\[ I_B = 0 \]

\[ I_d = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 \cdot (1 + \lambda V_{DS}) & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases} \]

\[ V_T = V_{T0} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right) \]

Model Parameters : \{\mu, C_{ox}, V_{T0}, \phi, \gamma, \lambda\}

Design Parameters : \{W, L\}  but only one degree of freedom W/L
Most analog circuits operate in the saturation region
(basic VVR operates in triode and is an exception)

Most digital circuits operate in triode and cutoff regions and switch between these two with Boolean inputs
Review from Last Lecture

Model Extension (short devices)

\[
I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^{\alpha} V_{DS} & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} < \theta_1 (V_{GS} - V_T)^2 \\
\theta_2 \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^{\alpha} & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} \geq \theta_1 (V_{GS} - V_T)^2 
\end{cases}
\]

\( \alpha \) is the velocity saturation index, \( 2 \geq \alpha \geq 1 \)

No longer a square-law model (some term it an \( \alpha \)-power model)

For long devices, \( \alpha=2 \)

Channel length modulation (\( \lambda \)) and bulk effects can be added to the velocity Saturation as well

Degrating of \( \alpha \) is not an attractive limitation of the MOSFET
Review from Last Lecture

Model Extension (BSIM model)

```
.MODEL CMOSN NMOS (  
+VERSION = 3.1  
+XJ      = 1.5E-7  
+K1      = 0.8976376  
+K3B     = -8.2369696  
+DVT0W   = 0  
+DVT0    = 2.7123969  
+U0      = 451.2322004  
+UC      = 1.22401E-11  
+AGS     = 0.130484  
+KETA    = -3.043349E-3  
+RDSW    = 1.367055E3  
+WR      = 1  
+XL      = 1E-7  
+DWB     = 3.676235E-8  
+CIT     = 0  
+CDSCB   = 0  
+DSUB    = 0.0764123  
+PDIBLC2 = 2.366707E-3  
+PSCBE1  = 6.611774E8  
+PRT     = 0  
+KT1L    = 0  
+UB1     = -7.61E-18  
+WL      = 0  
+WWN     = 1  
+LLN     = 1  
+LWL     = 0  
+CGDO    = 2.32E-10  
+CJ      = 4.282017E-4  
+CJSW    = 3.034055E-10  
+CJSWG   = 1.64E-10  
+CF      = 0  
+PK2     = -0.0289036  
*LEVEL   = 49  
TOX      = 1.42E-8  
VTH0     = 0.629035  
K3       = 24.0984767  
NLX      = 1E-9  
DVT1W    = 0  
DVT1     = 0.4232931  
UA       = 3.091785E-13  
VSAT     = 1.715884E5  
B0       = 2.446405E-6  
A1       = 8.18159E-7  
PRWG     = 0.0328586  
WINT     = 2.443677E-7  
A2       = 0.3363058  
DWF      = 0  
XW       = 0  
LINT     = 6.999776E-8  
B1       = 5E-6  
VOFP     = -1.493503E-4  
CDSC     = 2.4E-4  
ETA0     = 2.342963E-3  
CDSCD    = 0  
PCLM     = 2.5941582  
ETAB     = -1.5324E-4  
PDIRBC1  = 0.8187825  
DROUT    = 0.9919348  
PSCBE2   = 3.238266E-4  
PVAG     = 0  
UTE      = -1.5  
KT1      = -0.11  
UA1      = 4.31E-9  
UC1      = -5.6E-11  
AT       = 3.3E4  
WLN      = 1  
WW       = 0  
WVL      = 0  
LL       = 0  
LW       = 0  
CAPMOD   = 2  
XPART    = 0.5  
CGSO     = 2.32E-10  
CGBO     = 1E-9  
PB       = 0.9317787  
PBSW     = 0.8  
PBSWG    = 0.8  
PVTTH0   = 0.0520855  
PRDSW    = 112.8875816  
LKETA    = 1.728324E-3  )
```
Model Errors with Different W/L Values

Binning models can improve model accuracy
BSIM Binning Model
- Bin on device sizes
- multiple BSIM models!

With 32 bins, this model has 3040 model parameters!
Model Changes with Process Variations

(n-ch characteristics shown)

Corner models can improve model accuracy
BSIM Corner Models with Binning
- Often 4 corners in addition to nominal TT, FF, FS, SF, and SS
- bin on device sizes

With 32 size bins and 4 corners, this model has 15,200 model parameters!
How many models of the MOSFET do we have?

Switch-level model (2)

Square-law model

Square-law model (with $\lambda$ and bulk additions)

$\alpha$-law model (with $\lambda$ and bulk additions)

BSIM model

BSIM model (with binning extensions)

BSIM model (with binning extensions and process corners)
Difficult to obtain analytical functions that accurately fit actual devices over bias, size, and process variations.

\[
I_D = f_1(V_{GS}, V_{DS})
\]
\[
I_G = f_2(V_{GS}, V_{DS})
\]
\[
I_B = f_3(V_{GS}, V_{DS})
\]
In the next few slides, the models we have developed will be listed and reviewed

- Square-law Model
- Switch-level Models
- Extended Square-law model
- Short-channel model
- BSIM Model
- BSIM Binning Model
- Corner Models
Square-Law Model

Model Parameters: \( \{\mu, C_{ox}, V_{T0}\} \)

Design Parameters: \( \{W,L\} \) but only one degree of freedom \( W/L \)

\[
I_D = \begin{cases} 
0 & \text{if } V_{gs} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{gs} - V_T - \frac{V_{ds}}{2} \right) V_{ds} & \text{if } V_{gs} \geq V_T \land V_{ds} < V_{gs} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{gs} - V_T \right)^2 & \text{if } V_{gs} \geq V_T \land V_{ds} \geq V_{gs} - V_T
\end{cases}
\]
Switch-Level Models

Switch-level model including gate capacitance and drain resistance

\[ C_{GS} \text{ and } R_{SW} \text{ dependent upon device sizes and process} \]

For minimum-sized devices in a 0.5\(\mu\) process

\[ C_{GS} \approx 1.5fF \quad R_{sw} \approx \begin{cases} 2K\Omega & \text{n-channel} \\ 6K\Omega & \text{p-channel} \end{cases} \]

Considerable emphasis will be placed upon device sizing to manage \(C_{GS}\) and \(R_{SW}\)

Model Parameters : \(\{C_{GS}, R_{SW}\}\)
Extended Square-Law Model

\[ I_G = 0 \]
\[ I_B = 0 \]

\[ I_d = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left(V_{GS} - V_T\right)^2 \cdot (1 + \lambda V_{DS}) & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases} \]

\[ V_T = V_{T0} + \gamma \left(\sqrt{\phi - V_{BS}} - \sqrt{\phi}\right) \]

Model Parameters : \( \{ \mu, C_{OX}, V_{T0}, \phi, \gamma, \lambda \} \)

Design Parameters : \( \{ W, L \} \) but only one degree of freedom \( W/L \)
Short-Channel Model

\[ I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 V_{DS} & \text{if } V_{GS} \geq V_T, V_{DS} < \theta_1 (V_{GS} - V_T)^2 \\
\theta_2 \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^\alpha & \text{if } V_{GS} \geq V_T, V_{DS} \geq \theta_1 (V_{GS} - V_T)^2 
\end{cases} \]

\( \alpha \) is the velocity saturation index, \( 2 \geq \alpha \geq 1 \)

Channel length modulation (\( \lambda \)) and bulk effects can be added to the velocity Saturation as well.
BSIM model

.MODEL CMOSN NMOS

+VERSION = 3.1
+XJ = 1.5E-7
+K1 = 0.8976376
+K3B = -8.2369696
+DVTOW = 0
+DVT0 = 2.7123969
+U0 = 451.2322004
+UC = 1.22401E-11
+AGS = 0.130484
+KETA = -3.043349E-3
+RDSW = 1.367055E3
+WR = 1
+XL = 1E-7
+DWB = 3.676235E-8
+CIT = 0
+CDSCB = 0
+DSUB = 0.0764123
+PDIBLC2 = 2.366707E-3
+PSCBE1 = 6.61774E8
+PRT = 0
+KT1L = 0
+UB1 = -7.61E-18
+WL = 0
+WNN = 1
+LLN = 1
+LWL = 0
+CGDO = 2.32E-10
+CJ = 4.282017E-4
+CJSW = 3.034055E-10
+CJSWG = 1.64E-10
+CF = 0
+PK2 = -0.0289036

LEVEL = 49
TOX = 1.42E-8
VTH0 = 0.629035
K3 = 24.0984767
W0 = 1.041146E-8
NLX = 1E-9
DVT1W = 0
DVT2 = -0.1403765
UB = 1.702517E-18
A0 = 0.6580918
B0 = 2.446405E-6
A1 = 8.18159E-7
B1 = 5E-6
A2 = 0.3363058
PRWG = 0.0328586
PR WB = 0.0104806
LINT = 6.999776E-8
DWG = -1.256454E-8
Voff = -1.493503E-4
NSF ACTOR = 1.0354201
CDSC = 0
ETA0 = 2.342963E-3
ETAB = -1.5324E-4
PCLM = 2.5941582
PDIBLC1 = 0.8187825
PDIBLCB = -0.0431505
DROUT = 0.9919348
PVAG = 0
UTE = -1.5
KT1 = -0.11
KT2 = 0.022
UC1 = -5.6E-11
WLN = 1
WWL = 0
LW = 0
LWN = 1
CAPMOD = 2
XPART = 0.5
CGSO = 2.32E-10
CGBO = 1E-9
PB = 0.9317787
MJ = 0.4495867
PBSW = 0.8
PMJSW = 0.1713852
PB SW = 0.8
MJSWG = 0.1713852
PVTH0 = 0.0520855
PR DSW = 112.8875816
WK ETA = -0.0237483
LK ETA = 1.728324E-3

Note this model has 95 model parameters!
BSIM Binning Model
- Bin on device sizes
- multiple BSIM models!

```
.MODEL CMOSN NMOS

+VERSION = 3.1
+XJ = 1.5E-7
+K1 = 0.8976376
+K3B = -8.2369696
+DVTOW = 0
+DVT0 = 2.7123969
+U0 = 451.2322004
+UC = 1.22401E-11
+AGS = 0.130484
+KETA = -3.043349E-3
+RDSW = 1.367055E3
+WR = 1
+XL = 1E-7
+DWB = 3.676235E-8
+CIT = 0
+CDSCB = 0
+DSUB = 0.0764123
+PDIBLC2 = 2.366707E-3
+PSCBE1 = 6.611774E8
+PRT = 0
+KT1L = 0
+UB1 = -7.61E-18
+WL = 0
+WWN = 1
+LLN = 1
+LWL = 0
+CGDO = 2.32E-10
+CJ = 4.282017E-4
+CJSW = 3.034055E-10
+CF = 0
+PK2 = -0.0289036

TNOM = 27
NCH = 1.7E17
K2 = -0.09255
W0 = 1.041146E-8
DVT1W = 0
DVT1 = 0.4232931
UA = 3.091785E-13
VSAT = 1.715884E5
B0 = 2.446405E-6
A1 = 8.18159E-7
PRWG = 0.0328586
WINT = 2.443677E-7
XL = 1E-7
VOFF = -1.493503E-4
CDSC = 2.4E-4
ETA0 = 2.342963E-3
PCLM = 2.5941582
PDIBLC = -0.0431505
PSCE2 = 3.238266E-4
UTE = -1.5
KT2 = 0.022
UC1 = -5.6E-11
WL = 1
WWL = 0
LW = 0
CAPMOD = 2
CGSO = 2.32E-10
PB = 0.9317787
PBSW = 0.8
PVSWG = 0.8
PVT0H = 0.0520855
PKETA = -0.0237483

LEVEL = 49
TOX = 1.42E-8
VTH0 = 0.629035
K3 = 24.0984767
NLX = 1E-9
DV2 = -0.1403765
UB = 1.702517E-18
A0 = 0.6580918
B1 = 5E-6
PRWB = 0.0104806
LINT = 6.999776E-8
DWG = -1.256454E-8
NFACOR = 1.0354201
CDSCD = 0
ETAB = -1.5324E-4
PDIBLC1 = 0.8187825
DROUT = 0.9919348
PVAG = 0
KT1 = -0.11
UA1 = 4.31E-9
AT = 3.3E4
WW = 0
LL = 0
LWN = 1
XPART = 0.5
MJ = 0.4495867
MJSW = 0.1713852
MJSWG = 0.1713852
PRDSW = 112.8875816
LKETA = 1.728324E-3

* With 32 bins, this model has 3040 model parameters!
```
BSIM Corner Models

- Often 4 corners in addition to nominal TT, FF, FS, SF, and SS
- five different BSIM models!

With 4 corners, this model has 475 model parameters!
Hierarchical Model Comparisons

Accuracy

Complexity

Switch-Level Models
Number of Model Parameters
0 to 2

Square-Law Models
Number of Model Parameters
3 to 6

BSIM Models
Number of Model Parameters
Approx 100

BSIM Binning Models
Number of Model Parameters
Approx 3000 (for 30 bins)

Analytical
Numerical (for simulation only)

(For 30 bins)
Corner Models

Applicable at any level in model hierarchy (same model, different parameters)

Often 4 corners (FF, FS, SF, SS) used but sometimes many more

Designers must provide enough robustness so good yield at all corners
n-channel .... p-channel modeling

Positive $V_{DS}$ and $V_{GS}$ cause a positive $I_D$
n-channel .... p-channel modeling

Functional form of models are the same, just sign differences and some parameter differences (usually mobility is the most important)
n-channel .... p-channel modeling

The diagram shows a p-channel MOSFET with labels for Source, Gate, and Drain. The drain-current relationship is given by:

\[ I_D = \begin{cases} \mu_p C_{ox} \frac{W}{L} \left( V_{GS} - V_{Tp} - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} \geq V_{Tp} \\ - \mu_p C_{ox} \frac{W}{2L} \left( V_{GS} - V_{Tp} \right)^2 & \text{if } V_{GS} \leq V_{Tp}, V_{DS} > V_{GS} - V_{Tp} \\ \end{cases} \]

where \( I_D \) is the drain current, \( V_{GS} \) is the gate-source voltage, \( V_{DS} \) is the drain-source voltage, \( V_{Tp} \) is the threshold voltage, \( \mu_p \) is the mobility, \( C_{ox} \) is the oxide capacitance, \( W \) is the channel width, and \( L \) is the channel length.

The alternate equivalent representation is:

\[ I_D = \begin{cases} 0 & \text{if } |V_{GS}| \leq |V_{Tp}| \\ \mu_p C_{ox} \frac{W}{L} \left( V_{GS} - V_{Tp} - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } |V_{GS}| > |V_{Tp}|, |V_{DS}| < |V_{GS} - V_{Tp}| \\ \mu_p C_{ox} \frac{W}{2L} \left( V_{GS} - V_{Tp} \right)^2 & \text{if } |V_{GS}| > |V_{Tp}|, |V_{DS}| \geq |V_{GS} - V_{Tp}| \\ \end{cases} \]

The boundary condition is given by:

\[ I_G = I_B = 0 \]

These look like those for the n-channel device but with \(||\).
n-channel .... p-channel modeling

Models essentially the same with different signs and model parameters

\[
\begin{align*}
I_s &= 0 \\
I_s &= \mu_C \frac{W}{L} (V_{gs} - V_t - \frac{V_D}{2}) V_{es} \\
I_s &= \mu_C \frac{W}{2L} (V_{gs} - V_t) \\
I_s &= I_s = I_s = 0
\end{align*}
\]

\[
\begin{align*}
I_s &= 0 \\
I_s &= -\mu_C \frac{W}{L} (V_{gs} - V_t - \frac{V_D}{2}) V_{es} \\
I_s &= -\mu_C \frac{W}{2L} (V_{gs} - V_t) \\
I_s &= I_s = I_s = 0
\end{align*}
\]
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an n-channel MOSFET from square-law model.

In the 0.5µ CMOS process if $L=1µ$, $W=1µ$

(Assume $\mu C_{OX}=100\mu A V^{-2}$, $C_{OX}=2.5fF u^{-2}$, $V_T=1V$, $V_{DD}=3.5V$, $V_{SS}=0$)

$$I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{OX} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T
\end{cases}$$

when SW is on, operation is “deep” triode
Model Relationships

Determine \( R_{SW} \) and \( C_{GS} \) for an n-channel MOSFET from square-law model.

In the 0.5\( \mu \) CMOS process if \( L=1\mu \), \( W=1\mu \)

(Assume \( \mu C_{OX}=100\mu A V^{-2} \), \( C_{OX}=2.5fF\mu^{-2} \), \( V_{T0}=1V \), \( V_{DD}=3.5V \), \( V_{SS}=0 \))

\[
I_D = \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \mu C_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS}
\]

\[
R_{SQ} = \left| \frac{V_{DS}}{I_D} \right|_{V_{GS}=V_{DD}} = \frac{1}{\mu C_{OX} \frac{W}{L} (V_{GS} - V_T)} \bigg|_{V_{GS}=3.5V} = \frac{1}{(E-4) \left( \frac{1}{1} \right) (3.5-1)} = 4K\Omega
\]

\[
C_{GS} = C_{OX} WL = (2.5fF\mu^{-2})(1\mu^2) = 2.5fF
\]
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an *p*-channel MOSFET from square-law model
In the 0.5u CMOS process if $L=1u$, $W=1u$

\[
C_{OX}=2.5fF \mu m^{-2}, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0
\]

Observe $\mu_n/\mu_p \approx 3$

\[
I_d = \begin{cases} 
0 & V_{GS} \leq V_T \\ 
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\ 
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases}
\]

When SW is on, operation is “deep” triode
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an p-channel MOSFET from square-law model in the 0.5μ CMOS process if $L=1μ$, $W=1μ$

\[
(C_{OX}=2.5fFμ^{-2}, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0)
\]

Observe $\mu_n \mu_p \approx 3$

\[
I_d = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T 
\end{cases}
\]

When SW is on, operation is “deep” triode
**Model Relationships**

Determine $R_{SW}$ and $C_{GS}$ for an p-channel MOSFET from square-law model in the 0.5u CMOS process if $L=1u$, $W=1u$

\[
(C_{OX}=2.5fF\mu^{-2}, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0)
\]

Observe $\mu_n/\mu_p \approx 3$

\[
I_D = \mu_p C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \mu_p C_{OX} \frac{W}{L} \left( V_{GS} - V_T \right) V_{DS}
\]

\[
R_{SQ} = \left. \frac{V_{DS}}{I_D} \right|_{V_{GS}=V_{DD}} = \frac{1}{\mu_p C_{OX} \frac{W}{L} \left( V_{GS} - V_T \right)} \left|_{V_{GS}=3.5V} \right. = \frac{1}{\left( \frac{1}{3} E - 4 \right) \frac{1}{1} (3.5 - 1)} = 12K\Omega
\]

$C_{GS} = C_{OX}WL = (2.5fF\mu^{-2})(1\mu^2) = 2.5fF$

Observe the resistance of the p-channel device is approximately 3 times larger than that of the n-channel device for same bias and dimensions!
Modeling of the MOSFET

Goal: Obtain a mathematical relationship between the port variables of a device.

\[ I_D = f_1(V_{GS}, V_{DS}, V_{BS}) \]
\[ I_G = f_2(V_{GS}, V_{DS}, V_{BS}) \]
\[ I_B = f_3(V_{GS}, V_{DS}, V_{BS}) \]
Small-Signal Model

Goal with small signal model is to predict performance of circuit or device in the vicinity of an operating point

Operating point is often termed Q-point
Small-Signal Model

Analytical expressions for small signal model will be developed later
Technology Files

- Design Rules
- Process Flow (Fabrication Technology)
- Model Parameters
### TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process

<table>
<thead>
<tr>
<th>Step</th>
<th>Process Description</th>
<th>Mask</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Clean wafer</td>
<td></td>
</tr>
<tr>
<td>2.</td>
<td>GROW THIN OXIDE</td>
<td></td>
</tr>
<tr>
<td>3.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td>PATTERN n-well (MASK #1)</td>
<td></td>
</tr>
<tr>
<td>5.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>6.</td>
<td>Deposit and diffus n-type impurities</td>
<td></td>
</tr>
<tr>
<td>7.</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>8.</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>9.</td>
<td>Grow thin oxide</td>
<td></td>
</tr>
<tr>
<td>10.</td>
<td>Apply layer of Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>11.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>12.</td>
<td>PATTERN Si$_3$N$_4$ (active area definition) (MASK #2)</td>
<td></td>
</tr>
<tr>
<td>13.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>14.</td>
<td>Etch Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>15.</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Optional field threshold voltage adjust</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.1 Apply photoresist</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.2 PATTERN ANTIMOAT IN SUBSTRATE (MASK #A1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.3 Develop photoresist</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.4 FIELD IMPLANT p-type</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.5 Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>16.</td>
<td>GROW FIELD OXIDE</td>
<td></td>
</tr>
<tr>
<td>17.</td>
<td>Strip Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>18.</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>19.</td>
<td>GROW GATE OXIDE</td>
<td></td>
</tr>
<tr>
<td>20.</td>
<td>POLYSILICON DEPOSITION (POLY I)</td>
<td></td>
</tr>
<tr>
<td>21.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>22.</td>
<td>PATTERN POLYSILICON</td>
<td>(MASK #3)</td>
</tr>
<tr>
<td>23.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>24.</td>
<td>ETCH POLYSILICON</td>
<td></td>
</tr>
</tbody>
</table>
25. Strip photoresist  
*Optional steps for double polysilicon process*  
B.1 Strip thin oxide  
B.2 GROW THIN OXIDE  
B.3 POLYSILICON DEPOSITION (POLY II)  
B.4 Apply photoresist  
B.5 PATTERN POLYSILICON (MASK #B1)  
B.6 Develop photoresist  
B.7 ETCH POLYSILICON  
B.8 Strip photoresist  
B.9 Strip thin oxide

26. Apply photoresist

27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P+ GUARD RINGS (p-well ohmic contacts) (MASK #4)

28. Develop photoresist

29. p+ IMPLANT

30. Strip photoresist

31. Apply photoresist

32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)

33. Develop photoresist

34. n+ IMPLANT

35. Strip photoresist

36. Strip thin oxide

37. Grow oxide

38. Apply photoresist

39. PATTERN CONTACT OPENINGS (MASK #6)

40. Develop photoresist

41. Etch oxide

42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL (MASK #7)
46. Develop photoresist
47. Etch metal
48. Strip photoresist
   Optional steps for double metal process
   C.1 Strip thin oxide
   C.2 DEPOSIT INTERMETAL OXIDE
   C.3 Apply photoresist
   C.4 PATTERN VIAS (MASK #C1)
   C.5 Develop photoresist
   C.6 Etch oxide
   C.7 Strip photoresist
   C.8 APPLY METAL (Metal 2)
   C.9 Apply photoresist
   C.10 PATTERN METAL (MASK #C2)
   C.11 Develop photoresist
   C.12 Etch metal
   C.13 Strip photoresist
49. APPLY PASSIVATION (MASK #8)
50. Apply photoresist
51. PATTERN PAD OPENINGS
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST
Bulk CMOS Process Description

• n-well process
• Single Metal Only Depicted
• Double Poly
  - This type of process dominates what is used for high-volume “low-cost” processing of integrated circuits today
  - Many process variants and specialized processes are used for lower-volume or niche applications
  - Emphasis in this course will be on the electronics associated with the design of integrated electronic circuits in processes targeting high-volume low-cost products where competition based upon price differentiation may be acute
  - Basic electronics concepts, however, are applicable for lower-volume or niche applications
Components Shown

- n-channel MOSFET
- p-channel MOSFET
- Poly Resistor
- Doubly Poly Capacitor
Consider Basic Components Only

Well Contacts and Guard Rings Will be Discussed Later
Metal details hidden to reduce clutter

n-channel MOSFET
A

Capacitor

B

Resistor

p-channel MOSFET

A'

B'

n-channel MOSFET
<table>
<thead>
<tr>
<th></th>
<th>Process step</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Clean wafer</td>
</tr>
<tr>
<td>2.</td>
<td>GROW THIN OXIDE</td>
</tr>
<tr>
<td>3.</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>4.</td>
<td>PATTERN n-well</td>
</tr>
<tr>
<td>5.</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>6.</td>
<td>Deposit and diffus n-type impurities</td>
</tr>
<tr>
<td>7.</td>
<td>Strip photoresist</td>
</tr>
<tr>
<td>8.</td>
<td>Strip thin oxide</td>
</tr>
<tr>
<td>9.</td>
<td>Grow thin oxide</td>
</tr>
<tr>
<td>10.</td>
<td>Apply layer of Si$_3$N$_4$</td>
</tr>
<tr>
<td>11.</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>12.</td>
<td>PATTERN Si$_3$N$_4$ (active area definition)</td>
</tr>
<tr>
<td>13.</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>14.</td>
<td>Etch Si$_3$N$_4$</td>
</tr>
<tr>
<td>15.</td>
<td>Strip photoresist</td>
</tr>
<tr>
<td>A.1</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>A.2</td>
<td>PATTERN ANTIMOAT IN SUBSTRATE</td>
</tr>
<tr>
<td>A.3</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>A.4</td>
<td>FIELD IMPLANT p-type</td>
</tr>
<tr>
<td>A.5</td>
<td>Strip photoresist</td>
</tr>
<tr>
<td>16.</td>
<td>GROW FIELD OXIDE</td>
</tr>
<tr>
<td>17.</td>
<td>Strip Si$_3$N$_4$</td>
</tr>
<tr>
<td>18.</td>
<td>Strip thin oxide</td>
</tr>
<tr>
<td>19.</td>
<td>GROW GATE OXIDE</td>
</tr>
<tr>
<td>20.</td>
<td>POLYSILICON DEPOSITION (POLY I)</td>
</tr>
<tr>
<td>21.</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>22.</td>
<td>PATTERN POLYSILICON</td>
</tr>
<tr>
<td>23.</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>24.</td>
<td>ETCH POLYSILICON</td>
</tr>
<tr>
<td></td>
<td>(MASK #1)</td>
</tr>
<tr>
<td></td>
<td>(MASK #2)</td>
</tr>
<tr>
<td></td>
<td>(MASK #A1)</td>
</tr>
<tr>
<td></td>
<td>(MASK #3)</td>
</tr>
</tbody>
</table>
N-well Mask
N-well Mask
Detailed Description of First Photolithographic Steps Only

- Top View
- Cross-Section View
Will use positive photoresist (exposed region soluble in developer)
<table>
<thead>
<tr>
<th>Step</th>
<th>Action</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Clean wafer</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>GROW THIN OXIDE</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PATTERN n-well</td>
<td>(MASK #1)</td>
</tr>
<tr>
<td>5</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Deposit and diffus n-type impurities</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Grow thin oxide</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Apply layer of Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>PATTERN Si$_3$N$_4$ (active area definition)</td>
<td>(MASK #2)</td>
</tr>
<tr>
<td>13</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Etch Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>A.1</td>
<td>Optional field threshold voltage adjust</td>
<td></td>
</tr>
<tr>
<td>A.2</td>
<td>PATTERN ANTIMOAT IN SUBSTRATE</td>
<td>(MASK #A1)</td>
</tr>
<tr>
<td>A.3</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>A.4</td>
<td>FIELD IMPLANT p-type</td>
<td></td>
</tr>
<tr>
<td>A.5</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>GROW FIELD OXIDE</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Strip Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>GROW GATE OXIDE</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>POLYSILICON DEPOSITION (POLY I)</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>PATTERN POLYSILICON</td>
<td>(MASK #3)</td>
</tr>
<tr>
<td>23</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>ETCH POLYSILICON</td>
<td></td>
</tr>
</tbody>
</table>
Active Mask
Active Mask

Field Oxide

A-A’ Section

Field Oxide

Field Oxide

B-B’ Section
<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Mask</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Clean wafer</td>
<td></td>
</tr>
<tr>
<td>2.</td>
<td>GROW THIN OXIDE</td>
<td></td>
</tr>
<tr>
<td>3.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td>PATTERN n-well</td>
<td>MASK #1</td>
</tr>
<tr>
<td>5.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>6.</td>
<td>Deposit and diffus n-type impurities</td>
<td></td>
</tr>
<tr>
<td>7.</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>8.</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>9.</td>
<td>Grow thin oxide</td>
<td></td>
</tr>
<tr>
<td>10.</td>
<td>Apply layer of Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>11.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>12.</td>
<td>PATTERN Si$_3$N$_4$ (active area definition)</td>
<td>MASK #2</td>
</tr>
<tr>
<td>13.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>14.</td>
<td>Etch Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>15.</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Optional field threshold voltage adjust</td>
<td></td>
</tr>
<tr>
<td>A.1</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>A.2</td>
<td>PATTERN ANTIMOAT IN SUBSTRATE</td>
<td>MASK #A1</td>
</tr>
<tr>
<td>A.3</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>A.4</td>
<td>FIELD IMPLANT p-type</td>
<td></td>
</tr>
<tr>
<td>A.5</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>16.</td>
<td>GROW FIELD OXIDE</td>
<td></td>
</tr>
<tr>
<td>17.</td>
<td>Strip Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>18.</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>19.</td>
<td>GROW GATE OXIDE</td>
<td></td>
</tr>
<tr>
<td>20.</td>
<td>POLYSILICON DEPOSITION (POLY I)</td>
<td></td>
</tr>
<tr>
<td>21.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>22.</td>
<td>PATTERN POLYSILICON</td>
<td></td>
</tr>
<tr>
<td>23.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>24.</td>
<td>ETCH POLYSILICON</td>
<td>MASK #3</td>
</tr>
</tbody>
</table>
Poly plays a key role in all four types of devices!
Poly 1 Mask

A-A’ Section

Gate Oxide

B-B’ Section

Gate Oxide
TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process

<table>
<thead>
<tr>
<th>Step</th>
<th>Process Description</th>
<th>Mask</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Clean wafer</td>
<td></td>
</tr>
<tr>
<td>2.</td>
<td>GROW THIN OXIDE</td>
<td></td>
</tr>
<tr>
<td>3.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td>PATTERN n-well</td>
<td>(MASK #1)</td>
</tr>
<tr>
<td>5.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>6.</td>
<td>Deposit and diffus n-type impurities</td>
<td></td>
</tr>
<tr>
<td>7.</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>8.</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>9.</td>
<td>Grow thin oxide</td>
<td></td>
</tr>
<tr>
<td>10.</td>
<td>Apply layer of Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>11.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>12.</td>
<td>PATTERN Si$_3$N$_4$ (active area definition)</td>
<td>(MASK #2)</td>
</tr>
<tr>
<td>13.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>14.</td>
<td>Etch Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>15.</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td></td>
<td><strong>Optional field threshold voltage adjust</strong></td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.1 Apply photoresist</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.2 PATTERN ANTIMOAT IN SUBSTRATE</td>
<td>(MASK #A1)</td>
</tr>
<tr>
<td></td>
<td>A.3 Develop photoresist</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.4 FIELD IMPLANT p-type</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.5 Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>16.</td>
<td>GROW FIELD OXIDE</td>
<td></td>
</tr>
<tr>
<td>17.</td>
<td>Strip Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>18.</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>19.</td>
<td>GROW GATE OXIDE</td>
<td></td>
</tr>
<tr>
<td>20.</td>
<td>POLYSILICON DEPOSITION (POLY I)</td>
<td></td>
</tr>
<tr>
<td>21.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>22.</td>
<td>PATTERN POLYSILICON</td>
<td>(MASK #3)</td>
</tr>
<tr>
<td>23.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>24.</td>
<td>ETCH POLYSILICON</td>
<td></td>
</tr>
</tbody>
</table>
25. Strip photoresist

Optional steps for double polysilicon process

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist

27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P^+ GUARD RINGS (p-well ohmic contacts) (MASK #4)

28. Develop photoresist

29. p^+ IMPLANT

30. Strip photoresist

31. Apply photoresist

32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N^+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)

33. Develop photoresist

34. n^+ IMPLANT

35. Strip photoresist

36. Strip thin oxide

37. Grow oxide

38. Apply photoresist

39. PATTERN CONTACT OPENINGS (MASK #6)

40. Develop photoresist

41. Etch oxide

42. Strip photoresist
Poly 2 Mask
Poly 2 Mask

A-A’ Section

B-B’ Section
<table>
<thead>
<tr>
<th></th>
<th>Process scenario of major process steps in typical n-well CMOS process$^a$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Clean wafer</td>
</tr>
<tr>
<td>2.</td>
<td>GROW THIN OXIDE</td>
</tr>
<tr>
<td>3.</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>4.</td>
<td>PATTERN n-well (MASK #1)</td>
</tr>
<tr>
<td>5.</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>6.</td>
<td>Deposit and diffus n-type impurities</td>
</tr>
<tr>
<td>7.</td>
<td>Strip photoresist</td>
</tr>
<tr>
<td>8.</td>
<td>Strip thin oxide</td>
</tr>
<tr>
<td>9.</td>
<td>Grow thin oxide</td>
</tr>
<tr>
<td>10.</td>
<td>Apply layer of Si$_3$N$_4$</td>
</tr>
<tr>
<td>11.</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>12.</td>
<td>PATTERN Si$_3$N$_4$ (active area definition) (MASK #2)</td>
</tr>
<tr>
<td>13.</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>14.</td>
<td>Etch Si$_3$N$_4$</td>
</tr>
<tr>
<td>15.</td>
<td>Strip photoresist</td>
</tr>
<tr>
<td></td>
<td>Optional field threshold voltage adjust</td>
</tr>
<tr>
<td>A.1</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>A.2</td>
<td>PATTERN ANTIMOAT IN SUBSTRATE (MASK #A1)</td>
</tr>
<tr>
<td>A.3</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>A.4</td>
<td>FIELD IMPLANT p-type</td>
</tr>
<tr>
<td>A.5</td>
<td>Strip photoresist</td>
</tr>
<tr>
<td>16.</td>
<td>GROW FIELD OXIDE</td>
</tr>
<tr>
<td>17.</td>
<td>Strip Si$_3$N$_4$</td>
</tr>
<tr>
<td>18.</td>
<td>Strip thin oxide</td>
</tr>
<tr>
<td>19.</td>
<td>GROW GATE OXIDE</td>
</tr>
<tr>
<td>20.</td>
<td>POLYSILICON DEPOSITION (POLY I) (MASK #3)</td>
</tr>
<tr>
<td>21.</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>22.</td>
<td>PATTERN POLYSILICON</td>
</tr>
<tr>
<td>23.</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>24.</td>
<td>ETCH POLYSILICON</td>
</tr>
</tbody>
</table>
25. Strip photoresist

*Optional steps for double polysilicon process*

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON (MASK #B1)
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist

27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P⁺ GUARD RINGS (p-well ohmic contacts) (MASK #4)

28. Develop photoresist

29. p⁺ IMPLANT

30. Strip photoresist

31. Apply photoresist

32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N⁺ GUARD RINGS (top ohmic contact to substrate) (MASK #5)

33. Develop photoresist

34. n⁺ IMPLANT

35. Strip photoresist

36. Strip thin oxide

37. Grow oxide

38. Apply photoresist

39. PATTERN CONTACT OPENINGS (MASK #6)

40. Develop photoresist

41. Etch oxide

42. Strip photoresist
P-Select
P-Select
P-Select Mask – p-diffusion

Note the gate is self aligned !!
n-Select Mask – n-diffusion

A-A’ Section

B-B’ Section

n-diffusion
### TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Clean wafer</td>
</tr>
<tr>
<td>2.</td>
<td>GROW THIN OXIDE</td>
</tr>
<tr>
<td>3.</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>4.</td>
<td>PATTERN n-well</td>
</tr>
<tr>
<td>5.</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>6.</td>
<td>Deposit and diffus n-type impurities</td>
</tr>
<tr>
<td>7.</td>
<td>Strip photoresist</td>
</tr>
<tr>
<td>8.</td>
<td>Strip thin oxide</td>
</tr>
<tr>
<td>9.</td>
<td>Grow thin oxide</td>
</tr>
<tr>
<td>10.</td>
<td>Apply layer of Si$_3$N$_4$</td>
</tr>
<tr>
<td>11.</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>12.</td>
<td>PATTERN Si$_3$N$_4$ (active area definition)</td>
</tr>
<tr>
<td>13.</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>14.</td>
<td>Etch Si$_3$N$_4$</td>
</tr>
<tr>
<td>15.</td>
<td>Strip photoresist</td>
</tr>
<tr>
<td>16.</td>
<td>GROW FIELD OXIDE</td>
</tr>
<tr>
<td>17.</td>
<td>Strip Si$_3$N$_4$</td>
</tr>
<tr>
<td>18.</td>
<td>Strip thin oxide</td>
</tr>
<tr>
<td>19.</td>
<td>GROW GATE OXIDE</td>
</tr>
<tr>
<td>20.</td>
<td>POLYSILICON DEPOSITION (POLY I)</td>
</tr>
<tr>
<td>21.</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>22.</td>
<td>PATTERN POLYSILICON</td>
</tr>
<tr>
<td>23.</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>24.</td>
<td>ETCH POLYSILICON</td>
</tr>
</tbody>
</table>
25. Strip photoresist
   *Optional steps for double polysilicon process*
   B.1 Strip thin oxide
   B.2 GROW THIN OXIDE
   B.3 POLYSILICON DEPOSITION (POLY II)
   B.4 Apply photoresist
   B.5 PATTERN POLYSILICON (MASK #B1)
   B.6 Develop photoresist
   B.7 ETCH POLYSILICON
   B.8 Strip photoresist
   B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. P+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. N+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL
46. Develop photoresist
47. Etch metal
48. Strip photoresist
   Optional steps for double metal process
   C.1 Strip thin oxide
   C.2 DEPOSIT INTERMETAL OXIDE
   C.3 Apply photoresist
   C.4 PATTERN VIAS
   C.5 Develop photoresist
   C.6 Etch oxide
   C.7 Strip photoresist
   C.8 APPLY METAL (Metal 2)
   C.9 Apply photoresist
   C.10 PATTERN METAL
   C.11 Develop photoresist
   C.12 Etch metal
   C.13 Strip photoresist
49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST
<table>
<thead>
<tr>
<th>Step</th>
<th>Process Activity</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Clean wafer</td>
<td></td>
</tr>
<tr>
<td>2.</td>
<td><strong>GROW THIN OXIDE</strong></td>
<td></td>
</tr>
<tr>
<td>3.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td><strong>PATTERN n-well</strong></td>
<td><em>(MASK #1)</em></td>
</tr>
<tr>
<td>5.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>6.</td>
<td>Deposit and diffus n-type impurities</td>
<td></td>
</tr>
<tr>
<td>7.</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>8.</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>9.</td>
<td>Grow thin oxide</td>
<td></td>
</tr>
<tr>
<td>10.</td>
<td>Apply layer of Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>11.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>12.</td>
<td><strong>PATTERN Si$_3$N$_4$</strong> (active area definition)</td>
<td><em>(MASK #2)</em></td>
</tr>
<tr>
<td>13.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>14.</td>
<td>Etch Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>15.</td>
<td>Strip photoresist</td>
<td><strong>Optional field threshold voltage adjust</strong></td>
</tr>
<tr>
<td></td>
<td></td>
<td>A.1 Apply photoresist</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A.2 <strong>PATTERN ANTIMOAT IN SUBSTRATE</strong> <em>(MASK #A1)</em></td>
</tr>
<tr>
<td></td>
<td></td>
<td>A.3 Develop photoresist</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A.4 FIELD IMPLANT p-type</td>
</tr>
<tr>
<td></td>
<td></td>
<td>A.5 Strip photoresist</td>
</tr>
<tr>
<td>16.</td>
<td><strong>GROW FIELD OXIDE</strong></td>
<td></td>
</tr>
<tr>
<td>17.</td>
<td>Strip Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>18.</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>19.</td>
<td><strong>GROW GATE OXIDE</strong></td>
<td></td>
</tr>
<tr>
<td>20.</td>
<td><strong>POLYSILICON DEPOSITION (POLY I)</strong></td>
<td><em>(MASK #3)</em></td>
</tr>
<tr>
<td>21.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>22.</td>
<td><strong>PATTERN POLYSILICON</strong></td>
<td><em>(MASK #3)</em></td>
</tr>
<tr>
<td>23.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>24.</td>
<td><strong>ETCH POLYSILICON</strong></td>
<td></td>
</tr>
</tbody>
</table>
25. Strip photoresist
   *Optional steps for double polysilicon process*
   B.1 Strip thin oxide
   B.2 GROW THIN OXIDE
   B.3 POLYSILICON DEPOSITION (POLY II)
   B.4 Apply photoresist
   B.5 PATTERN POLYSILICON (MASK #B1)
   B.6 Develop photoresist
   B.7 ETCH POLYSILICON
   B.8 Strip photoresist
   B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL
46. Develop photoresist
47. Etch metal
48. Strip photoresist
   
   Optional steps for double metal process
   C.1 Strip thin oxide
   C.2 DEPOSIT INTERMETAL OXIDE
   C.3 Apply photoresist
   C.4 PATTERN VIAS
   C.5 Develop photoresist
   C.6 Etch oxide
   C.7 Strip photoresist
   C.8 APPLY METAL (Metal 2)
   C.9 Apply photoresist
   C.10 PATTERN METAL
   C.11 Develop photoresist
   C.12 Etch metal
   C.13 Strip photoresist
49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST

(MASK #7)

(MASK #C1)

(MASK #C2)

(MASK #8)
A capacitor

B' resistor

P-channel MOSFET

B n-channel MOSFET
End of Lecture 15