EE 330
Lecture 16

Model Relationships
CMOS Process Flow
Quiz 13  Determine the current $I_D$ for the following circuit. Assume the MOS transistor can be modeled by the basic square-law model with parameters $V_T=0.8\,\text{V}$, $\mu C_{Ox}=100 \, \mu \text{A/V}^2$ and $C_{ox}=4 \, \text{fF/\mu}^2$ and the device has dimensions $W=10\mu$ and $L=2\mu$. 
And the number is ....
And the number is .... 3
Quiz 13 Determine the current $I_D$ for the following circuit. Assume the MOS transistor can be modeled by the basic square-law model with parameters $V_T=0.8V$, $\mu C_{OX}=100\mu A/V^2$ and $C_{OX}=4fF/\mu^2$ and the device has dimensions $W=10\mu$ and $L=2\mu$.

Solution:
1. Guess the device is operating in the **Saturation Region**
2. Analyze the circuit with the device in this region
3. Verify region of operation
4. Repeat steps 1-3 if guess was not correct
Quiz 13 Determine the current $I_D$ for the following circuit. Assume the MOS transistor can be modeled by the basic square-law model with parameters $V_T=0.8\text{V}$, $\mu C_{\text{OX}}=100\mu\text{A/V}^2$ and $C_{\text{OX}}=4\text{fF/}\mu^2$ and the device has dimensions $W=10\mu$ and $L=2\mu$.

Solution:

2. Analyze the circuit with the device in this region

$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{\text{OX}} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\ \mu C_{\text{OX}} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T \end{cases}$$
Quiz 13 Determine the current $I_D$ for the following circuit. Assume the MOS transistor can be modeled by the basic square-law model with parameters $V_T=0.8V$, $\mu C_{OX}=100\mu A/V^2$ and $C_{OX}=4fF/\mu^2$ and the device has dimensions $W=10\mu$ and $L=2\mu$.

Solution:

2. Analyze the circuit with the device in this region

$$I_D = \mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2$$

$$= 10^{-4} \times \frac{10}{2 \times 2} (1.5 - 0.8)^2$$

$$I_D = 123\mu A$$

3. Verify region of operation

$$V_{GS} \geq ? V_T$$

$$V_{DS} > ? V_{GS} - V_T$$

$$1.5V > 0.8V$$

$$3V > 1.5V - 0.8V$$

Verifies!
Review from Last Time

n-Channel MOSFET Operation and Model

Increase $V_{DS}$ even more

Inversion layer disappears near drain

Termed “saturation” region of operation

Saturation first occurs when $V_{DS} = V_{GS} - V_T$

$I_D = ?$

$I_G = 0$

$I_B = 0$
Graphical Interpretation of MOS Model

Review from Last Time

Graphical representation of the MOS model showing different regions:
- **Triode** region
- **Saturation** region
- **Cutoff** region

Mathematical equations for the drain current $I_D$ are given as:

$$I_D = \begin{cases} 
0 & \text{for } V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{for } V_{GS} \geq V_T, \ V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 & \text{for } V_{GS} \geq V_T, \ V_{DS} \geq V_{GS} - V_T
\end{cases}$$
Square-Law Model

\[ I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T
\end{cases} \]
Switch-Level Models

Switch-level model including gate capacitance and drain resistance

$C_{GS}$ and $R_{SW}$ dependent upon device sizes and process

For minimum-sized devices in a 0.5u process

$C_{GS} \approx 1.5fF$ \quad $R_{SW} \approx \begin{cases} 2K\Omega & \text{n-channel} \\ 6K\Omega & \text{p-channel} \end{cases}$

Considerable emphasis will be placed upon device sizing to manage $C_{GS}$ and $R_{SW}$
Extended Square-Law Model

\[ I_G = 0 \]
\[ I_B = 0 \]

\[ I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 \cdot (1 + \lambda V_{DS}) & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T 
\end{cases} \]

\[ V_T = V_{T0} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right) \]

Model Parameters : \{\mu, C_{OX}, V_{T0}, \phi, \gamma, \lambda\}

Design Parameters : \{W, L\} but only one degree of freedom \( W/L \)
Short-Channel Model

\[
I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^{\alpha} V_{DS} & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} < \theta_1 (V_{GS} - V_T)^{\alpha} \\
\theta_2 \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^{\alpha} & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} \geq \theta_1 (V_{GS} - V_T)^{\alpha} 
\end{cases}
\]

\(\alpha\) is the velocity saturation index, \(2 \geq \alpha \geq 1\)

Channel length modulation (\(\lambda\)) and bulk effects can be added to the velocity Saturation as well.
BSIM model

.MODEL CMOSN NMOS (LEVEL = 49)
+VERSION = 3.1
+XJ = 1.5E-7
+K1 = 0.8976376
+K3B = -8.2369696
+DVTOW = 0
+DVT0 = 2.7123969
+U0 = 451.2322004
+UC = 1.22401E-11
+AGS = -0.130484
+KETA = -3.043349E-3
+RDSW = 1.367055E3
+WR = 1
+XL = 1E-7
+DWB = 3.676235E-8
+VREF = -1.493030E-4
+CDSC = 2.4E-4
+CDSCB = 0
+PCLM = 2.5941582
+PSCBE1 = 6.611774E8
+PRT = 0
+KT1L = 0
+UB1 = -7.61E-10
+WL = 0
+WPN = 1
+ILN = 1
+LWL = 2
+CGDO = 2.32E-10
+CJ = 4.282017E-4
+CJSW = 3.034055E-10
+CF = 0
+FK2 = -0.0289036

*
BSIM Binning Model
- multiple BSIM models!

.MODEL CMOSN NMOS (
+VERSION = 3.1  TNOM = 27  LEVEL = 49
+XJ = 1.5E-7  NCH = 1.7E17  TOX = 1.42E-8
+K1 = 0.8976376  K2 = -0.09255  VTH0 = 0.629035
+K3B = -8.2369696  W0 = 1.041146E-8  K3 = 24.0984767
+DVTOW = 0  DVT1W = 0  NLX = 1E-9
+DVT0 = 2.7123969  DVT1 = 0.4232931  DVT2 = -0.1403765
+U0 = 451.2322004  UA = 3.091785E-13  UB = 1.702517E-18
+UC = 1.22401E-11  VSAT = 1.715884E5  A0 = 0.6580918
+AGS = -0.130484  B0 = 2.446405E-6  B1 = 5E-6
+KETA = -3.043349E-3  A1 = 8.18159E-7  A2 = 0.3363058
+RDSW = 1.367055E3  PRWG = 0.0328586  PRWB = 0.0104806
+WR = 1  WINT = 2.443677E-7  LINT = 6.999776E-8
+XL = 1E-7  XW = 0  DWG = -1.256454E-8
+DWB = 3.676235E-8  VOFF = -1.49303E-4  NFACTOR = 1.0354201
+CI = 0  CDSC = 2.4E-4  CDSCD = 0
+CDSCB = 0  ETA0 = 2.342963E-3  ETAB = -1.5324E-4
+DSCB = 0.0764123  PCLM = 2.5941582  PDIBLC1 = 0.8187825
+PDIBLC2 = 2.366707E-3  PDIBLCB = -0.0431505  DROUT = 0.9919348
+PSCEB1 = 6.611774E8  PSCEB2 = 3.238266E-4  PVAG = 0
+FRT = 0  UTE = -1.5  KT1 = -0.11
+KTI1L = 0  KT2 = 0.022  UAI1 = 4.31E-9
+UB1 = -7.61E-10  UC1 = -5.6E-11  AT = 3.3E4
+WL = 0  WLN = 1  WW = 0
+WNN = 1  WWL = 0  LL = 0
+LNN = 1  LW = 0  LWN = 1
+LWL = 0  CAPMOD = 2  XPART = 0.5
+CGDO = 2.32E-10  CGSO = 2.32E-10  CGBO = 1E-9
+CJ = 4.282017E-4  PB = 0.9317787  MJ = 0.4495867
+CJSW = 3.034055E-10  PBSW = 0.8  MJSW = 0.1713852
+CJSWG = 1.64E-10  PBSWG = 0.8  MJSWG = 0.1713852
+CF = 0  PVTH0 = 0.0520855  PRDSW = 112.8875816
+FK2 = -0.0289036  WKETA = -0.0237483  LKETA = 1.728324E-3 )
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an n-channel MOSFET from square-law model
In the 0.5µ CMOS process if $L=1µ$, $W=1µ$

(Assume $\mu C_{OX}=100µAV^{-2}$, $C_{OX}=2.5fFu^{-2}$, $V_{T0}=1V$, $V_{DD}=3.5V$, $V_{SS}=0$)

$$I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) & \text{if } V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\frac{W}{2L} \left( V_{GS} - V_T \right)^2 & \text{if } V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases}$$

When SW is on, operation is “deep” triode
**Model Relationships**

Determine $R_{SW}$ and $C_{GS}$ for an n-channel MOSFET from square-law model in the 0.5u CMOS process if $L=1u$, $W=1u$

(Assume $\mu C_{OX}=100\mu AV^{-2}$, $C_{OX}=2.5fF u^{-2}$, $V_{T0}=1V$, $V_{DD}=3.5V$, $V_{SS}=0$)

\[
I_D = \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \mu C_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS}
\]

\[
R_{SO} = \left. \frac{V_{DS}}{I_D} \right|_{V_{GS}=V_{oo}} = \frac{1}{\mu C_{OX} \frac{W}{L} (V_{GS} - V_T)} \bigg|_{V_{GS}=3.5V} = \frac{1}{(E-4)(\frac{1}{1})(3.5-1)} = 4K\Omega
\]

$C_{GS} = C_{OX}WL = (2.5fF u^{-2})(1u^2) = 2.5fF$
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an p-channel MOSFET from square-law model
In the 0.5u CMOS process if $L=1u, W=1u$

\[
(C_{OX}=2.5fF/u^2, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0)
\]

Observe $\mu_n \approx 3$

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T
\end{cases}
\]

When SW is on, operation is “deep” triode
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an p-channel MOSFET from square-law model
In the 0.5u CMOS process if $L=1\mu$, $W=1\mu$

$$ C_{OX}=2.5fF\mu^{-2}, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0 $$

Observe $\mu_n \mu_p \approx 3$

$$ I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{ox} \frac{W}{L} (V_{GS} - V_T - \frac{V_{DS}}{2}) V_{DS} & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T \end{cases} $$

When SW is on, operation is “deep” triode
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an p-channel MOSFET from square-law model
In the 0.5u CMOS process if $L=1u$, $W=1u$

$\left(C_{OX}=2.5fF\mu^{-2}, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0\right)$

Observe $\mu_n/\mu_p\approx3$

$I_D = \mu_p C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \mu_p C_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS}$

$R_{SQ} = \left. \frac{V_{DS}}{I_D} \right|_{V_{gs}=V_{bd}} = \left. \frac{1}{\mu_p C_{OX} \frac{W}{L} (V_{GS} - V_T)} \right|_{V_{gs}=3.5V}$

$= \frac{1}{\left(\frac{1}{3}E - 4\right) \left(\frac{1}{1}\right) (3.5 - 1)} = 12 K\Omega$

$C_{GS}= C_{OX}WL = (2.5fF\mu^{-2})(1\mu^2) = 2.5fF$

Observe the resistance of the p-channel device is approximately 3 times larger than that of the n-channel device for same bias and dimensions!
Modeling of the MOSFET

goal: Obtain a mathematical relationship between the port variables of a device.

\[
\begin{align*}
I_D &= f_1(V_{GS}, V_{DS}, V_{BS}) \\
I_G &= f_2(V_{GS}, V_{DS}, V_{BS}) \\
I_B &= f_3(V_{GS}, V_{DS}, V_{BS})
\end{align*}
\]
Small-Signal Model

Goal with small signal model is to predict performance of circuit or device in the vicinity of an operating point

Operating point is often termed Q-point
Small-Signal Model

\[ x \rightarrow \begin{array}{c}
\text{Q-point} \\
X_Q \\
\text{Y_Q}
\end{array} \]
Technology Files

• Design Rules

• Process Flow (Fabrication Technology) (will discussion next)

• Model Parameters (will discuss in substantially more detail after device operation and more advanced models are introduced)
TABLE 2B.1
Process scenario of major process steps in typical p-well CMOS processa

<table>
<thead>
<tr>
<th>Step</th>
<th>Description</th>
<th>Mask</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Clean wafer</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>GROW THIN OXIDE</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>PATTERN P-WELL (MASK #1)</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Deposit and diffuse p-type impurities</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>Grow thin oxide</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>Apply layer of Si₃N₄</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>12</td>
<td>PATTERN Si₃N₄ (active area definition)</td>
<td>(MASK #2)</td>
</tr>
<tr>
<td>13</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>Etch Si₃N₄</td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Optional field threshold voltage adjust</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.1 Apply photoresist</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.2 PATTERN ANTIMOAT IN SUBSTRATE (MASK #A1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.3 Develop photoresist</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.4 FIELD IMPLANT (n-type)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>A.5 Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>GROW FIELD OXIDE</td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>Strip Si₃N₄</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>GROW GATE OXIDE</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>POLYSILICON DEPOSITION (POLY I)</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>22</td>
<td>PATTERN POLYSILICON (MASK #3)</td>
<td></td>
</tr>
<tr>
<td>23</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>24</td>
<td>ETCH POLYSILICON</td>
<td></td>
</tr>
</tbody>
</table>

This table discusses a p-well process flow, an n-well process flow is actually used in the following set of slides with straightforward modifications of this process flow.
25. Strip photoresist

*Optional steps for double polysilicon process*

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist:
B.5 PATTERN POLYSILICON
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist

27. PATTERN P-CHANNEL DRAINS AND SOURCES AND
   P⁺ GUARD RINGS (p-well ohmic contacts) (MASK #4)

28. Develop photoresist

29. p⁺ IMPLANT

30. Strip photoresist

31. Apply photoresist

32. PATTERN N-CHANNEL DRAINS AND SOURCES AND
   N⁺ GUARD RINGS (top ohmic contact to substrate) (MASK #5)

33. Develop photoresist

34. n⁺ IMPLANT

35. Strip photoresist

36. Strip thin oxide

37. Grow oxide

38. Apply photoresist

39. PATTERN CONTACT OPENINGS (MASK #6)

40. Develop photoresist

41. Etch oxide

42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL  (MASK #7)
46. Develop photoresist
47. Etch metal
48. Strip photoresist
  Optional steps for double metal process
  C.1 Strip thin oxide
  C.2 DEPOSIT INTERMETAL OXIDE
  C.3 Apply photoresist
  C.4 PATTERN VIAS  (MASK #C1)
  C.5 Develop photoresist
  C.6 Etch oxide
  C.7 Strip photoresist
  C.8 APPLY METAL (Metal 2)  (MASK #C2)
  C.9 Apply photoresist
  C.10 PATTERN METAL
  C.11 Develop photoresist
  C.12 Etch metal
  C.13 Strip photoresist
49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS  (MASK #8)
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST
Bulk CMOS Process Description

- n-well process
- Single Metal Only Depicted
- Double Poly
Components Shown

• n-channel MOSFET
• p-channel MOSFET
• Poly Resistor
• Doubly Poly Capacitor
Consider Basic Components Only

Well Contacts and Guard Rings Will be Discussed Later
n-channel MOSFET
n-channel MOSFET
Capacitor
p-channel MOSFET
Resistor
N-well Mask

A

A'

B

B'

[Diagram of N-well Mask with annotations A, A', B, B']
N-well Mask
Detailed Description of First Photolithographic Steps Only

- Top View
- Cross-Section View
Develop

A-A’ Section

B-B’ Section

Photoresist

N-well Mask

Exposure

Develop
Active Mask
Poly1 Mask
Poly 2 Mask

A-A’ Section

B-B’ Section
P-Select
P-Select Mask – n-diffusion

A-A’ Section

B-B’ Section

n-diffusion
P-Select Mask – p-diffusion

A-A’ Section

B-B’ Section

g-diffusion
Contact Mask
That’s all folks!