EE 330
Lecture 16

MOS Transistor Models
CMOS Process Flow
Graphical Interpretation of MOS Model

$$I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T \text{ and } V_{DS} < V_{GS} - V_T \\ \mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T \end{cases}$$

- **Cutoff**: $V_{GS} \leq V_T$
- **Saturation**: $V_{GS} \geq V_T \text{ and } V_{DS} < V_{GS} - V_T$
- **Triode**: $V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T$
Review from Last Time

Model Extensions

Existing Model

Slope is not 0
Typical Effects of Bulk on Threshold Voltage for n-channel Device

$$V_T = V_{T0} + \gamma \left( \sqrt{\phi} - V_{BS} - \sqrt{\phi} \right)$$

\( \gamma \approx 0.4V^{\frac{1}{2}} \) \( \phi \approx 0.6V \)

Bulk-Diffusion Generally Reverse Biased \((V_{BS} < 0 \text{ or at least } -0.3V)\) for n-channel
Shift in threshold voltage with bulk voltage can be substantial
Often \( V_{BS} = 0 \)
Model Extension Summary

\[ I_G = 0 \]
\[ I_B = 0 \]

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} > V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 \cdot (1 + \lambda V_{DS}) & V_{GS} > V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases}
\]

\[ V_T = V_{T0} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right) \]

Model Parameters : \{\mu, C_{OX}, V_{T0}, \phi, \gamma, \lambda\}

Design Parameters : \{W,L\} but only one degree of freedom W/L
Model Extension (short devices)

\[
I_D = \begin{cases} 
0 & V_{gs} \leq V_T \\
\frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)^{\alpha} V_{ds} & V_{gs} \geq V_T \quad V_{ds} < \theta_1 (V_{gs} - V_T)^{\alpha} \\
\theta_2 \mu C_{ox} \frac{W}{L} (V_{gs} - V_T)^{\alpha} & V_{gs} \geq V_T \quad V_{ds} \geq \theta_1 (V_{gs} - V_T)^{\alpha}
\end{cases}
\]

\(\alpha\) is the velocity saturation index, \(2 \geq \alpha \geq 1\)

No longer a square-law model (some term it an \(\alpha\)-power model)

For long devices, \(\alpha=2\)

Channel length modulation (\(\lambda\)) and bulk effects can be added to the velocity Saturation as well

Degrading of \(\alpha\) is not an attractive limitation of the MOSFET
Review from Last Time

Model Extension (BSIM model)

```plaintext
.MODEL CMOSN NMOS (LEVEL = 49
+VERSION = 3.1
+KJ = 1.5E-7
+K1 = 0.8976376
+K3B = -8.2369696
+DVTOW = 0
+DVT0 = 2.7123969
+U0 = 451.2322004
+UC = 1.22401E-11
+AGS = -0.130484
+KETA = -3.043349E-3
+RDSW = 1.367055E3
+WR = 1
+XL = 1E-7
+DWB = 3.676235E-8
+CIT = 0
+CDSCB = 0
+DSUB = 0.0764123
+PDBLC2 = 2.366707E-3
+PSCBE1 = 6.611774E8
+FRT = 0
+KT1L = 0
+UB1 = -7.61E-18
+WL = 0
+WNN = 1
+ILN = 1
+LWL = 0
+CGDO = 2.32E-10
+CJ = 4.282017E-4
+CJSSW = 3.034055E-10
+CJSWG = 1.64E-10
+CF = 0
+FK2 = -0.0289036
+VTH0 = 0.629035
+K2 = -0.09255
+W0 = 1.041146E-8
+UA = 3.091785E-13
+VSAT = 1.715884E5
+Bo = 2.446405E-6
+A1 = 8.18159E-7
+PRWG = 0.0328586
+WINT = 2.443677E-7
+PLM = 2.5941582
+PRWB = 0.0104806
+LINT = 6.999776E-8
+PB = 0.9317787
+PSBL = 0.8
+PSW = 0.8
+FVTH0 = 0.0520655
+WKETA = -0.0237483
+LKETA = 1.728324E-3
)
```
Model Extension (BSIM model)

Binning Models - multiple BSIM models!

```
.MOdel CMOSN NMOS (LEVEL = 49)
+VERSION = 3.1
+XJ = 1.5E-7
+KJ = 0.8976376
+K3B = -8.2369696
+DVTOW = 0
+DVT0 = 2.7123969
+U0 = 451.2322004
+UC = 1.22401E-11
+AGS = -0.130484
+KETA = -3.043349E-3
+RDSW = 1.367055E3
+W = 1
+XL = 1E-7
+DW = 3.676235E-8
+CIT = 0
+CDSCB = 0
+DSUB = 0.0764123
+PDIBLC2 = 2.366707E-3
+PSCE = 6.611774E8
+FRT = 0
+KT1L = 0
+UB1 = -7.618E-18
+WLN = 0
+WLN = 1
+LNN = 1
+LWL = 0
+CGDO = 2.32E-10
+CJ = 4.282017E-4
+CJSW = 3.034055E-10
+CJSWG = 1.64E-10
+CF = 0
+FK2 = -0.0289036
+WK = 1
+VTH0 = 0.629035
+K1 = -0.09255
+W0 = 1.041146E-8
+K3 = 24.0984767
+VTH1 = 1E-9
+U = 3.091785E-13
+VSAT = 1.715884E5
+B0 = 2.446405E-6
+A1 = 8.18159E-7
+PRWB = 0.0104806
+WINT = 2.443677E-7
+LU = 1.702517E-18
+UB = 1.702517E-18
+UA = 451.2322004
+AO = 0.6580918
+B1 = 5E-6
+EB = -1.49303E-4
+CDSCD = 2.4E-4
+ETA0 = 2.342963E-3
+PCLM = 2.5941582
+PDIBLC1 = 0.8187825
+PDIBLCB = 0.0431505
+PSCE = 3.238265E-4
+PSCE2 = 3.238265E-4
+NACTOR = 1.0354201
+CPR = 0.018
+CPR = 0.018
+K1 = -0.11
+UA1 = 4.318E-9
+AT = 3.3E4
+WW = 0
+LL = 0
+LWN = 1
+XPART = 0.5
+CGBO = 1E-9
+PB = 0.9317787
+MJ = 0.4495867
+MJ = 0.4495867
+PBSW = 0.8
+MJSW = 0.1713582
+PBSWG = 0.8
+MJSWG = 0.1713582
+PVTH = 0.0520855
+FRDSW = 112.0675816
+LKETA = 1.728324E-3
*
```
How many models of the MOSFET do we have?

Switch-level model (2)

Square-law model (with $\lambda$ and bulk additions)

$\alpha$-law model (with $\lambda$ and bulk additions)

BSIM model (with binning extensions)
Model Status

- Simple dc Model
  - Square-Law Model
    - BSIM Model
      - Square-Law Model (with extensions for \( v \) \( y \) effects)
        - Short-Channel \( \alpha \)-law Model
          - Switch-Level Models
            - Ideal switches
            - \( R_{SW} \) and \( C_{GS} \)
  - Better Analytical dc Model
  - Sophisticated Model for Computer Simulations
- Small Signal
- Frequency Dependent Small Signal
- Simpler dc Model
Square-Law Model

\[
I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T, \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} > V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & \text{if } V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases}
\]
Switch-Level Models

Switch-level model including gate capacitance and drain resistance

C\textsubscript{GS} and R\textsubscript{SW} dependent upon device sizes and process

For minimum-sized devices in a 0.5\textmu m process

\[
C_{\text{GS}} \approx 1.5\text{fF} \quad R_{\text{SW}} \approx \begin{cases} 2\text{K}\Omega & \text{n-channel} \\ 6\text{K}\Omega & \text{p-channel} \end{cases}
\]

Considerable emphasis will be placed upon device sizing to manage C\textsubscript{GS} and R\textsubscript{SW}
Extended Square-Law Model

\[ I_G = 0 \]
\[ I_B = 0 \]

\[ I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 \bullet (1 + \lambda V_{DS}) & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases} \]

\[ V_T = V_{T0} + \gamma \left( \sqrt{\phi - V_{BS}} - \sqrt{\phi} \right) \]

Model Parameters : \{\mu, C_{ox}, V_{T0}, \phi, \gamma, \lambda\}

Design Parameters : \{W, L\}  but only one degree of freedom \( W/L \)
Short-Channel Model

\[
I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^{\alpha} V_{DS} & \text{if } V_{GS} \geq V_T, \ V_{DS} < \theta_1 (V_{GS} - V_T)^{\frac{\alpha}{2}} \\
\theta_2 \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^{\alpha} & \text{if } V_{GS} \geq V_T, \ V_{DS} \geq \theta_1 (V_{GS} - V_T)^{\frac{\alpha}{2}} 
\end{cases}
\]

\[\alpha \text{ is the velocity saturation index, } 2 \geq \alpha \geq 1\]

Channel length modulation (\(\lambda\)) and bulk effects can be added to the velocity Saturation as well.
.MODEL CMOSN NMOS 
+VERSION = 3.1
+LEVEL = 49
+TNOM = 27
+TOX = 1.42E-8
+KJ = 1.5E-7
+NCH = 1.7E17
+VTH0 = 0.629035
+K1 = 0.8976376
+K2 = -0.09255
+K3 = 24.0984767
+W0 = 1.041146E-8
+K3B = -8.2369696
+NLX = 1E-9
+DVTO = 0
+DVT1W = 0
+DVT2W = 0
+DVT2 = -0.1403765
+UA = 3.091785E-13
+UB = 1.702517E-18
+VSAT = 1.715884E5
+A0 = 0.6580918
+AGS = 0.130484
+B0 = 2.446405E-6
+B1 = 5E-6
+KETA = -3.043349E-3
+A1 = 8.18159E-7
+A2 = 0.3363058
+RDSW = 1.367055E3
+FRWG = 0.0328386
+PRWB = 0.0104806
+WR = 1
+WINT = 2.443677E-7
+LINT = 6.999776E-8
+XL = 1E-7
+XW = 0
+DWG = -1.256454E-8
+VOFF = -1.493030E-4
+NFACOR = 1.0354201
+CSC = 2.4E-4
+CSDC = 0
+ETA0 = 2.342963E-3
+ETAB = -1.5324E-4
+PCLM = 2.5941582
+PDIBLC1 = 0.8187825
+PDIBLC2 = 2.366707E-3
+PDIBLCB = -0.0431505
+DROUT = 0.9919348
+PSCEB1 = 6.611774E8
+PSCEB2 = 3.238256E-4
+PVAR = 0
+FRT = 0
+KNT1 = 0
+K1T = 0.022
+UAI1 = 4.31E-9
+UBL = -7.61E-18
+UC1 = -5.6E-11
+AT = 3.3E4
+WLN = 1
+WW = 0
+WLN = 1
+LL = 0
+LWN = 1
+WLN = 0
+CAPMOD = 2
+XPART = 0.5
+CGDO = 2.32E-10
+CGSO = 2.32E-10
+CGBO = 1E-9
+PJ = 4.282017E-4
+PB = 0.9317787
+MJ = 0.4495867
+CSW = 3.034055E-10
+PBSW = 0.8
+MSW = 0.1713852
+CSWG = 1.64E-10
+PBSWG = 0.8
+MSWG = 0.1713852
+CF = 0
+VFTHO = 0.0520855
+FRDSW = 112.8675616
+FK2 = -0.0289036
+WKE = -0.0237483
+LKETA = 1.728324E-3

*
BSIM Binning Model
- multiple BSIM models!

.MODEL CMOSN NMOS (LEVEL = 49
+VERSION = 3.1 TNUM = 27 TOX = 1.42E-8
+XJ = 1.5E-7 NCH = 1.7E17 VTH0 = 0.629035
+K1 = 0.8976376 K2 = -0.09255 K3 = 24.0984767
+K3B = -8.2369696 W0 = 1.041146E-8 NLX = 1E-9
+DVTO 0 DVT1W = 0 DVT2W = 0
+DVTO = 2.7123969 DVT1 = 0.4232931 DVT2 = -0.1403765
+UG = 451.2322004 UA = 3.091785E-13 UB = 1.702517E-18
+UC = 1.22401E-11 VSAT = 1.715884E5 A0 = 0.6580918
+AGS = 0.130484 B0 = 2.446405E-6 B1 = 5E-6
+KETA = -3.043349E-3 A1 = 8.18159E-7 A2 = 0.3363058
+RDSW = 1.367055E3 PRWG = 0.0328586 PRWB = 0.0104806
+W1K = 1 WINT = 2.443677E-7 LINT = 6.999776E-8
+XL = 1E-7 XW = 0 DWG = -1.256454E-8
+DWB = 3.676235E-8 VOFF = -1.493033E-4 NFACTOR = 1.0354201
+SWSC = 0 CDSC = 2.4E-4 CDSCD = 0
+DSUSE = 0 ETA0 = 2.342963E-3 ETA = -1.5324E-4
+DSUB = 0.0764123 PCLM = 2.5941582 PDIBLC1 = 0.8187825
+PDIBLC2 = 2.366707E-3 PDIBLCB = -0.0431505 DROUT = 0.9919348
+PSCBE1 = 6.61774E8 PSCBE2 = 3.2382656E-4 PVAG = 0
+FRT = 0 UTE = -1.5 KT1 = -0.11
+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+W1 = 0 WLN = 1 WW = 0
+W1W = 1 WWL = 0 LL = 0
+ILW = 1 LW = 0 LWN = 1
+LWT = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 2.32E-10 CGSO = 2.32E-10 CGBO = 1E-9
+CJ = 4.282017E-4 PB = 0.9317787 MJ = 0.4495867
+CJSW = 3.034055E-10 PB5SW = 0.8 MJSW = 0.1713852
+CJSW = 1.64E-10 PB5SWG = 0.8 MJSWG = 0.1713852
+CF = 0 FVTH0 = 0.0520655 FRDSW = 112.8675816
+FK2 = -0.0289036 WKETA = -0.0237483 LKETA = 1.728324E-3 )
*
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an n-channel MOSFET from square-law model

In the 0.5μm CMOS process if $L=1μm$, $W=1μm$

(Assume $\mu C_{OX}=100μAV^{-2}$, $C_{OX}=2.5fFμ^{-2}$, $V_{T0}=1V$, $V_{DD}=3.5V$, $V_{SS}=0$)

$$I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{OX} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T
\end{cases}$$

when SW is on, operation is “deep” triode
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an n-channel MOSFET from square-law model

In the 0.5µ CMOS process if $L=1µ$, $W=1µ$

(Assume $\mu C_{OX}=100µAV^{-2}$, $C_{OX}=2.5fFµ^{-2}$, $V_{T0}=1V$, $V_{DD}=3.5V$, $V_{SS}=0$)

\[ I_D = \mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \mu C_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS} \]

\[ R_{SQ} = \left. \frac{V_{DS}}{I_D} \right|_{V_{GS}=V_{DD}} = \frac{1}{\mu C_{OX} \frac{W}{L} (V_{GS} - V_T)} \left|_{V_{GS}=3.5V} \right. \]

\[ = \frac{1}{(E-4)\left(\frac{1}{1}\right)(3.5-1)} = 4K\Omega \]

$C_{GS} = C_{OX}WL = (2.5fFµ^{-2})(1µ^2) = 2.5fF$
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an \textit{p-channel} MOSFET from square-law model

In the 0.5\textmu{}CMOS process if $L=1u$, $W=1u$

\[
(C_{OX}=2.5fF, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0)
\]

Observe $\mu_n \mu_p \approx 3$

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T \  V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \geq V_T \  V_{DS} \geq V_{GS} - V_T
\end{cases}
\]

When SW is on, operation is “deep” triode
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an *p-channel* MOSFET from square-law model
In the 0.5μ CMOS process if $L=1u$, $W=1u$

\[ (C_{OX}=2.5fFμ^{-2}, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0) \]

Observe $\mu_n \mu_p \approx 3$

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left(V_{GS} - V_T\right)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T
\end{cases}
\]

When SW is on, operation is “deep” triode
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an p-channel MOSFET from square-law model in the 0.5u CMOS process if $L=1u$, $W=1u$

\[
(C_{OX}=2.5fF\mu^{-2}, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0)
\]

Observe $\mu_n/\mu_p \approx 3$

\[
I_D = \mu_p C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \cong \mu_p C_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS}
\]

\[
R_{SQ} = \left. \frac{V_{DS}}{I_D} \right|_{V_{GS}=V_{DD}} = \frac{1}{\mu_p C_{OX} \frac{W}{L} (V_{GS} - V_T)} \bigg|_{V_{GS}=3.5V} = \frac{1}{\left(1\over 3\right) (E - 4) \left(\frac{1}{1}\right) (3.5 - 1)} = 12K\Omega
\]

\[
C_{GS} = C_{OX} WL = (2.5fF\mu^{-2})(1\mu^2) = 2.5fF
\]

Observe the resistance of the p-channel device is approximately 3 times larger than that of the n-channel device for same bias and dimensions!
Modeling of the MOSFET

Goal: Obtain a mathematical relationship between the port variables of a device.

\[
\begin{align*}
I_D &= f_1(V_{GS}, V_{DS}, V_{BS}) \\
I_G &= f_2(V_{GS}, V_{DS}, V_{BS}) \\
I_B &= f_3(V_{GS}, V_{DS}, V_{BS})
\end{align*}
\]
Small-Signal Model

Goal with small signal model is to predict performance of circuit or device in the vicinity of an operating point

Operating point is often termed Q-point
Analytical expressions for small signal model will be developed later
Technology Files

• Design Rules

Process Flow (Fabrication Technology)

• Model Parameters
TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process

<table>
<thead>
<tr>
<th>Step</th>
<th>Process Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Clean wafer</td>
</tr>
<tr>
<td>2</td>
<td>GROW THIN OXIDE</td>
</tr>
<tr>
<td>3</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>4</td>
<td>PATTERN n-well</td>
</tr>
<tr>
<td>5</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>6</td>
<td>Deposit and diffus n-type impurities</td>
</tr>
<tr>
<td>7</td>
<td>Strip photoresist</td>
</tr>
<tr>
<td>8</td>
<td>Strip thin oxide</td>
</tr>
<tr>
<td>9</td>
<td>Grow thin oxide</td>
</tr>
<tr>
<td>10</td>
<td>Apply layer of Si$_3$N$_4$</td>
</tr>
<tr>
<td>11</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>12</td>
<td>PATTERN Si$_3$N$_4$ (active area definition)</td>
</tr>
<tr>
<td>13</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>14</td>
<td>Etch Si$_3$N$_4$</td>
</tr>
<tr>
<td>15</td>
<td>Strip photoresist</td>
</tr>
<tr>
<td>A.1</td>
<td>Optional field threshold voltage adjust</td>
</tr>
<tr>
<td>A.2</td>
<td>PATTERN ANTIMOAT IN SUBSTRATE</td>
</tr>
<tr>
<td>A.3</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>A.4</td>
<td>FIELD IMPLANT p-type</td>
</tr>
<tr>
<td>A.5</td>
<td>Strip photoresist</td>
</tr>
<tr>
<td>16</td>
<td>GROW FIELD OXIDE</td>
</tr>
<tr>
<td>17</td>
<td>Strip Si$_3$N$_4$</td>
</tr>
<tr>
<td>18</td>
<td>Strip thin oxide</td>
</tr>
<tr>
<td>19</td>
<td>GROW GATE OXIDE</td>
</tr>
<tr>
<td>20</td>
<td>POLYSILICON DEPOSITION (POLY I)</td>
</tr>
<tr>
<td>21</td>
<td>Apply photoresist</td>
</tr>
<tr>
<td>22</td>
<td>PATTERN POLYSILICON</td>
</tr>
<tr>
<td>23</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>24</td>
<td>ETCH POLYSILICON</td>
</tr>
</tbody>
</table>
25. Strip photoresist
   *Optional steps for double polysilicon process*
   B.1 Strip thin oxide
   B.2 GROW THIN OXIDE
   B.3 POLYSILICON DEPOSITION (POLY II)
   B.4 Apply photoresist
   B.5 PATTERN POLYSILICON (MASK #B1)
   B.6 Develop photoresist
   B.7 ETCH POLYSILICON
   B.8 Strip photoresist
   B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL (MASK #7)
46. Develop photoresist
47. Etch metal
48. Strip photoresist
   Optional steps for double metal process
   C.1 Strip thin oxide
   C.2 DEPOSIT INTERMETAL OXIDE
   C.3 Apply photoresist
   C.4 PATTERN VIAS (MASK #C1)
   C.5 Develop photoresist
   C.6 Etch oxide
   C.7 Strip photoresist
   C.8 APPLY METAL (Metal 2) (MASK #C2)
   C.9 Apply photoresist
   C.10 PATTERN METAL
   C.11 Develop photoresist
   C.12 Etch metal
   C.13 Strip photoresist
49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS (MASK #8)
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST
Bulk CMOS Process Description

- n-well process
- Single Metal Only Depicted
- Double Poly
Components Shown

- n-channel MOSFET
- p-channel MOSFET
- Poly Resistor
- Doubly Poly Capacitor
Consider Basic Components Only

Well Contacts and Guard Rings Will be Discussed Later
Metal details hidden to reduce clutter

n-channel MOSFET

A

A'

B

B'

D

G

S

n-channel MOSFET
| **TABLE 2B.1** |
| Process scenario of major process steps in typical n-well CMOS process<sup>a</sup> |

1. Clean wafer
2. GROW THIN OXIDE
3. Apply photoresist
4. PATTERN n-well
5. Develop photoresist
6. Deposit and diffus n-type impurities
7. Strip photoresist
8. Strip thin oxide
9. Grow thin oxide
10. Apply layer of Si<sub>3</sub>N<sub>4</sub>
11. Apply photoresist
12. PATTERN Si<sub>3</sub>N<sub>4</sub> (active area definition)  \(\text{(MASK \#1)}\)
13. Develop photoresist
14. Etch Si<sub>3</sub>N<sub>4</sub>
15. Strip photoresist
   Optional field threshold voltage adjust
   A.1 Apply photoresist
   A.2 PATTERN ANTIMOAT IN SUBSTRATE  \(\text{(MASK \#A1)}\)
   A.3 Develop photoresist
   A.4 FIELD IMPLANTI p-type)
   A.5 Strip photoresist
16. GROW FIELD OXIDE
17. Strip Si<sub>3</sub>N<sub>4</sub>
18. Strip thin oxide
19. GROW GATE OXIDE
20. POLYSILICON DEPOSITION (POLY I)
21. Apply photoresist
22. PATTERN POLYSILICON  \(\text{(MASK \#3)}\)
23. Develop photoresist
24. ETCH POLYSILICON
N-well Mask
N-well Mask
Detailed Description of First Photolithographic Steps Only

• Top View
• Cross-Section View
N-well Mask

A-A’ Section

n-well

B-B’ Section
### TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process

<table>
<thead>
<tr>
<th>Step</th>
<th>Process Description</th>
<th>Notes</th>
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<tbody>
<tr>
<td>1.</td>
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<td>2.</td>
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<td>(MASK #1)</td>
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<td>Apply photoresist</td>
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<td>4.</td>
<td>PATTERN n-well</td>
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</tr>
<tr>
<td>5.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>6.</td>
<td>Deposit and diffuse n-type impurities</td>
<td></td>
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<tr>
<td>7.</td>
<td>Strip photoresist</td>
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<tr>
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<td>Grow thin oxide</td>
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<tr>
<td>10.</td>
<td>Apply layer of Si$_3$N$_4$</td>
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<td>Apply photoresist</td>
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<td>PATTERN Si$_3$N$_4$ (active area definition)</td>
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<td>14.</td>
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<td>15.</td>
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  *Optional field threshold voltage adjust*

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<th>Sub-step</th>
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<tr>
<td>A.1</td>
<td>Apply photoresist</td>
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<td>PATTERN ANTIMOAT IN SUBSTRATE</td>
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<tr>
<td>A.3</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>A.4</td>
<td>FIELD IMPLANT p-type</td>
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<td>A.5</td>
<td>Strip photoresist</td>
</tr>
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<td>16.</td>
<td>GROW FIELD OXIDE</td>
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Active Mask
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<td>Clean wafer</td>
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<td>3.</td>
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<td>PATTERN n-well</td>
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<tr>
<td>10.</td>
<td>Apply layer of Si₃N₄</td>
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<td>Optional field threshold voltage adjust</td>
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<tr>
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<td>A.2 PATTERN ANTIMOAT IN SUBSTRATE</td>
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<tr>
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<td>A.3 Develop photoresist</td>
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</tr>
<tr>
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<td>A.4 FIELD IMPLANT p-type</td>
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<td></td>
<td>A.5 Strip photoresist</td>
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<td>24.</td>
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</table>
Poly1 Mask
Poly plays a key role in all four types of devices!
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<td>Etch Si$_3$N$_4$</td>
</tr>
<tr>
<td>15</td>
<td>Strip photoresist</td>
</tr>
</tbody>
</table>

*Optional field threshold voltage adjust*

| A.1 | Apply photoresist |
| A.2 | PATTERN ANTIMOX IN SUBSTRATE | *(MASK #A1)* |
| A.3 | Develop photoresist |
| A.4 | FIELD IMPLANT p-type |
| A.5 | Strip photoresist |

| 16   | GROW FIELD OXIDE |
| 17   | Strip Si$_3$N$_4$ |
| 18   | Strip thin oxide |
| 19   | GROW GATE OXIDE |
| 20   | POLYSILICON DEPOSITION (POLY I) |
| 21   | Apply photoresist |
| 22   | PATTERN POLYSILICON | *(MASK #3)* |
| 23   | Develop photoresist |
| 24   | ETCH POLYSILICON |
25. Strip photoresist

*Optional steps for double polysilicon process*
B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

(MASK #B1)

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P⁺ GUARD RINGS (p-well ohmic contacts)  (MASK #4)
28. Develop photoresist
29. p⁺ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N⁺ GUARD RINGS (top ohmic contact to substrate)  (MASK #5)
33. Develop photoresist
34. n⁺ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS  (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
Poly 2 Mask

A

B

A'

B'
<table>
<thead>
<tr>
<th>Step</th>
<th>Process Step</th>
<th>Notes</th>
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<td>(MASK #1)</td>
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<td>Deposit and diffuse n-type impurities</td>
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<tr>
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<td>13.</td>
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<tr>
<td>14.</td>
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<td><strong>Optional field threshold voltage adjust</strong></td>
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<tr>
<td>A.1</td>
<td>Apply photoresist</td>
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<tr>
<td>A.2</td>
<td>PATTERN ANTIMOAT IN SUBSTRATE</td>
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<td>A.3</td>
<td>Develop photoresist</td>
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<tr>
<td>A.4</td>
<td>FIELD IMPLANT p-type</td>
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<td>Strip Si$_3$N$_4$</td>
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<td>19.</td>
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<td>20.</td>
<td>POLYSILICON DEPOSITION (POLY I)</td>
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<td>21.</td>
<td>Apply photoresist</td>
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<td>22.</td>
<td>PATTERN POLYSILICON</td>
<td>(MASK #3)</td>
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<td>Develop photoresist</td>
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</tr>
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<td>ETCH POLYSILICON</td>
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</table>
25. Strip photoresist

*Optional steps for double polysilicon process*

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON (MASK #B1)
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

![Red circles highlighting steps 27, 29, and 32.]

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
P-Select
P-Select Mask – p-diffusion

Note the gate is self aligned!!
P-Select Mask – n-diffusion

A-A’ Section

n-diffusion

B-B’ Section
<table>
<thead>
<tr>
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<th>Process Description</th>
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<tbody>
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<td>Optional field threshold voltage adjust</td>
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<tr>
<td></td>
<td>A.1 Apply photoresist</td>
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<tr>
<td></td>
<td>A.2 PATTERN ANTIMOAT IN SUBSTRATE</td>
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<td>A.3 Develop photoresist</td>
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<td>A.4 FIELD IMPLANT p-type</td>
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</table>
25. Strip photoresist
   *Optional steps for double polysilicon process*
   B.1 Strip thin oxide
   B.2 GROW THIN OXIDE
   B.3 POLYSILICON DEPOSITION (POLY II)
   B.4 Apply photoresist
   B.5 PATTERN POLYSILICON (MASK #B1)
   B.6 Develop photoresist
   B.7 ETCH POLYSILICON
   B.8 Strip photoresist
   B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND
    P+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND
    N+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL (MASK #7)
46. Develop photoresist
47. Etch metal
48. Strip photoresist
   Optional steps for double metal process
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   C.2 DEPOSIT INTERMETAL OXIDE
   C.3 Apply photoresist
   C.4 PATTERN VIAS (MASK #C1)
   C.5 Develop photoresist
   C.6 Etch oxide
   C.7 Strip photoresist
   C.8 APPLY METAL (Metal 2) (MASK #C2)
   C.9 Apply photoresist
   C.10 PATTERN METAL
   C.11 Develop photoresist
   C.12 Etch metal
   C.13 Strip photoresist
49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS (MASK #8)
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST
TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process

1. Clean wafer
2. GROW THIN OXIDE
3. Apply photoresist
4. PATTERN n-well (MASK #1)
5. Develop photoresist
6. Deposit and diffus n-type impurities
7. Strip photoresist
8. Strip thin oxide
9. Grow thin oxide
10. Apply layer of Si₃N₄
11. Apply photoresist
12. PATTERN Si₃N₄ (active area definition) (MASK #2)
13. Develop photoresist
14. Etch Si₃N₄
15. Strip photoresist
   Optional field threshold voltage adjust
   A.1 Apply photoresist
   A.2 PATTERN ANTIMOAT IN SUBSTRATE (MASK #A1)
   A.3 Develop photoresist
   A.4 FIELD IMPLANT p-type
   A.5 Strip photoresist
16. GROW FIELD OXIDE
17. Strip Si₃N₄
18. Strip thin oxide
19. GROW GATE OXIDE
20. POLYSILICON DEPOSITION (POLY I)
21. Apply photoresist
22. PATTERN POLYSILICON (MASK #3)
23. Develop photoresist
24. ETCH POLYSILICON
25. Strip photoresist
   \textit{Optional steps for double polysilicon process}
   B.1 Strip thin oxide
   B.2 GROW THIN OXIDE
   B.3 POLYSILICON DEPOSITION (POLY II)
   B.4 Apply photoresist
   B.5 PATTERN POLYSILICON \hfill (MASK \#B1)
   B.6 Develop photoresist
   B.7 ETCH POLYSILICON
   B.8 Strip photoresist
   B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND \hfill (MASK \#4)
    P\textsuperscript{+} GUARD RINGS (p-well ohmic contacts)
28. Develop photoresist
29. p\textsuperscript{+} IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND \hfill (MASK \#5)
    N\textsuperscript{+} GUARD RINGS (top ohmic contact to substrate)
33. Develop photoresist
34. n\textsuperscript{+} IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS \hfill (MASK \#6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL
46. Develop photoresist
47. Etch metal
48. Strip photoresist
   Optional steps for double metal process
   C.1 Strip thin oxide
   C.2 DEPOSIT INTERMETAL OXIDE
   C.3 Apply photoresist
   C.4 PATTERN VIAS
   C.5 Develop photoresist
   C.6 Etch oxide
   C.7 Strip photoresist
   C.8 APPLY METAL (Metal 2)
   C.9 Apply photoresist
   C.10 PATTERN METAL
   C.11 Develop photoresist
   C.12 Etch metal
   C.13 Strip photoresist
49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST
Metal 1 Mask
Capacitor

Resistor

P-channel MOSFET

n-channel MOSFET
End of Lecture 16