Devices in Semiconductor Processes

- MOSFETs

Bulk CMOS Process Flow
Graphical Representation of MOS Model

Review from Last Lecture

\[
I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \text{ and } V_{DS} < 2V_T - V_{GS} \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T \right) V_{DS} & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T 
\end{cases}
\]

\[I_G = I_B = 0\]
PMOS and NMOS Models

- Functional form identical, sign changes and parameter values different
- Will give details about p-channel model later
Model Extensions

Review from Last Lecture

\[ I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 \cdot (1 + \lambda V_{DS}) & V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T 
\end{cases} \]

Note: This introduces small discontinuity (not shown) in model at SAT/Triode transition
Most analog circuits operate in the saturation region
(basic VVR operates in triode and is an exception)

Most digital circuits operate in triode and cutoff regions and switch
between these two with Boolean inputs
Model Extension (short devices)

As the channel length becomes very short, velocity saturation will occur in the channel and this will occur with electric fields around 2V/u. So, if a gate length is around 1u, then voltages up to 2V can be applied without velocity saturation. But, if gate length decreases and voltages are kept high, velocity saturation will occur.

\[
I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{ox} \frac{W}{2L} (V_{GS} - V_T)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T \\
\theta_2 \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T \right)^{\alpha} V_{DS} & V_{GS} \geq V_T \\
\theta_2 \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T \right)^{\alpha} & V_{GS} \geq V_T, V_{DS} \geq \theta_1 (V_{GS} - V_T)^{\alpha} 
\end{cases}
\]

\(\alpha\) is the velocity saturation index, \(2 \geq \alpha \geq 1\)
Model Extension (BSIM model)

```
.MODEL CMOSN NMOS (LEVEL = 49)
+VERSION = 3.1
+TNOM = 27
+TOX = 1.42E-8
+XJ = 1.5E-7
+NCH = 1.7E17
+VTH0 = 0.629035
+K1 = 0.8976376
+K2 = -0.09255
+K3 = 24.0984767
+W0 = 1.041146E-8
+NLX = 1E-9
+DVT1W = 0
+DVT2W = 0
+DVT0 = 2.7123969
+DVT1 = 0.4232931
+UA = 3.091785E-13
+UB = 1.702517E-18
+UC = 1.22401E-11
+VSAT = 1.715884E5
+AO = 0.6580918
+AGS = 0.130484
+B0 = 2.446405E-6
+B1 = 5E-6
+KETA = -3.043349E-3
+A1 = 8.18159E-7
+A2 = 0.3363058
+RDSW = 1.367055E3
+PRWG = 0.0328586
+PRWB = 0.0104806
+W = 1
+WINT = 2.443677E-7
+LINT = 6.999776E-8
+XL = 1E-7
+XW = 0
+DWG = -1.256454E-8
+DWB = 3.676235E-8
+VOFF = -1.493503E-4
+NFACOR = 1.0354201
+CIT = 0
+CDSC = 2.4E-4
+CDSCD = 0
+CDSCB = 0
+ETA0 = 2.342963E-3
+ETAB = -1.5324E-4
+DSUB = 0.0764123
+PCLM = 2.5941582
+PDIBLC1 = 0.8187825
+PDIBLC2 = 2.366707E-3
+PDIBLCB = -0.0431505
+PSCBE1 = 6.611774E8
+PSCBE2 = 3.238266E-4
+DROUT = 0.9919348
+PVTAG = 0
+PRT = 0
+UTE = -1.5
+XTAG = -0.11
+K1L = 0
+KT2 = 0.022
+UA1 = 4.31E-9
+UB1 = -7.61E-18
+UC1 = -5.6E-11
+WL = 0
+WLN = 0
+WWL = 0
+WW = 0
+WLN = 0
+LW = 0
+LLN = 1
+LWN = 1
+LWL = 0
+CAPMOD = 2
+XPART = 0.5
+CGDO = 2.32E-10
+CGSO = 2.32E-10
+CGBO = 1E-9
+PJ = 4.282017E-4
+PB = 0.9317787
+PBSW = 0.8
+PBSWG = 0.8
+CF = 0
+PVTH0 = 0.0520855
+PRDSW = 112.8875816
+PK2 = -0.0289036
+WKETA = -0.0237483
+LKETA = 1.728324E-3
)```

Review from Last Lecture
Review from Last Lecture

Model Errors with Different W/L Values

Binning models can improve model accuracy
BSIM Binning Model
- Bin on device sizes
- multiple BSIM models!

With 32 bins, this model has 3040 model parameters!
Model Changes with Process Variations

(n-ch characteristics shown)

Corner models can improve model accuracy
BSIM Corner Models with Binning
- Often 4 corners in addition to nominal TT, FF, FS, SF, and SS
- bin on device sizes

With 32 size bins and 4 corners, this model has 15,200 model parameters!
How many models of the MOSFET do we have?

Switch-level model (2)

Square-law model

Square-law model (with $\lambda$ and bulk additions)

$\alpha$-law model (with $\lambda$ and bulk additions)

BSIM model

BSIM model (with binning extensions)

BSIM model (with binning extensions and process corners)
The Modeling Challenge

Difficult to obtain analytical functions that accurately fit actual devices over bias, size, and process variations
Model Status

- Simple dc Model
  - Square-Law Model
  - Square-Law Model (with extensions for λ, γ effects)
  - Short-Channel α-law Model

- Better Analytical dc Model
  - BSIM Model

- Sophisticated Model for Computer Simulations
  - Switch-Level Models
    - Ideal switches
    - $R_{SW}$ and $C_{GS}$

- Small Signal
  - Frequency Dependent Small Signal

- Simpler dc Model
In the next few slides, the models we have developed will be listed and reviewed:

- Square-law Model
- Switch-level Models
- Extended Square-law model
- Short-channel model
- BSIM Model
- BSIM Binning Model
- Corner Models
Square-Law Model

Model Parameters : \{\mu, C_{\text{OX}}, V_{T0}\}

Design Parameters : \{W,L\}  but only one degree of freedom W/L

\[ I_D = \begin{cases} 
0 & V_{GS} \leq V_T \\
\frac{\mu C_{\text{OX}}}{L} W \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\frac{\mu C_{\text{OX}}}{2L} \left( V_{GS} - V_T \right)^2 & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases} \]
Switch-Level Models

Switch-level model including gate capacitance and drain resistance

Switch closed for $V_{GS} = \text{“1”}$

$C_{GS}$ and $R_{SW}$ dependent upon device sizes and process

For minimum-sized devices in a 0.5u process

$C_{GS} \approx 1.5\text{fF} \quad R_{SW} \approx \begin{cases} 2\text{K}\Omega & \text{n-channel} \\ 6\text{K}\Omega & \text{p-channel} \end{cases}$

Considerable emphasis will be placed upon device sizing to manage $C_{GS}$ and $R_{SW}$

Model Parameters: $\{C_{GS}, R_{SW}\}$
Extended Square-Law Model

\[ I_G = 0 \]
\[ I_B = 0 \]

\[ I_d = \begin{cases} 
0 & V_{GS} \leq V_T \\
\mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T, V_{DS} < V_{GS} - V_T \\
\mu C_{OX} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 \cdot (1 + \lambda V_{DS}) & V_{GS} \geq V_T, V_{DS} \geq V_{GS} - V_T 
\end{cases} \]

\[ V_T = V_{T0} + \gamma \left( \sqrt{\phi} - V_{BS} - \sqrt{\phi} \right) \]

Model Parameters : \( \{ \mu, C_{OX}, V_{T0}, \phi, \gamma, \lambda \} \)

Design Parameters : \( \{ W, L \} \) but only one degree of freedom \( W/L \)
Short-Channel Model

\[ I_D = \begin{cases} 
0 & \text{if} \quad V_{GS} \leq V_T \\
\frac{\theta_2}{\theta_1} \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^{\alpha} V_{DS} & \text{if} \quad V_{GS} \geq V_T, \quad V_{DS} < \theta_1 (V_{GS} - V_T)^{\alpha} \\
\theta_2 \mu C_{ox} \frac{W}{L} (V_{GS} - V_T)^{\alpha} & \text{if} \quad V_{GS} \geq V_T, \quad V_{DS} \geq \theta_1 (V_{GS} - V_T)^{\alpha}
\end{cases} \]

\( \alpha \) is the velocity saturation index, \( 2 \geq \alpha \geq 1 \)

Channel length modulation (\( \lambda \)) and bulk effects can be added to the velocity Saturation as well.
BSIM model

Note this model has 95 model parameters!
BSIM Binning Model

- Bin on device sizes
- multiple BSIM models!

With 32 bins, this model has 3040 model parameters!
BSIM Corner Models

- Often 4 corners in addition to nominal: TT, FF, FS, SF, and SS
- five different BSIM models!

```
.MODEL CMOSN NMOS 
+VERSION = 3.1
+XJ = 1.5E-7
+K1 = 0.8976376
+K3B = -8.2369696
+DVTOW = 0
+DVT0 = 2.7123969
+U0 = 451.2322004
+UC = 1.22401E-11
+AGS = 0.130484
+KETA = -3.043349E-3
+RDSW = 1.367055E3
+WR = 1
+XL = 1E-7
+DWB = 3.676235E-8
+CIT = 0
+CDSCB = 0
+DSUB = 0.0764123
+PDBLC2 = 2.366707E-3
+PSCEB1 = 6.611774E8
+DRITA = 0.0 1
+PRT = 0
+K1L = 0
+UBL = -7.61E-18
+WLN = 0
+WWN = 1
+LNL = 1
+LWL = 0
+CGDO = 2.32E-10
+RJ = 4.282017E-4
+CJSW = 3.034055E-10
+CF = 0
+PK2 = -0.0289036
+KMIN = -0.09255
W0 = 1.041146E-8
DVT1W = 0
DVT1 = 0.4232931
UA = 3.091785E-13
VSAT = 1.715884E5
B0 = 2.446405E-6
A1 = 8.18159E-7
PRWG = 0.0328586
WINT = 2.443677E-7
XW = 0
VOFF = -1.493503E-4
CDSC = 2.4E-4
ETA0 = 2.342963E-3
PCLM = 2.5941582
PDIBLCB = -0.0431505
PSCEB2 = 3.238266E-4
NORMIN = 1
UTE = -1.5
KT2 = 0.022
UC1 = -5.6E-11
WLN = 1
WWL = 0
LW = 0
CAPMOD = 2
CGSO = 2.32E-10
PB = 0.9317787
PSW = 0.8
PB3 = 0
PKTHO = -0.0237483
TP = 0.9317787
MK = 0.4495867
M3 = 0.173852
M3J = 0.173852
M3JS = 112.887516
PKTH = 0.9317787
LKB = 1.728324E-3

LEVEL = 49
TOX = 1.42E-8
VTH0 = 0.629035
K3 = 24.0984767
NLX = 1E-9
DVT2W = 0
DVT2 = -0.1403765
UB = 1.702517E-18
A0 = 0.6580918
B1 = 5E-6
A2 = 0.3363058
PRWB = 0.0104806
LINT = 6.999776E-8
DWG = -1.256454E-8
NFACTOR = 1.0354201
CDSCD = 0
ETA = -1.5324E-4
PDIBLC1 = 0.8187825
DROUT = 0.9919348
PVAG = 0

TT: typical-typical
FF: fast n, fast p
FS: fast n, slow p
SF: slow n, fast p
SS: slow n, slow p

With 4 corners and 30 bins, this model has 15,200 model parameters!
Hierarchical Model Comparisons

- **Switch-Level Models**
  - Number of Model Parameters: 0 to 2

- **Square-Law Models**
  - Number of Model Parameters: 3 to 6

- **BSIM Models**
  - Number of Model Parameters: Approx 100

- **BSIM Binning Models**
  - Number of Model Parameters: Approx 3000 (for 30 bins)

Accuracy
Complexity

Analytical
Numerical (for simulation only)
Corner Models

Number of model parameters now approximately 15,000

Applicable at any level in model hierarchy (same model, different parameters)

Often 4 corners (FF, FS, SF, SS) used but sometimes many more

Designers must provide enough robustness so good yield at all corners
n-channel .... p-channel modeling

Positive $V_{DS}$ and $V_{GS}$ cause a positive $I_D$

$$I_D = \begin{cases} 0 & \text{for } V_{GS} \leq V_{Tn} \\ \mu_n C_{OX} \frac{W}{L} (V_{GS} - V_{Tn} - \frac{V_{DS}}{2}) V_{DS} & \text{for } V_{GS} \geq V_{Tn} \text{ and } V_{DS} < V_{GS} - V_{Tn} \\ \mu_n C_{OX} \frac{W}{2L} (V_{GS} - V_{Tn})^2 & \text{for } V_{GS} \geq V_{Tn} \text{ and } V_{DS} \geq V_{GS} - V_{Tn} \end{cases}$$

$V_{GS4} > V_{GS3} > V_{GS2} > V_{GS1} > 0$

(for enhancement devices)

$n$-channel MOSFET

- Gate
- Source
- Drain
- Bulk
n-channel .... p-channel modeling

Functional form of models are the same, just sign differences and some parameter differences (usually mobility is the most important)
n-channel …. p-channel modeling

- Gate
- Drain
- Source
- Bulk

p-channel MOSFET

\[ I_D = \begin{cases} \ 0 & \text{if } V_{GS} \geq V_{Tp} \\ \ -\mu_p C_{OX} \frac{W}{L} \left( V_{GS} - V_{Ts} - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} \leq V_{Ts} \text{ and } V_{DS} > V_{GS} - V_{Tp} \\ \ -\mu_p C_{OX} \frac{W}{2L} \left( V_{GS} - V_{Ts} \right)^2 & \text{if } V_{GS} \leq V_{Ts} \text{ and } V_{DS} \leq V_{GS} - V_{Tp} \end{cases} \]

- \( I_G = I_B = 0 \)

- Actually should use \( C_{OXp} \) and \( C_{OXn} \) but they are usually almost identical in most processes
- \( \mu_n \approx 3\mu_p \)
- May choose to model \(-I_D\) which will be non-negative
n-channel .... p-channel modeling

Gate Drain Source Bulk
p-channel MOSFET

(for enhancement devices)

\[ V_{GS4} < V_{GS3} < V_{GS2} < V_{GS1} < 0 \]

\[ I_D = \begin{cases} 
0 & \text{if } V_{GS} \geq V_{TP} \\
-\mu_p C_{ox} \frac{W}{L} \left( V_{GS} - V_{TP} - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} \leq V_{TP} \text{ and } V_{DS} > V_{GS} - V_{TP} \\
-\mu_p C_{ox} \frac{W}{2L} \left( V_{GS} - V_{TP} \right)^2 & \text{if } V_{GS} \leq V_{TP} \text{ and } V_{DS} \leq V_{GS} - V_{TP} 
\end{cases} \]

\[ I_G = I_B = 0 \]

Alternate equivalent representation

\[ I_D = \begin{cases} 
0 & \text{if } |V_{GS}| \leq |V_{TP}| \\
\mu_p C_{ox} \frac{W}{L} \left( V_{GS} - V_{TP} - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } |V_{GS}| \geq |V_{TP}| \text{ and } |V_{DS}| < |V_{GS} - V_{TP}| \\
\mu_p C_{ox} \frac{W}{2L} \left( V_{GS} - V_{TP} \right)^2 & \text{if } |V_{GS}| \geq |V_{TP}| \text{ and } |V_{DS}| \geq |V_{GS} - V_{TP}| 
\end{cases} \]

\[ I_G = I_B = 0 \]

These look like those for the n-channel device but with ||
n-channel .... p-channel modeling

Models essentially the same with different signs and model parameters

\[
I_D = \begin{cases} 
0 & \text{if } V_{gs} \leq V_n \\
\mu_n C_{ox} \frac{W}{L} \left( V_{gs} - V_n - \frac{V_d}{2} \right) V_{ds} & \text{if } V_{gs} \geq V_n, \ V_{gs} < V_{gs} - V_n \\
\mu_n C_{ox} \frac{W}{2L} \left( V_{gs} - V_n \right)^2 & \text{if } V_{gs} \geq V_n, \ V_{gs} \geq V_{gs} - V_n \\
\end{cases}
\]

\[
I_D = \begin{cases} 
0 & \text{if } V_{gs} \geq V_t \ \\
-\mu_p C_{ox} \frac{W}{L} \left( V_{gs} - V_t - \frac{V_d}{2} \right) V_{ds} & \text{if } V_{gs} \leq V_t, \ V_{gs} > V_{gs} - V_t \\
-\mu_p C_{ox} \frac{W}{2L} \left( V_{gs} - V_t \right)^2 & \text{if } V_{gs} \leq V_t, \ V_{gs} \leq V_{gs} - V_t \\
\end{cases}
\]
Determine $R_{SW}$ and $C_{GS}$ for an n-channel MOSFET from square-law model in the 0.5u ON CMOS process if $L=1u, W=1u$

(Assume $\mu C_{OX}=100\mu AV^{-2}, C_{OX}=2.5f Fu^{-2}, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0$)

\[
I_D = \begin{cases} 
0 & \text{if } V_{GS} \leq V_T \\
\mu C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} < V_{GS} - V_T \\
\mu C_{OX} \frac{W}{2L} (V_{GS} - V_T)^2 & \text{if } V_{GS} \geq V_T \text{ and } V_{DS} \geq V_{GS} - V_T 
\end{cases}
\]

when SW is on, operation is “deep” triode
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an n-channel MOSFET from square-law model in the 0.5μ ON CMOS process if $L=1μ$, $W=1μ$

(Assume $μC_{OX}=100μAV^2$, $C_{OX}=2.5fFμ^{-2}$, $V_{T0}=1V$, $V_{DD}=3.5V$, $V_{SS}=0$)

When on operating in deep triode

$$I_D = μC_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx μC_{OX} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

$$R_{SQ} = \left. \frac{V_{DS}}{I_D} \right|_{V_{GS}=V_{DD}} = \left. \frac{1}{μC_{OX} \frac{W}{L} (V_{GS} - V_T)} \right|_{V_{GS}=3.5V} = \frac{1}{(E - 4) \left( \frac{1}{1} \right) (3.5 - 1)} = 4KΩ$$

$$C_{GS} = C_{OX}WL = (2.5fFμ^{-2})(1μ^2) = 2.5fF$$
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an p-channel MOSFET from square-law model in the 0.5μ ON CMOS process if $L=1μ$, $W=1μ$

$\left( C_{OX}=2.5fFμ^{-2}, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0 \right)$

Observe $\mu_n/\mu_p \approx 3$

$$-I_D = \begin{cases} 0 & V_{GS} \leq V_T \\ \mu C_{ox} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} & V_{GS} \geq V_T \quad V_{DS} < V_{GS} - V_T \\ \mu C_{ox} \frac{W}{2L} \left( V_{GS} - V_T \right)^2 & V_{GS} \geq V_T \quad V_{DS} \geq V_{GS} - V_T \end{cases}$$

When SW is on, operation is “deep” triode
Model Relationships

Determine $R_{SW}$ and $C_{GS}$ for an p-channel MOSFET from square-law model in the 0.5u ON CMOS process if $L=1u$, $W=1u$

$$ ( C_{OX}=2.5fF u^{-2}, V_{T0}=1V, V_{DD}=3.5V, V_{SS}=0) $$

Observe $\mu_n/\mu_p \approx 3$

$$ -I_D = \mu_p C_{OX} \frac{W}{L} \left( V_{GS} - V_T - \frac{V_{DS}}{2} \right) V_{DS} \approx \mu_p C_{OX} \frac{W}{L} \left( V_{GS} - V_T \right) V_{DS} $$

$$ R_{SO} = \frac{-V_{DS}}{-I_D} \bigg|_{V_{GS}=V_{DD}} = \frac{1}{\mu_p C_{OX} \frac{W}{L} \left( V_{GS} - V_T \right)} \bigg|_{V_{GS}=3.5V} = 12K\Omega $$

$$ C_{GS} = C_{OX} WL = (2.5fF u^{-2})(1u^2) = 2.5fF $$

Observe the resistance of the p-channel device is approximately 3 times larger than that of the n-channel device for same bias and dimensions!
Modeling of the MOSFET

Goal: Obtain a mathematical relationship between the port variables of a device.

\[
\begin{align*}
I_D &= f_1(V_{GS}, V_{DS}, V_{BS}) \\
I_G &= f_2(V_{GS}, V_{DS}, V_{BS}) \\
I_B &= f_3(V_{GS}, V_{DS}, V_{BS})
\end{align*}
\]
Small-Signal Model

Goal with small signal model is to predict performance of circuit or device in the vicinity of an operating point.

Operating point is often termed Q-point.
Small-Signal Model

Analytical expressions for small signal model will be developed later
Technology Files

- Design Rules

→ Process Flow (Fabrication Technology)

- Model Parameters
TABLE 2B.1  
Process scenario of major process steps in typical n-well CMOS process$^a$

<table>
<thead>
<tr>
<th>Step</th>
<th>Process Description</th>
<th>Mask Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>Clean wafer</td>
<td></td>
</tr>
<tr>
<td>2.</td>
<td>GROW THIN OXIDE</td>
<td></td>
</tr>
<tr>
<td>3.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>4.</td>
<td>PATTERN n-well</td>
<td>(MASK #1)</td>
</tr>
<tr>
<td>5.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>6.</td>
<td>Deposit and diffus n-type impurities</td>
<td></td>
</tr>
<tr>
<td>7.</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td>8.</td>
<td>Strip thin oxide</td>
<td></td>
</tr>
<tr>
<td>9.</td>
<td>Grow thin oxide</td>
<td></td>
</tr>
<tr>
<td>10.</td>
<td>Apply layer of Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>11.</td>
<td>Apply photoresist</td>
<td></td>
</tr>
<tr>
<td>12.</td>
<td>PATTERN Si$_3$N$_4$ (active area definition)</td>
<td>(MASK #2)</td>
</tr>
<tr>
<td>13.</td>
<td>Develop photoresist</td>
<td></td>
</tr>
<tr>
<td>14.</td>
<td>Etch Si$_3$N$_4$</td>
<td></td>
</tr>
<tr>
<td>15.</td>
<td>Strip photoresist</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Optional field threshold voltage adjust</td>
<td></td>
</tr>
<tr>
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<td>PATTERN ANTIMOSAT IN SUBSTRATE</td>
<td>(MASK #A1)</td>
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<td>Develop photoresist</td>
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<td>A.4</td>
<td>FIELD IMPLANT p-type)</td>
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<td>(MASK #3)</td>
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<td>21.</td>
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<td>24.</td>
<td>ETCH POLYSILICON</td>
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</table>
25. Strip photoresist

*Optional steps for double polysilicon process*

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON  (MASK #B1)
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND  (MASK #4)
P⁺ GUARD RINGS (p-well ohmic contacts)
28. Develop photoresist
29. p⁺ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND  (MASK #5)
N⁺ GUARD RINGS (top ohmic contact to substrate)
33. Develop photoresist
34. n⁺ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS  (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL
46. Develop photoresist
47. Etch metal
48. Strip photoresist
   Optional steps for double metal process
   C.1 Strip thin oxide
   C.2 DEPOSIT INTERMETAL OXIDE
   C.3 Apply photoresist
   C.4 PATTERN VIAS
   C.5 Develop photoresist
   C.6 Etch oxide
   C.7 Strip photoresist
   C.8 APPLY METAL (Metal 2)
   C.9 Apply photoresist
   C.10 PATTERN METAL
   C.11 Develop photoresist
   C.12 Etch metal
   C.13 Strip photoresist
49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST

(MASK #7)

(MASK #C1)

(MASK #C2)

(MASK #8)
Bulk CMOS Process Description

• n-well process
• Single Metal Only Depicted
• Double Poly

- This type of process dominates what is used for high-volume “low-cost” processing of integrated circuits today

- Many process variants and specialized processes are used for lower-volume or niche applications

- Emphasis in this course will be on the electronics associated with the design of integrated electronic circuits in processes targeting high-volume low-cost products where competition based upon price differentiation may be acute

- Basic electronics concepts, however, are applicable for lower-volume or niche applications
Components Shown

• n-channel MOSFET
• p-channel MOSFET
• Poly Resistor
• Doubly Poly Capacitor
Consider Basic Components Only

Well Contacts and Guard Rings Will be Discussed Later
Metal details hidden to reduce clutter

n-channel MOSFET
Capacitor

Resistor

p-channel MOSFET

n-channel MOSFET
TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process

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</table>

(MASK #1)
(MASK #2)
(MASK #A1)
(MASK #3)
N-well Mask
Detailed Description of First Photolithographic Steps Only

• Top View
• Cross-Section View
Blank Wafer

- p-doped Substrate

Expose

Develop

Photoresist

n-well Mask

Implant

Will use positive photoresist (exposed region soluble in developer)
Develop

A-A' Section

B-B' Section

Photoresist

N-well Mask

Exposure

Develop
N-well Mask

A-A’ Section

B-B’ Section

n-well
<table>
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Active Mask
Active Mask
TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process

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Poly1 Mask
Poly plays a key role in all four types of devices!
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</table>
25. Strip photoresist

Optional steps for double polysilicon process

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

(MASK #B1)

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND
   P⁺ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p⁺ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND
   N⁺ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n⁺ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
Poly 2 Mask
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25. Strip photoresist

*Optional steps for double polysilicon process*

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON (MASK #B1)
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
P-Select
P-Select Mask – p-diffusion

Note the gate is self aligned!!
n-Select Mask – n-diffusion

A-A’ Section

B-B’ Section

n-diffusion
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</tr>
<tr>
<td></td>
<td>A.4 FIELD IMPLANT p-type)</td>
</tr>
<tr>
<td></td>
<td>A.5 Strip photoresist</td>
</tr>
<tr>
<td>17.</td>
<td>GROW FIELD OXIDE</td>
</tr>
<tr>
<td>18.</td>
<td>Strip Si$_3$N$_4$</td>
</tr>
<tr>
<td>19.</td>
<td>Strip thin oxide</td>
</tr>
<tr>
<td>20.</td>
<td>GROW GATE OXIDE</td>
</tr>
<tr>
<td>21.</td>
<td>POLYSILICON DEPOSITION (POLY I)</td>
</tr>
<tr>
<td>22.</td>
<td>Apply photoresist (MASK #3)</td>
</tr>
<tr>
<td>23.</td>
<td>PATTERN POLYSILICON</td>
</tr>
<tr>
<td>24.</td>
<td>Develop photoresist</td>
</tr>
<tr>
<td>25.</td>
<td>ETCH POLYSILICON</td>
</tr>
</tbody>
</table>
25. Strip photoresist
   *Optional steps for double polysilicon process*
   B.1 Strip thin oxide
   B.2 GROW THIN OXIDE
   B.3 POLYSILICON DEPOSITION (POLY II)
   B.4 Apply photoresist
   B.5 PATTERN POLYSILICON (MASK #B1)
   B.6 Develop photoresist
   B.7 ETCH POLYSILICON
   B.8 Strip photoresist
   B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P+ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p+ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N+ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n+ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL
46. Develop photoresist
47. Etch metal
48. Strip photoresist

*Optional steps for double metal process*
C.1 Strip thin oxide
C.2 DEPOSIT INTERMETAL OXIDE
C.3 Apply photoresist
C.4 PATTERN VIAS
C.5 Develop photoresist
C.6 Etch oxide
C.7 Strip photoresist
C.8 APPLY METAL (Metal 2)
C.9 Apply photoresist
C.10 PATTERN METAL
C.11 Develop photoresist
C.12 Etch metal
C.13 Strip photoresist

49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST
Contact Mask
TABLE 2B.1
Process scenario of major process steps in typical n-well CMOS process

1. Clean wafer
2. GROW THIN OXIDE
3. Apply photoresist
4. PATTERN n-well                  (MASK #1)
5. Develop photoresist
6. Deposit and diffus n-type impurities
7. Strip photoresist
8. Strip thin oxide
9. Grow thin oxide
10. Apply layer of Si$_3$N$_4$
11. Apply photoresist
12. PATTERN Si$_3$N$_4$ (active area definition)    (MASK #2)
13. Develop photoresist
14. Etch Si$_3$N$_4$
15. Strip photoresist
   *Optional field threshold voltage adjust*
   A.1 Apply photoresist
   A.2 PATTERN ANTIMOAT IN SUBSTRATE          (MASK #A1)
   A.3 Develop photoresist
   A.4 FIELD IMPLANT p-type
   A.5 Strip photoresist
16. GROW FIELD OXIDE
17. Strip Si$_3$N$_4$
18. Strip thin oxide
19. GROW GATE OXIDE
20. POLYSILICON DEPOSITION (POLY I)
21. Apply photoresist
22. PATTERN POLYSILICON                  (MASK #3)
23. Develop photoresist
24. ETCH POLYSILICON
25. Strip photoresist

*Optional steps for double polysilicon process*

B.1 Strip thin oxide
B.2 GROW THIN OXIDE
B.3 POLYSILICON DEPOSITION (POLY II)
B.4 Apply photoresist
B.5 PATTERN POLYSILICON (MASK #B1)
B.6 Develop photoresist
B.7 ETCH POLYSILICON
B.8 Strip photoresist
B.9 Strip thin oxide

26. Apply photoresist
27. PATTERN P-CHANNEL DRAINS AND SOURCES AND P⁺ GUARD RINGS (p-well ohmic contacts) (MASK #4)
28. Develop photoresist
29. p⁺ IMPLANT
30. Strip photoresist
31. Apply photoresist
32. PATTERN N-CHANNEL DRAINS AND SOURCES AND N⁺ GUARD RINGS (top ohmic contact to substrate) (MASK #5)
33. Develop photoresist
34. n⁺ IMPLANT
35. Strip photoresist
36. Strip thin oxide
37. Grow oxide
38. Apply photoresist
39. PATTERN CONTACT OPENINGS (MASK #6)
40. Develop photoresist
41. Etch oxide
42. Strip photoresist
43. APPLY METAL
44. Apply photoresist
45. PATTERN METAL
46. Develop photoresist
47. Etch metal
48. Strip photoresist

Optional steps for double metal process
C.1 Strip thin oxide
C.2 DEPOSIT INTERMETAL OXIDE
C.3 Apply photoresist
C.4 PATTERN VIAS
C.5 Develop photoresist
C.6 Etch oxide
C.7 Strip photoresist
C.8 APPLY METAL (Metal 2)
C.9 Apply photoresist
C.10 PATTERN METAL
C.11 Develop photoresist
C.12 Etch metal
C.13 Strip photoresist

49. APPLY PASSIVATION
50. Apply photoresist
51. PATTERN PAD OPENINGS
52. Develop photoresist
53. Etch passivation
54. Strip photoresist
55. ASSEMBLE, PACKAGE AND TEST
Metal 1 Mask
Capacitor

P-channel MOSFET

Resistor

n-channel MOSFET
End of Lecture 17