EE 330
Lecture 2

Basic Concepts
Quiz 1

The International Technology Roadmap for Semiconductors (ITRS) makes predictions on challenges and trends in the semiconductor industry. What is the ITRS projecting for the supply voltage of digital ICs in 10 years?
And the number is ....
And the number is ....
Quiz 1

The International Technology Roadmap for Semiconductors (ITRS) makes predictions on challenges and trends in the semiconductor industry. What is the ITRS projecting for the supply voltage of digital ICs in 10 years?

Solution: Approximately 600mV
Review from Last Time

• Semiconductor Industry is One of the Largest Sectors in the World Economy and Growing
• All Initiatives Driven by Economic Opportunities and Limitations
• Rapidly Growing Device Count and Rapidly Shrinking Feature Sizes (Moore’s Law?)
• Designers Must Handle Incredible Complexity Yet Work in Large Teams and Make Almost No Mistakes
• Understand the Big Picture and Solve the Right Problem
Review from Last Time

ITRS Technology Predictions

ITRS 2004 Supply Voltage Predictions

Volts

Analog

Digital

Year

Review from Last Time

ITRS Technology Predictions

Minimum ASIC Gate Length

Length in nm

YEAR

How can complex circuits with a very large number of transistors be efficiently designed with low probability of error?

• Many designers often work on a single design

• Single error in reasoning, in circuit design, or in implementing circuit on silicon generally results in failure

• Design costs and fabrication costs for test circuits are very high
  – Design costs for even rather routine circuits often a few million dollars and some much more
  – Masks and processing for state of the art processes often between $1M and $2M

• Although much re-use is common on many designs, considerable new circuits that have never been designed or tested are often required

• Time to market critical – missing a deadline by even a week or 2 may kill the market potential
How can complex circuits with a very large number of transistors be efficiently designed with low probability of error?

- CAD tools and CAD-tool environment critical for success today
- Small number of VLSI CAD toolset vendors
- CAD toolset helps the engineer and it is highly unlikely the CAD tools will replace the design engineer
- Major emphasis in this course on using toolset to support the design process
CAD Environment for Integrated Circuit Design

• Typical Tool Flow
  – (See Chapter 8 of Text)

• Laboratory Experiments in Course
VLSI Design Flow Summary

Analog Flow

System Description

Circuit Design (Schematic)

SPICE Simulation

Layout/DRC...

Extraction

Back-Annotated Extraction

Fabrication

Post-Layout Simulation

Print Circuit Schematic

DRC Report

LVS

LVS Output File

Post-Layout Simulation

Simulation Results

Spectre (or HSPICE)

Assura DRC

Assura RCX

Assura LVS

Schematic Editor

Cadence Virtuoso

Spectre (or HSPICE)
VLSI Design Flow Summary

Digital Flow

1. System Description
2. Verilog Description
3. Verilog Simulation
4. Synthesis (Synopsys)
5. Simulate (Gate Level)
6. Place and Route (SoC Encounter)
7. Circuit Schematic (Cadence)
8. DRC
10. Fabrication
11. Post-Layout Simulation

- VHDL Simulation Results and
  And Comparison with System Specs.
- Print Circuit Schematic
- Connectivity Report and
  Show Routing to TA
- DRC Report
- LVS
- LVS Output File
- Post-Layout Simulation
VLSI Design Flow Summary

**Mixed Signal Flow (Digital Part)**

1. **System Description**
2. **VHDL Description**
3. **VHDL Simulation**
4. **Synthesis (Synopsys)**
   - **DEF or GDS2 File**
   - **Simulate (Gate Level)**
   - **Gate-level Simulation**
5. **Place and Route (Silicon Ensemble)**
   - **DEF or GDS2 File**
6. **DRC**
   - **DRC Report**
7. **Back-Annotated Extraction**
8. **Post-Layout Simulation**
9. **Circuit Schematic (Cadence)**
   - **LVS**
   - **LVS Output File**
   - **Post-Layout Simulation**
10. **Print Circuit Schematic**
11. **VHDL Simulation Results and And Comparison with System Specs.**
VLSI Design Flow Summary

Mixed-Signal Flow (Analog Part)

System Description

Circuit Design (Schematic)

SPICE Simulation

Layout/DRC

Extraction

Back-Annotated Extraction

LVS

LVS Output File

Post-Layout Simulation

Print Circuit Schematic

Simulation Results

DRC Report
VLSI Design Flow Summary

Mixed-Signal Flow (Analog-Digital Merger)

- A: Layout Merge
- C: Extraction
- B: Schematic Merge
- D: LVS/DRC Output Files

Flow Diagram:
- A → C (Layout Merge → Extraction)
- C → LVS/DRC
- D → LVS/DRC
- LVS/DRC → Post-Layout Simulation
- Fabrication

Notations:
- Show Layout to TA
- LVS/DRC Output Files
- Simulation Results
Comments

• The Analog Design Flow is often used for small digital blocks or when particular structure or logic styles are used in digital systems

• Variants of these flows are widely used and often personalized by a given company or for specific classes of circuits
- 6 inches to 12 inches in diameter
- All complete cells ideally identical
- flat edge
- very large number of die if die size is small
Feature Size

Feature size is the minimum lateral feature size that can be reliably manufactured.

Often given as either feature size or pitch.

Minimum feature size often identical for different features.
What is meant by “reliably”

Yield is acceptable if a very large number of these features are made

If $P$ is the probability that a feature is good

$n$ is the number of features on an IC

$Y$ is the yield

\[ Y = P^n \]

\[ P = e^{\frac{\log Y}{n}} \]
Example: How reliable must a feature be?

\[ n = 5 \times 10^3 \]
\[ Y = 0.9 \]

\[ P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5 \times 10^3}} = 0.999979 \]

But is \( n = 5000 \) large enough?

More realistically \( n = 5 \times 10^9 \)

\[ P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5 \times 10^9}} = 0.999999999979 \]

Extremely high reliability must be achieved in all processing steps to obtain acceptable yields in state of the art processes.
Feature Size

• Typically minimum length of a transistor
• Often minimum width or spacing of a metal interconnect (wire)
• Point of “bragging” by foundries
  – Drawn length and actual length differ
• Often specified in terms of pitch
  – Pitch approximately equal to twice minimum feature size
Feature Size Evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Feature Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mid 70’s</td>
<td>25µ</td>
</tr>
<tr>
<td>2005</td>
<td>90nm</td>
</tr>
<tr>
<td>2010</td>
<td>20nm</td>
</tr>
<tr>
<td>2020</td>
<td>10nm</td>
</tr>
</tbody>
</table>

\[ 1\mu = 10^3 \text{ nm} = 10^{-6} \text{ m} = 10^4 \text{ Å} \]
MOS Transistor

Active

Poly
MOS Transistor

Source

Drain

Gate

Region of Interest (Channel)

Drawn Length and Width Shown
MOS Transistor

Actual Drain and Source at Edges of Channel
MOS Transistor

Effective Width and Length Generally Smaller than Drawn Width and Length
Technology Nomenclature

- **SSI** Small Scale Integration 1-100
- **MSI** Medium Scale Integration 100-10^3
- **LSI** Large Scale Integration 10^3-10^5
- **VLSI** Very Large Scale Integration 10^5-10^6

Any design in a process capable of incorporating a large number of devices is generally termed a VLSI design.
Device and Die Costs

Consider the high-volume incremental costs of manufacturing integrated circuits

Example: Assume an 8” wafer in a 0.25µ process costs $800

Determine the number of minimum-sized transistors that can be fabricated on this wafer and the cost per transistor. Neglect spacing and interconnect.

Solution:

\[ n_{\text{trans}} \approx \frac{A_{\text{wafer}}}{A_{\text{trans}}} = \frac{\pi (4in)^2}{(0.25\mu)^2} = 5.2E11 \]

\[ C_{\text{trans}} = \frac{C_{\text{wafer}}}{n_{\text{trans}}} = \frac{\$800}{5.2E11} = \$15.4E-9 \]

Note: the device count may be decreased by a factor of 10 or more if Interconnect and spacing is included but even with this decrease, the cost per transistor is still very low!
Device and Die Costs

\[ C_{\text{per unit area}} \approx \$2.5 / cm^2 \]

Example: If the die area of the 741 op amp is 1.8mm², determine the cost of the silicon needed to fabricate this op amp

\[ C_{741} = \$2.5 / cm^2 \cdot (1.8mm^2) \approx \$0.05 \]

Actual integrated op amp will be dramatically less if bonding pads are not needed
Size of Atoms and Molecules in Semiconductor Processes

Silicon:  
- Average Atom Spacing: 2.7 Å
- Lattice Constant: 5.4 Å

$\text{SiO}_2$:  
- Average Atom Spacing: 3.5 Å

Air:  
- Breakdown Voltage: $5 \text{ to } 10 \text{MV/cm} = 5 \text{ to } 10 \text{mV/Å}$
- $20 \text{KV/cm}$

Physical size of atoms and molecules place fundamental limit on conventional scaling approaches
End of Lecture 2