EE 330
Lecture 21

Bipolar Devices
Thyristors
  SCRs
  Triacs
Review from Last Lecture

A-A' Section

vertical npn

B-B' Section

lateral pnp
Review from Last Lecture

B-B’ Section

p-channel JFET
Review from Last Lecture

vertical npn

lateral pnp
Review from Last Lecture

Diode (capacitor)

Resistor

n-channel JFET
The vertical npn transistor

- Emitter area only geometric parameter that appears in basic device model
- Transistor much larger than emitter
- Base region very thin to provide large $\beta$
- Multiple-emitter devices often used (TTL Logic) and don’t significantly increase area
- The “flagship” device in most bipolar processes
Enhancement and Depletion MOS Devices

- Enhancement Mode n-channel devices
  \[ V_T > 0 \]
- Enhancement Mode p-channel devices
  \[ V_T < 0 \]
- Depletion Mode n-channel devices
  \[ V_T < 0 \]
- Depletion Mode p-channel devices
  \[ V_T > 0 \]
Enhancement and Depletion MOS Devices

- Depletion mode devices require only one additional mask step
- Older n-mos and p-mos processes usually had depletion device and enhancement device
- Depletion devices usually not available in CMOS because applications usually do not justify the small increasing costs in processing
The JFET

In triode region under reverse bias (channel thins)
The JFET

In saturation (pinch-off) region under reverse bias and large $V_{DS}$ (channel pinches off)
The JFET

Square-law model of n-channel JFET

\[ I_D = \begin{cases} 
0 & \text{if } V_{GS} < V_P \\
\frac{2I_{DSS}}{V_P^2} \left( V_{GS} - V_P - \frac{V_{DS}}{2} \right) V_{DS} & \text{if } V_{GS} > V_P, \ V_{DS} < V_{GS} - V_P \\
I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 & \text{if } V_{GS} > V_P, \ V_{DS} < V_{GS} - V_P 
\end{cases} \]

- Functionally identical to the square-law model of MOSFET
- Parameters \( I_{DSS} \) and \( V_P \) characterize the device
- \( I_{DSS} \) proportional to \( W/L \) where \( W \) and \( L \) are width and length of n+ diff
- \( V_P \) is negative for n-channel device, positive for p-channel device thus JFET is depletion mode device
- Must not forward bias GS junction by over about 300mV or excessive base current will flow
- Widely used as input stage for bipolar op amps
The Schottky Diode

- Metal-Semiconductor Junction
- One contact is ohmic, other is rectifying
- Not available in all processes
- Relatively inexpensive adder in some processes
- Lower cut-in voltage than pn junction diode
- High speed
The MESFET

- Metal-Semiconductor Junction for Gate
- Drain and Source contacts ohmic, other is rectifying
- Usually not available in standard CMOS processes
- Must not forward bias very much
- Lower cut-in voltage than pn junction diode
- High speed
The Thyristor

A bipolar device in CMOS Processes

Consider a Bulk-CMOS Process

Have formed a lateral pnnpn device!

Will spend some time studying pnnpn devices
Thyristors

The good and the bad!
Thyristors

The good

SCRs
Triacs

The bad

Parasitic Device that can destroy integrated circuits
The SCR

Silicon Controlled Rectifier

- Widely used to switch large resistive or inductive loads
- Widely used in the power electronics field
- Widely used in consumer electronic to interface between logic and power

![Diagram of SCR]

Usually made by diffusions in silicon

Consider first how this 4-layer 3-junction device operates
Operation of the SCR

Not actually separated but useful for describing operation
Consider a small positive bias (voltage or current) on the gate \( V_{GC} < 0.5V \) and a positive and large voltage \( V_F \)

Will have \( V_{C1} \geq V_F - 0.5V \)

Thus \( Q_1 \) has a large positive voltage on its collector

Since \( V_{BE1} \) is small, \( I_{C1} \) will be small as will \( I_{C2} \) so diode equation governs BE junction of \( Q_1 \)

\( I_F \) will be very small
Operation of the SCR

Now let bias on the gate increase ($V_{GC}$ around 0.6V) so $Q_1$ and $Q_2$ in FA

From diode equation, base voltage $V_{BE1}$ will increase and collector current $I_{C1}$ will increase

Thus base current $I_{B2}$ will increase as will the collector current of $I_{C2}$

Under assumption of operation in FA region get expression

$$I_{B1} = I_G + \beta_1 \beta_2 I_{B1}$$

This is regenerative feedback (actually can show pole in RHP)
Operation of the SCR

\[ V_{C1} \geq V_F - 0.5V \]

Under assumption of operation in FA region get expression

\[ I_{B1} = I_G + \beta_1 \beta_2 I_{B1} \]

What will happen with this is regenerative feedback?

- \( I_G \) can now be removed and current will continue to flow
- \( I_{C1} \) will continue to increase and drive \( Q_1 \) into SAT

This will try to drive \( V_A \) towards 0.9V

- The current in \( V_F \) will go towards \( \infty \)

The SCR will self-destruct because of excessive heating!

Too bad the circuit self-destructed because the small gate current was able to control a lot of current!
Operation of the SCR

Consider a modified application by adding a load (depicted as $R_L$)

All operation is as before, but now, after the triggering occurs, the voltage $V_F$ will drop to approximately 0.8 V and the voltage $V_{CC} - .8$ will appear across $R_L$

If $V_{CC}$ is very large, the SCR has effectively served as a switch putting $V_{CC}$ across the load and after triggering occurs, $I_G$ can be removed!

But, how can we turn it off? Will discuss that later
Operation of the SCR

The Ideal SCR

\[ I_F = f(V_F, V_G) \]

\( I_H \) is very small
\( I_{G1} \) is small (but not too small)

\[ I_F = f(V_F, V_G) \]

called the SCR model

As for MOSFET, Diode, and BJT, several models for SCR can be developed.
Operation of the SCR

Operation with the Ideal SCR

Load Line: \[ V_{CC} = I_F R_L + V_F \]

Analysis: \[ V_{CC} = I_F R_L + V_F \]
\[ I_{FI} = f(V_F, V_G) \]

The solution of these two equations is at the intersection of the load line and the device characteristics.

Note three intersection points:
- Two (upper and lower) are stable equilibrium points, one is not.

When operating at upper point, \( V_F = 0 \) so \( V_{CC} \) appears across \( R_L \) \( \implies \) We say SCR is ON

When operating at lower point, \( I_F \) approx 0 so no signal across \( R_L \) \( \implies \) We say SCR is OFF

When \( I_G = 0 \), will stay in whatever state it was in
Operation of the SCR

Operation with the Ideal SCR

Now assume it was initially in the OFF state and then a gate current was applied.

\[ V_{CC} = I_F R_L + V_F \]
\[ I_{FI} = f(V_F, V_G) \]

Now there is a single intersection point so a unique solution.

The SCR is now ON.

Removing the gate current will return to the previous solution but it will remain in the ON state.
Operation of the SCR

Operation with the Ideal SCR

Turning SCR off when $I_G=0$

Reduce $V_{CC}$ so that $V_{CC}/R_L$ goes below $I_H$

This will provide a single intersection point

$V_{CC}$ can then be increased again and SCR will stay off

Must not increase $V_{CC}$ above $V_{BGF0}$ else will turn on
Operation of the SCR

Operation with the Ideal SCR

Turning SCR off when $I_G = 0$
Operation of the SCR

Operation with the Ideal SCR

Often $V_{CC}$ is an AC signal (often 110V)

SCR will turn off whenever AC signal goes negative
Operation of the SCR

Operation with the Ideal SCR

Turning SCR off when \( I_G > 0 \)

Reduce \( V_{CC} \) so that \( V_{CC}/R_L \) goes below \( I_H \)

This will provide a single intersection point

But when \( V_{CC} \) is then increased SCR will again turn on

Not practical to turn it off if \( I_G \) is very large
Operation of the SCR

Operation with the Ideal SCR

Duty cycle control of $R_L$

- $V_{AC}$
- $t$
- $V_{LOAD}$
- $I_{GATE}$
Operation of the SCR

Operation with the Ideal SCR

Duty cycle control of $R_L$

![Diagram showing the operation of an SCR with duty cycle control of $R_L$. The diagram includes a graph with $V_{LOAD}$ and $I_{GATE}$, and a circuit diagram with $V_{AC}$, $R_L$, $I_F$, $V_F$, and $V_G$.]
Operation of the SCR

Operation with the actual SCR
Operation of the SCR

Operation with the actual SCR

\[ V_{BR} \]

Currents and voltages for different gate currents:

\[ I_{G4} > I_{G3} > I_{G2} > I_{G1} = 0 \]

\[ V_{BRF0} \]
Operation of the SCR

Operation with the actual SCR

Still two stable equilibrium points and one unstable point
Operation of the SCR

Operation with the actual SCR

To turn on, must make $I_G$ large enough to have single intersection point.
$I_H$ is the holding current

$I_L$ is the latching current (current immediately after turn-on)

$V_{BGF0}$ is the forward break-over voltage

$V_{BRR}$ is the reverse break-down voltage

$I_{GT}$ is the gate trigger current

$V_{GT}$ is the gate trigger voltage
SCR Terminology

Issues and Observations

- Trigger parameters ($V_{GT}$ and $I_{GT}$) highly temperature dependent
- Want gate “sensitive” but not too sensitive (to avoid undesired triggering)
- SCR can switch very large currents but power dissipation is large
- Heat sinks widely used to manage power
- Trigger parameters affected by both environment and application
- Trigger parameters generally dependent upon $V_F$
- Exceeding $V_{BRR}$ will usually destroy the device
- Exceeding $V_{BGF0}$ will destroy some devices
- Lack of electronic turn-off unattractive in some applications
- Can be used in alarm circuits to attain forced reset
- Maximum 50% duty cycle in AC applications is often not attractive
End of Lecture 21