Thyristors
The JFET

Square-law model of n-channel JFET

\[
I_b = \begin{cases} 
0 & V_{GS} < V_P \\
\frac{2I_{DSS}}{V_P^2} \left( V_{GS} - V_P - \frac{V_{DS}}{2} \right)V_{DS} & V_{GS} > V_P, V_{DS} < V_{GS} - V_P \\
I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 & V_{GS} > V_P, V_{DS} < V_{GS} - V_P 
\end{cases}
\]

- Functionally identical to the square-law model of MOSFET
- Parameters \( I_{DSS} \) and \( V_P \) characterize the device
- \( I_{DSS} \) proportional to \( W/L \) where \( W \) and \( L \) are width and length of n+ diff
- \( V_P \) is negative for n-channel device, positive for p-channel device thus JFET is depletion mode device
- Must not forward bias GS junction by over about 300mV or excessive base current will flow

Review from Last Lecture
The Thyristor
A bipolar device in CMOS Processes

Consider a Bulk-CMOS Process

Have formed a lateral pnpn device!
**The SCR**

**Silicon Controlled Rectifier**

- Widely used to switch large resistive or inductive loads
- Widely used in the power electronics field
- Widely used in consumer electronic to interface between logic and power

Usually made by diffusions in silicon

Consider first how this 4-layer 3-junction device operates
Review from Last Lecture

Operation of the SCR

Not actually separated but useful for describing operation
The Ideal SCR

\[ I_F = f(V_F, V_G) \]

\( I_H \) is very small
\( I_{G1} \) is small (but not too small)

\[ I_F = f(V_F, V_G) \]

called the SCR model

As for MOSFET, Diode, and BJT, several models for SCR can be developed
Review from Last Lecture

**Operation of the SCR**

**Operation with the Ideal SCR**

Now assume it was initially in the OFF state and then a gate current was applied.

\[ V_{CC} = I_F R_L + V_F \]

\[ I_{FI} = f(V_F, V_G) \]

Now there is a single intersection point so a unique solution.

The SCR is now ON.

Removing the gate current will return to the previous solution but it will remain in the ON state.
Review from Last Lecture

Operation of the SCR

Operation with the Ideal SCR

Duty cycle control of $R_L$

$V_{LOAD}$

$I_{GATE}$

$V_{AC}$

$R_L$

$I_F$

$V_F$

$V_G$
Review from Last Lecture

Operation of the SCR

Operation with the actual SCR

\[ I_F \]

\[ I_H \]

\[ V_{BRR} \]

\[ V_F \]

\[ I_F \]

\[ I_G \]

\[ V_G \]

\[ V_{BF0} \]

\[ I_{G4} > I_{G3} > I_{G2} > I_{G1} = 0 \]
Review from Last Lecture

Operation of the SCR

Operation with the actual SCR

To turn on, must make $I_G$ large enough to have single intersection point
Thyristors

The good

- SCRs
- Triacs

The bad

Parasitic Device that can destroy integrated circuits
Limitations of the SCR

1. Only conducts in one direction
2. Can’t easily turn off (though not major problem in AC switching)
Bi-directional switching

Use two cross-coupled SCRs

Limitations

Size and cost overhead with this solution
Inconvenient triggering since $G_1$ and $G_2$ WRT different terminals
Bi-directional switching with the Triac

- Has two cross-coupled SCRs!
- Manufactured by diffusions
- Single Gate Control
The Triac

- Can define two cross-coupled transistor pairs in each side

As for SCR, both circuits have regenerative feedback

Can turn ON in either direction with either positive or negative current

Defines 4 quadrants for operation

\[
\begin{align*}
V_{MT2} &> V_{MT1} & & V_{G-MT1} > 0 & & \text{Quadrant 1} \\
V_{MT2} &> V_{MT1} & & V_{G-MT1} < 0 & & \text{Quadrant 2} \\
V_{MT2} &< V_{MT1} & & V_{G-MT1} < 0 & & \text{Quadrant 3} \\
V_{MT2} &< V_{MT1} & & V_{G-MT1} > 0 & & \text{Quadrant 4}
\end{align*}
\]

Usually use only one quadrant for control

Different voltage, duration strategies exist for triggering

Can’t have single quadrant control with two SCRs
The Triac

Consider the basic Triac circuit
The Basic Triac Circuit

Assume ideal Triac

Load Line: \( V_{CC} = I_T R_L + V_{TR} \)

Analysis:
\[
V_{AC} = I_T R_L + V_{TR} \\
I_{FI} = f(V_{TR}, V_{GT1})
\]

The solution of these two equations is at the intersection of the load line and the device characteristics

Two stable operating points for both positive and negative \( V_{AC} \)
The Basic Triac Circuit

Assume ideal Triac

Load Line: \( V_{CC} = I_T R_L + V_{TR} \)

Analysis: \( V_{AC} = I_T R_L + V_{TR} \)

\( I_{Fl} = f(V_{TR}, V_{GT2}) \)

Single solution for both positive and negative \( V_{AC} \)

Thus this state turns on the Triac for any input
The Actual Triac

\[ I_T \]

\[ V_{TR} \]

\[ I_{G4} > I_{G3} > I_{G2} > I_{G1} = 0 \]
The Actual Triac in Basic Circuit

$I_G=0$ State

Two stable operating points
The Actual Triac in Basic Circuit

Can turn on for either positive or negative $V_{AC}$ with single gate signal
Phase controlled bidirectional switching with Triacs
Thyristor Types

Some of the more major types:

- SCR
- Triac
- Bidirectional Phase-controlled thyristors (BCT)
- LASCR (Light activated SCR)
- Gate Turn-off thyristors (GTO)
- FET-controlled thyristors (FET-CTH)
- MOS Turn-off thyristors (MTO)
- MOS-controlled thyristors (MCT)
Thanks to Prof. Ajjarapu for providing the following slides:

**APPLICATIONS**

- Pulse Power
- Crowbars
- Ignitron Replacement

**KEY PARAMETERS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DRM}$</td>
<td>4500V</td>
</tr>
<tr>
<td>$I_{T(AV)}$</td>
<td>760A</td>
</tr>
<tr>
<td>$I_{TSM}$</td>
<td>13000A</td>
</tr>
<tr>
<td>$dl/dt$</td>
<td>5000A/μS</td>
</tr>
</tbody>
</table>
Thanks to Prof. Ajjarapu for providing the following slides:

THE BIDIRECTIONAL CONTROL THYRISTOR (BCT)

by

Kenneth M. Thomas, Björn Backlund, Orhan Toker
ABB Semiconductors AG, CH5600 Lenzburg, Switzerland

Björn Thorvaldsson
ABB Power Systems AB, S-721 64 Västerås, Sweden

ABSTRACT
The Bidirectional Control Thyristor (BCT) is a new concept for high power thyristors integrated on a single silicon wafer with separate gate contacts. This unique design, based on free-floating silicon technology, successfully overcomes the traditional problems of interference experienced by bidirectional thyristors during dynamic operation which previously prevented the use of such devices. Such components are suitable for applications at high voltages like a normal thyristor but where triacs can no longer be used.
High Current, High Voltage Solid State Discharge Switches for Electromagnetic Launch Applications

A. Welleman, R. Leutwyler, J. Waldmeyer
ABB Switzerland Ltd, Semiconductors - CH-5600 Lenzburg

Abstract—This presentation is about the work done on design, built-up, production and test of ready-to-use solid state switch assemblies using Thyristor- or IGCT technology. The presented thyristor switch assemblies, using 120 mm wafer size, are made to switch 3MJ stored energy into a load. The maximum charge voltage of the assembly is 12 kVdc, current capability more than 260kA@tp=3.3ms and a pulse repetition rate of up to 6 shots per minute with convection air cooling. New very large thyristors with 150 mm wafer diameter will be available from fall 2008. As second a 70 kA/21kVdc switch using IGCT technology will be presented. The switch is designed for fast discharge in the micro-second range and has a very high di/dt capability. Because for adapted standard products which can fulfill the requirements for pulsed applications. Beside the semiconductor devices, ABB is also in the position to supply complete custom made ready-to-use solid state switch assemblies including clamping, triggering, cooling and with application oriented testing. The presentation describes both, the loose semiconductor components as well as some custom made solid state switches for single pulse or low repetition rate pulsing.

II. DEVICE TECHNOLOGY

2008 Paper
Thanks to Prof. Ajjarapu for providing the following slides:

Fig.3: Thyristor Switch Assembly A-STP 5742U-18-CC
Thanks to Prof. Ajjarapu for providing the following slides:

- **Auxiliary Cathode Lead (Red)**
  Extends cathode potential to the control circuit.

- **Gate Lead (White)**

- **Stud-Anode**

**Stud-Mounted SCR**
110 Amp RMS Rating
Cross-section of a BCT wafer showing the antiparallel arrangement of the A and B component thyristors. The arrows indicate the convention of forward blocking for A and B.
Thanks to Prof. Ajjarapu for providing the following slides:

Thyristor Valve - 12 Pulse Converter (6.5Kv, 1568 Amp, Water cooled)
Many different structures used to build thyristors

Range from low power devices to extremely high power devices

Often single-wafer solutions for high power applications

Usually formed by diffusions

Widely used throughout society but little visibility

Applications somewhat restricted
Thyristors

The good

- SCRs
- Triacs

The bad

Parasitic Device that can destroy integrated circuits
The Thyristor

A bipolar device in CMOS Processes

Consider a Bulk-CMOS Process

If this parasitic SCR turns on, either circuit will latch up or destroy itself.

Guard rings must be included to prevent latchup.

Design rules generally include provisions for guard rings.
MOS and Bipolar Area Comparisons

How does the area required to realize a MOSFET compare to that required to realize a BJT?

Will consider a minimum-sized device in both processes
TABLE 2C.2
Design rules for a typical bipolar process (λ = 2.5 µ)
(See Table 2C.3 in color plates for graphical interpretation)

<table>
<thead>
<tr>
<th></th>
<th>Dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>n⁺ buried collector diffusion (Yellow, Mask #1)</td>
</tr>
<tr>
<td></td>
<td>1.1 Width</td>
</tr>
<tr>
<td></td>
<td>1.2 Overlap of p-base diffusion (for vertical npn)</td>
</tr>
<tr>
<td></td>
<td>1.3 Overlap of n⁺ emitter diffusion (for collector contact of vertical npn)</td>
</tr>
<tr>
<td></td>
<td>1.4 Overlap of p-base diffusion (for collector and emitter of lateral npn)</td>
</tr>
<tr>
<td></td>
<td>1.5 Overlap of n⁺ emitter diffusion (for base contact of lateral npn)</td>
</tr>
<tr>
<td>2.</td>
<td>Isolation diffusion (Orange, Mask #2)</td>
</tr>
<tr>
<td></td>
<td>2.1 Width</td>
</tr>
<tr>
<td></td>
<td>2.2 Spacing</td>
</tr>
<tr>
<td></td>
<td>2.3 Distance to n⁺ buried collector</td>
</tr>
<tr>
<td>3.</td>
<td>p-base diffusion (Brown, Mask #3)</td>
</tr>
<tr>
<td></td>
<td>3.1 Width</td>
</tr>
<tr>
<td></td>
<td>3.2 Spacing</td>
</tr>
<tr>
<td></td>
<td>3.3 Distance to isolation diffusion</td>
</tr>
<tr>
<td></td>
<td>3.4 Width (resistor)</td>
</tr>
<tr>
<td></td>
<td>3.5 Spacing (as resistor)</td>
</tr>
<tr>
<td>4.</td>
<td>n⁺ emitter diffusion (Green, Mask #4)</td>
</tr>
<tr>
<td></td>
<td>4.1 Width</td>
</tr>
<tr>
<td></td>
<td>4.2 Spacing</td>
</tr>
<tr>
<td></td>
<td>4.3 p-base diffusion overlap of n⁺ emitter diffusion (emitter in base)</td>
</tr>
<tr>
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<td>4.4 Spacing to isolation diffusion (for collector contact)</td>
</tr>
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<td>4.5 Spacing to p-base diffusion (for base contact of lateral npn)</td>
</tr>
<tr>
<td></td>
<td>4.6 Spacing to p-base diffusion (for collector contact of vertical npn)</td>
</tr>
</tbody>
</table>
5. Contact (Black, Mask #5)
   5.1 Size (exactly)  
   5.2 Spacing  
   5.3 Metal overlap of contact  
   5.4 n\(^+\) emitter diffusion overlap of contact  
   5.5 p-base diffusion overlap of contact  
   5.6 p-base to n\(^+\) emitter  
   5.7 Spacing to isolation diffusion  

6. Metalization (Blue, Mask #6)
   6.1 Width  
   6.2 Spacing  
   6.3 Bonding pad size  
   6.4 Probe pad size  
   6.5 Bonding pad separation  
   6.6 Bonding to probe pad  
   6.7 Probe pad separation  
   6.8 Pad to circuitry  
   6.9 Maximum current density  

7. Passivation (Purple, Mask #7)
   7.1 Minimum bonding pad opening  
   7.2 Minimum probe pad opening
Consider Initially the Emitter in the BJT surrounded by a base region
<table>
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<tbody>
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</tr>
<tr>
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<td>Width</td>
<td>3$\lambda$</td>
</tr>
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<td>Overlap of p-base diffusion (for vertical npn)</td>
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</tr>
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<td>Isolation diffusion (Orange, Mask #2)</td>
<td></td>
</tr>
<tr>
<td>2.1</td>
<td>Width</td>
<td>4$\lambda$</td>
</tr>
<tr>
<td>2.2</td>
<td>Spacing</td>
<td>24$\lambda$</td>
</tr>
<tr>
<td>2.3</td>
<td>Distance to n$^+$ buried collector</td>
<td>14$\lambda$</td>
</tr>
<tr>
<td>3.</td>
<td>p-base diffusion (Brown, Mask #3)</td>
<td></td>
</tr>
<tr>
<td>3.1</td>
<td>Width</td>
<td>3$\lambda$</td>
</tr>
<tr>
<td>3.2</td>
<td>Spacing</td>
<td>5$\lambda$</td>
</tr>
<tr>
<td>3.3</td>
<td>Distance to isolation diffusion</td>
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<td>3.4</td>
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<td>4.2</td>
<td>Spacing</td>
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<tr>
<td>4.3</td>
<td>p-base diffusion overlap of n$^+$ emitter diffusion (emitter in base)</td>
<td>2$\lambda$</td>
</tr>
<tr>
<td>4.4</td>
<td>Spacing to isolation diffusion (for collector contact)</td>
<td>12$\lambda$</td>
</tr>
<tr>
<td>4.5</td>
<td>Spacing to p-base diffusion (for base contact of lateral pnp)</td>
<td>6$\lambda$</td>
</tr>
<tr>
<td>4.6</td>
<td>Spacing to p-base diffusion (for collector contact of vertical npn)</td>
<td>6$\lambda$</td>
</tr>
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   5.1 Size (exactly)
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   5.3 Metal overlap of contact
   5.4 $n^+$ emitter diffusion overlap of contact
   5.5 p-base diffusion overlap of contact
   5.6 p-base to $n^+$ emitter
   5.7 Spacing to isolation diffusion
   \[4\lambda \times 4\lambda\]

6. Metalization (Blue, Mask #6)
   6.1 Width
   6.2 Spacing
   6.3 Bonding pad size
   6.4 Probe pad size
   6.5 Bonding pad separation
   6.6 Bonding to probe pad
   6.7 Probe pad separation
   6.8 Pad to circuitry
   6.9 Maximum current density
   \[100 \mu \times 100 \mu\]
   \[75 \mu \times 75 \mu\]
   \[50 \mu\]
   \[30 \mu\]
   \[30 \mu\]
   \[40 \mu\]
   \[0.8 \text{mA/\mu width}\]

7. Passivation (Purple, Mask #7)
   7.1 Minimum bonding pad opening
   7.2 Minimum probe pad opening
   \[90 \mu \times 90 \mu\]
   \[65 \mu \times 65 \mu\]
From design rules (left to right) 4.3, 5.1, 5.4, 5.6, 5.5
**TABLE 2C.2**  
Design rules for a typical bipolar process ($\lambda = 2.5 \mu$)  
(See Table 2C.3 in color plates for graphical interpretation)

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<td>$2\lambda$</td>
</tr>
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<td>2.</td>
<td>Isolation diffusion (Orange, Mask #2)</td>
<td></td>
</tr>
<tr>
<td>2.1</td>
<td>Width</td>
<td>$4\lambda$</td>
</tr>
<tr>
<td>2.2</td>
<td>Spacing</td>
<td>$24\lambda$</td>
</tr>
<tr>
<td>2.3</td>
<td>Distance to $n^+$ buried collector</td>
<td>$14\lambda$</td>
</tr>
<tr>
<td>3.</td>
<td>p-base diffusion (Brown, Mask #3)</td>
<td></td>
</tr>
<tr>
<td>3.1</td>
<td>Width</td>
<td>$3\lambda$</td>
</tr>
<tr>
<td>3.2</td>
<td>Spacing</td>
<td>$5\lambda$</td>
</tr>
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<td>Distance to isolation diffusion</td>
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<td>Width (resistor)</td>
<td>$3\lambda$</td>
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<td>3.5</td>
<td>Spacing (as resistor)</td>
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</tr>
<tr>
<td>4.</td>
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<td>$3\lambda$</td>
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<tr>
<td>4.2</td>
<td>Spacing</td>
<td>$3\lambda$</td>
</tr>
<tr>
<td>4.3</td>
<td>p-base diffusion overlap of $n^+$ emitter diffusion (emitter in base)</td>
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</tr>
<tr>
<td>4.4</td>
<td>Spacing to isolation diffusion (for collector contact)</td>
<td>$12\lambda$</td>
</tr>
<tr>
<td>4.5</td>
<td>Spacing to p-base diffusion (for base contact of lateral pnp)</td>
<td>$6\lambda$</td>
</tr>
<tr>
<td>4.6</td>
<td>Spacing to p-base diffusion (for collector contact of vertical npn)</td>
<td>$6\lambda$</td>
</tr>
</tbody>
</table>
Add n+ buried for collector

From design rule 1.2
### TABLE 2C.2
Design rules for a typical bipolar process ($\lambda = 2.5 \mu$)
*(See Table 2C.3 in color plates for graphical interpretation)*

<table>
<thead>
<tr>
<th>1. n$^+$ buried collector diffusion (Yellow, Mask #1)</th>
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</thead>
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<tr>
<td>1.1 Width</td>
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</tr>
<tr>
<td>1.2 Overlap of p-base diffusion (for vertical n/p)</td>
<td>$2\lambda$</td>
</tr>
<tr>
<td>1.3 Overlap of n$^+$ emitter diffusion (for collector contact of vertical n/p)</td>
<td>$2\lambda$</td>
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<tr>
<td>1.5 Overlap of n$^+$ emitter diffusion (for base contact of lateral pnp)</td>
<td>$2\lambda$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>2. Isolation diffusion (Orange, Mask #2)</th>
<th>Dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1 Width</td>
<td>$4\lambda$</td>
</tr>
<tr>
<td>2.2 Spacing</td>
<td>$24\lambda$</td>
</tr>
<tr>
<td>2.3 Distance to n$^+$ buried collector</td>
<td>$14\lambda$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>3. p-base diffusion (Brown, Mask #3)</th>
<th>Dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td>3.1 Width</td>
<td>$3\lambda$</td>
</tr>
<tr>
<td>3.2 Spacing</td>
<td>$5\lambda$</td>
</tr>
<tr>
<td>3.3 Distance to isolation diffusion</td>
<td>$14\lambda$</td>
</tr>
<tr>
<td>3.4 Width (resistor)</td>
<td>$5\lambda$</td>
</tr>
<tr>
<td>3.5 Spacing (as resistor)</td>
<td>$3\lambda$</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>4. n$^+$ emitter diffusion (Green, Mask #4)</th>
<th>Dimension</th>
</tr>
</thead>
<tbody>
<tr>
<td>4.1 Width</td>
<td>$3\lambda$</td>
</tr>
<tr>
<td>4.2 Spacing</td>
<td>$3\lambda$</td>
</tr>
<tr>
<td>4.3 p-base diffusion overlap of n$^+$ emitter diffusion (emitter in base)</td>
<td>$2\lambda$</td>
</tr>
<tr>
<td>4.4 Spacing to isolation diffusion (for collector contact)</td>
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<td>4.5 Spacing to p-base diffusion (for base contact of lateral pnp)</td>
<td>$6\lambda$</td>
</tr>
<tr>
<td>4.6 Spacing to p-base diffusion (for collector contact of vertical n/p)</td>
<td>$6\lambda$</td>
</tr>
</tbody>
</table>
Add n-epi region from design rules 2.3 and 3.3
5. Contact (Black, Mask #5)
   5.1 Size (exactly) \(4\lambda \times 4\lambda\)
   5.2 Spacing \(2\lambda\)
   5.3 Metal overlap of contact \(\lambda\)
   5.4 \(n^+\) emitter diffusion overlap of contact \(2\lambda\)
   5.5 p-base diffusion overlap of contact \(2\lambda\)
   5.6 p-base to \(n^+\) emitter \(3\lambda\)
   5.7 Spacing to isolation diffusion \(4\lambda\)

6. Metalization (Blue, Mask #6)
   6.1 Width \(2\lambda\)
   6.2 Spacing \(2\lambda\)
   6.3 Bonding pad size \(100 \mu \times 100 \mu\)
   6.4 Probe pad size \(75 \mu \times 75 \mu\)
   6.5 Bonding pad separation \(50 \mu\)
   6.6 Bonding to probe pad \(30 \mu\)
   6.7 Probe pad separation \(30 \mu\)
   6.8 Pad to circuitry \(40 \mu\)
   6.9 Maximum current density \(0.8 \text{ mA/\mu width}\)

7. Passivation (Purple, Mask #7)
   7.1 Minimum bonding pad opening \(90 \mu \times 90 \mu\)
   7.2 Minimum probe pad opening \(65 \mu \times 65 \mu\)
Add contact to n-epi region from design rules 2.3 and 3.3
<p>| | | |</p>
<table>
<thead>
<tr>
<th></th>
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</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>n⁺ buried collector diffusion (Yellow, Mask #1)</td>
<td></td>
</tr>
<tr>
<td>1.1</td>
<td>Width</td>
<td>3λ</td>
</tr>
<tr>
<td>1.2</td>
<td>Overlap of p-base diffusion (for vertical npn)</td>
<td>2λ</td>
</tr>
<tr>
<td>1.3</td>
<td>Overlap of n⁺ emitter diffusion (for collector contact of vertical npn)</td>
<td>2λ</td>
</tr>
<tr>
<td>1.4</td>
<td>Overlap of p-base diffusion (for collector and emitter of lateral pnp)</td>
<td>2λ</td>
</tr>
<tr>
<td>1.5</td>
<td>Overlap of n⁺ emitter diffusion (for base contact of lateral pnp)</td>
<td>2λ</td>
</tr>
<tr>
<td>2.</td>
<td>Isolation diffusion (Orange, Mask #2)</td>
<td></td>
</tr>
<tr>
<td>2.1</td>
<td>Width</td>
<td>4λ</td>
</tr>
<tr>
<td>2.2</td>
<td>Spacing</td>
<td>24λ</td>
</tr>
<tr>
<td>2.3</td>
<td>Distance to n⁺ buried collector</td>
<td>14λ</td>
</tr>
<tr>
<td>3.</td>
<td>p-base diffusion (Brown, Mask #3)</td>
<td></td>
</tr>
<tr>
<td>3.1</td>
<td>Width</td>
<td>3λ</td>
</tr>
<tr>
<td>3.2</td>
<td>Spacing</td>
<td>5λ</td>
</tr>
<tr>
<td>3.3</td>
<td>Distance to isolation diffusion</td>
<td>14λ</td>
</tr>
<tr>
<td>3.4</td>
<td>Width (resistor)</td>
<td>3λ</td>
</tr>
<tr>
<td>3.5</td>
<td>Spacing (as resistor)</td>
<td>3λ</td>
</tr>
<tr>
<td>4.</td>
<td>n⁺ emitter diffusion (Green, Mask #4)</td>
<td></td>
</tr>
<tr>
<td>4.1</td>
<td>Width</td>
<td>3λ</td>
</tr>
<tr>
<td>4.2</td>
<td>Spacing</td>
<td>3λ</td>
</tr>
<tr>
<td>4.3</td>
<td>p-base diffusion overlap of n⁺ emitter diffusion (emitter in base)</td>
<td>2λ</td>
</tr>
<tr>
<td>4.4</td>
<td>Spacing to isolation diffusion (for collector contact)</td>
<td>12λ</td>
</tr>
<tr>
<td>4.5</td>
<td>Spacing to p-base diffusion (for base contact of lateral pnp)</td>
<td>6λ</td>
</tr>
<tr>
<td>4.6</td>
<td>Spacing to p-base diffusion (for collector contact of vertical npn)</td>
<td>6λ</td>
</tr>
</tbody>
</table>
5. Contact (Black, Mask #5)
   5.1 Size (exactly) \[4\lambda \times 4\lambda\]
   5.2 Spacing \[2\lambda\]
   5.3 Metal overlap of contact \[\lambda\]
   5.4 \(n^+\) emitter diffusion overlap of contact \[2\lambda\]
   5.5 p-base diffusion overlap of contact \[2\lambda\]
   5.6 p-base to \(n^+\) emitter \[3\lambda\]
   5.7 Spacing to isolation diffusion \[4\lambda\]

6. Metalization (Blue, Mask #6)
   6.1 Width \[2\lambda\]
   6.2 Spacing \[2\lambda\]
   6.3 Bonding pad size \[100 \mu \times 100 \mu\]
   6.4 Probe pad size \[75 \mu \times 75 \mu\]
   6.5 Bonding pad separation \[50 \mu\]
   6.6 Bonding to probe pad \[30 \mu\]
   6.7 Probe pad separation \[30 \mu\]
   6.8 Pad to circuitry \[40 \mu\]
   6.9 Maximum current density \[0.8 \text{mA}/\mu\text{width}\]

7. Passivation (Purple, Mask #7)
   7.1 Minimum bonding pad opening \[90 \mu \times 90 \mu\]
   7.2 Minimum probe pad opening \[65 \mu \times 65 \mu\]
But, there are some rather strict rules relating to the epi contact from (left to right) rules 4.4, 5.4, 4.6

Note: 26\(\lambda\) required between p-base and isolation diffusion

NOT TO SCALE
Consider a structure with a collector contact on both sides of epi.

Note: Not to vertical Scale

Note: 26\(\lambda\) required Between p-base and isolation diffusion
Note: Not to vertical Scale

Note: 26\(\lambda\) required Between p-base and isolation diffusion
Note: Not to vertical Scale
Major contributor to large size of BJT is the isolation diffusion which diffuses laterally a large distance beyond the drawn edges of the isolation mask.

Note: Not to vertical Scale

Bounding Area = $3600\lambda^2$
Comparison with Area for n-channel MOSFET in Bulk CMOS

Bounding Area = $208\lambda^2$
Minimum-Sized MOSFET

Bounding Area = $168\lambda^2$
Active Area = $6\lambda^2$
Note: Not to vertical Scale
Area Comparison between BJT and MOSFET

- BJT Area = $3600 \lambda^2$
- n-channel MOSFET Area = $168 \lambda^2$
- Area Ratio = 21:1
Operating Point Analysis of MOS and Bipolar Devices

Determine $V_{\text{OUTQ}}$ and $V_{\text{CQ}}$
Operating Point Analysis of MOS and Bipolar Devices

Examples: Several Sample Circuits were Analyzed

Determine $V_{OUTQ}$ and $V_{CQ}$
End of Lecture 20