EE 330
Lecture 29

Bipolar Processes

• Device Sizes
• Parasitic Devices
  – JFET
  – Thyristors

Thyristors

• SCR – Basic operation
Topical Coverage Change

Will have several additional lectures on amplifier structures but will temporarily suspend discussion of amplifiers to consider Thyristors

This is being done so that the Thyristor laboratory experiments can be conducted this week
Outline

Bipolar Processes
- Comparison of MOS and Bipolar Process
- Parasitic Devices in CMOS Processes
- JFET

Special Bipolar Processes
- Thyristors
  - SCR
  - TRIAC
Review from a Previous Lecture

A-A’ Section

vertical npn

lateral pnp

B-B’ Section
Review from a Previous Lecture
Review from a Previous Lecture

vertical npn

lateral pnp
Review from a Previous Lecture

- Diode (capacitor)
- Resistor
- p-channel JFET
Will consider next the JFET but first some additional information about MOS Devices

Enhancement and Depletion MOS Devices

• Enhancement Mode n-channel devices
  \( V_T > 0 \)
• Enhancement Mode p-channel devices
  \( V_T < 0 \)
• Depletion Mode n-channel devices
  \( V_T < 0 \)
• Depletion Mode p-channel devices
  \( V_T > 0 \)
Enhancement and Depletion MOS Devices

- Depletion mode devices require only one additional mask step.
- Older n-mos and p-mos processes usually had a depletion device and an enhancement device.
- Depletion devices usually not available in CMOS because applications usually do not justify the small increasing costs in processing.
The JFET

With $V_{GS}=0$, channel exists under gate between D and S

Under sufficiently large reverse bias (depletion region widens and channel disappears - “pinches off”)
Under smaller reverse bias (depletion region widens and channel thins)
The JFET

Under small reverse bias and large negative $V_{DS}$ (channel pinches off)
The JFET

n-channel

p-channel

Square-law model of p-channel JFET

\[
I_D = \begin{cases} 
0 & V_{GS} > V_P \\
\frac{2I_{DSSp}}{V_P^2} \left(V_{GS} - V_P - \frac{V_{DS}}{2}\right) V_{DS} & -0.3 < V_{GS} < V_P \\
I_{DSSp} \left(1 - \frac{V_{GS}}{V_P}\right)^2 & V_{GS} + 0.3 > V_{DS} > V_{GS} - V_P \\
I_{DSSp} & -0.3 < V_{GS} < V_P, \quad V_{DS} < V_{GS} - V_P 
\end{cases}
\]

(I_{DSSp} carries negative sign)

- Functionally identical to the square-law model of MOSFET
- Parameters $I_{DSS}$ and $V_P$ characterize the device
- $I_{DSS}$ proportional to $W/L$ where $W$ and $L$ are width and length of n+ diff
- $V_P$ is negative for n-channel device, positive for p-channel device thus JFET is depletion mode device
- Must not forward bias GS junction by over about 300mV or excessive base current will flow (red constraint)
- Widely used as input stage for bipolar op amps
The JFET

Square-law model of n-channel JFET

\[
I_D = \begin{cases} 
0 & V_{GS} < V_P \\
\frac{2I_{DSS}}{V_P^2} \left( V_{GS} - V_P - \frac{V_{DS}}{2} \right) V_{DS} & 0.3 > V_{GS} > V_P \\
I_{DSS} \left( 1 - \frac{V_{GS}}{V_P} \right)^2 & 0.3 > V_{GS} > V_P \text{ and } V_{DS} > V_{GS} - V_P 
\end{cases}
\]

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- Must not forward bias GS junction by over about 300mV or excessive base current will flow (red constraint)
- Widely used as input stage for bipolar op amps
The Schottky Diode

- Metal-Semiconductor Junction
- One contact is ohmic, other is rectifying
- Not available in all processes
- Relatively inexpensive adder in some processes
- Lower cut-in voltage than pn junction diode
- High speed
The MESFET

- Metal-Semiconductor Junction for Gate
- Drain and Source contacts ohmic, other is rectifying
- Usually not available in standard CMOS processes
- Must not forward bias very much
- Lower cut-in voltage than pn junction diode
- High speed
The Thyristor

A bipolar device in CMOS Processes

Consider a Bulk-CMOS Process

Have formed a lateral pnpn device!

Will spend some time studying pnnpn devices
How does the area required to realize a MOSFET compare to that required to realize a BJT?

Will consider a minimum-sized device in both processes
<table>
<thead>
<tr>
<th></th>
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<tbody>
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</table>
5. Contact (Black, Mask #5)
   5.1 Size (exactly) 4\(\lambda\) \times 4\(\lambda\)
   5.2 Spacing 2\(\lambda\)
   5.3 Metal overlap of contact \(\lambda\)
   5.4 \(n^+\) emitter diffusion overlap of contact 2\(\lambda\)
   5.5 p-base diffusion overlap of contact 2\(\lambda\)
   5.6 p-base to \(n^+\) emitter 3\(\lambda\)
   5.7 Spacing to isolation diffusion 4\(\lambda\)

6. Metalization (Blue, Mask #6)
   6.1 Width 2\(\lambda\)
   6.2 Spacing 2\(\lambda\)
   6.3 Bonding pad size 100 \(\mu\) \times 100 \(\mu\)
   6.4 Probe pad size 75 \(\mu\) \times 75 \(\mu\)
   6.5 Bonding pad separation 50 \(\mu\)
   6.6 Bonding to probe pad 30 \(\mu\)
   6.7 Probe pad separation 30 \(\mu\)
   6.8 Pad to circuitry 40 \(\mu\)
   6.9 Maximum current density 0.8 mA/\(\mu\) width

7. Passivation (Purple, Mask #7)
   7.1 Minimum bonding pad opening 90 \(\mu\) \times 90 \(\mu\)
   7.2 Minimum probe pad opening 65 \(\mu\) \times 65 \(\mu\)
Consider Initially the Emitter in the BJT surrounded by a base region
TABLE 2C.2
Design rules for a typical bipolar process ($\lambda = 2.5 \, \mu$)
(See Table 2C.3 in color plates for graphical interpretation)

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   5.3 Metal overlap of contact 
   5.4 n⁺ emitter diffusion overlap of contact 
   5.5 p-base diffusion overlap of contact 
   5.6 p-base to n⁺ emitter 
   5.7 Spacing to isolation diffusion 
   \[4\lambda \times 4\lambda\]
   \[2\lambda\]
   \[\lambda\]
   \[2\lambda\]
   \[2\lambda\]
   \[3\lambda\]
   \[4\lambda\]

6. Metalization (Blue, Mask #6)
   6.1 Width 
   6.2 Spacing 
   6.3 Bonding pad size 
   6.4 Probe pad size 
   6.5 Bonding pad separation 
   6.6 Bonding to probe pad 
   6.7 Probe pad separation 
   6.8 Pad to circuitry 
   6.9 Maximum current density 
   \[2\lambda\]
   \[2\lambda\]
   \[100 \mu \times 100 \mu\]
   \[75 \mu \times 75 \mu\]
   \[50 \mu\]
   \[30 \mu\]
   \[30 \mu\]
   \[40 \mu\]
   \[0.8 \text{mA/\mu width}\]

7. Passivation (Purple, Mask #7)
   7.1 Minimum bonding pad opening 
   7.2 Minimum probe pad opening 
   \[90 \mu \times 90 \mu\]
   \[65 \mu \times 65 \mu\]
From design rules (left to right) 4.3, 5.1, 5.4, 5.6, 5.5
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Design rules for a typical bipolar process ($\lambda = 2.5 \ \mu$)
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Add n+ buried for collector

From design rule 1.2

\[ \text{23}\lambda \]

\[ \text{2}\lambda \]
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Add n-epi region from design rules 2.3 and 3.3
5. Contact (Black, Mask #5)
   5.1 Size (exactly) \hspace{1cm} 4\lambda \times 4\lambda
   5.2 Spacing \hspace{1cm} 2\lambda
   5.3 Metal overlap of contact \hspace{1cm} \lambda
   5.4 n^+ emitter diffusion overlap of contact \hspace{1cm} 2\lambda
   5.5 p-base diffusion overlap of contact \hspace{1cm} 2\lambda
   5.6 p-base to n^+ emitter \hspace{1cm} 3\lambda
   5.7 Spacing to isolation diffusion \hspace{1cm} 4\lambda

6. Metalization (Blue, Mask #6)
   6.1 Width \hspace{1cm} 2\lambda
   6.2 Spacing \hspace{1cm} 2\lambda
   6.3 Bonding pad size \hspace{1cm} 100 \mu \times 100 \mu
   6.4 Probe pad size \hspace{1cm} 75 \mu \times 75 \mu
   6.5 Bonding pad separation \hspace{1cm} 50 \mu
   6.6 Bonding to probe pad \hspace{1cm} 30 \mu
   6.7 Probe pad separation \hspace{1cm} 30 \mu
   6.8 Pad to circuitry \hspace{1cm} 40 \mu
   6.9 Maximum current density \hspace{1cm} 0.8 \text{mA/\mu width}

7. Passivation (Purple, Mask #7)
   7.1 Minimum bonding pad opening \hspace{1cm} 90 \mu \times 90 \mu
   7.2 Minimum probe pad opening \hspace{1cm} 65 \mu \times 65 \mu
Add contact to n-epi region from design rules 2.3 and 3.3
### TABLE 2C.2
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</tr>
<tr>
<td>4.6 Spacing to p-base diffusion (for collector contact of vertical npn)</td>
<td>$6\lambda$</td>
</tr>
</tbody>
</table>
5. Contact (Black, Mask #5)
   5.1 Size (exactly) \[4\lambda \times 4\lambda\]
   5.2 Spacing \[2\lambda\]
   5.3 Metal overlap of contact \[\lambda\]
   5.4 n\(^+\) emitter diffusion overlap of contact \[2\lambda\]
   5.5 p-base diffusion overlap of contact \[2\lambda\]
   5.6 p-base to n\(^+\) emitter \[3\lambda\]
   5.7 Spacing to isolation diffusion \[4\lambda\]

6. Metalization (Blue, Mask #6)
   6.1 Width \[2\lambda\]
   6.2 Spacing \[2\lambda\]
   6.3 Bonding pad size \[100 \mu \times 100 \mu\]
   6.4 Probe pad size \[75 \mu \times 75 \mu\]
   6.5 Bonding pad separation \[50 \mu\]
   6.6 Bonding to probe pad \[30 \mu\]
   6.7 Probe pad separation \[30 \mu\]
   6.8 Pad to circuitry \[40 \mu\]
   6.9 Maximum current density \[0.8 \text{mA}/\mu \text{width}\]

7. Passivation (Purple, Mask #7)
   7.1 Minimum bonding pad opening \[90 \mu \times 90 \mu\]
   7.2 Minimum probe pad opening \[65 \mu \times 65 \mu\]
But, there are some rather strict rules relating to the epi contact from (left to right) rules 4.4, 5.4, 4.6.

Note: 26\(\lambda\) required between p-base and isolation diffusion.
Consider a structure with a collector contact on both sides of epi.

Note: 26\(\lambda\) required between p-base and isolation diffusion.

Note: Not to vertical Scale.
Note: Not to vertical Scale

Note: 26λ required Between p-base and isolation diffusion
Note: Not to vertical Scale
Major contributor to large size of BJT is the isolation diffusion which diffuses laterally a large distance beyond the drawn edges of the isolation mask.
Comparison with Area for n-channel MOSFET in Bulk CMOS

Bounding Area = 208\lambda^2
Minimum-Sized MOSFET

Bounding Area = 168$\lambda^2$
Active Area = 6$\lambda^2$
Area Comparison between BJT and MOSFET

- BJT Area = $3600 \lambda^2$
- n-channel MOSFET Area = $168 \lambda^2$
- Area Ratio = 21:1
Outline

Two-Port Amplifier Models

Bipolar Processes

• Comparison of MOS and Bipolar Process
• Parasitic Devices in CMOS Processes
• JFET

Special Bipolar Processes

• Thyristors
  SCR
  TRIAC
Thyristors

The good and the bad!
Thyristors

The good

SCRs
Triacs

The bad

Parasitic Device that can destroy integrated circuits
The SCR

Silicon Controlled Rectifier

- Widely used to switch large resistive or inductive loads
- Widely used in the power electronics field
- Widely used in consumer electronic to interface between logic and power

Usually made by diffusions in silicon

Consider first how this 4-layer 3-junction device operates
Operation of the SCR

Not actually separated but useful for describing operation
Variation of Current Gain ($\beta$) with Bias for BJT

Note that current gain gets very small at low base current levels.
Operation of the SCR

Consider a small positive bias (voltage or current) on the gate ($V_{GC}<0.5V$) and a positive and large voltage $V_F$

Will have $V_{C1} \geq V_F - 0.5V$

Thus $Q_1$ has a large positive voltage on its collector

Since $V_{B_{E1}}$ is small, $I_{C1}$ will be small as will $I_{C2}$ so diode equation governs BE junction of $Q_1$

$I_F$ will be very small
Operation of the SCR

Now let bias on the gate increase ($V_{GC}$ around 0.6V) so $Q_1$ and $Q_2$ in FA

From diode equation, base voltage $V_{BE1}$ will increase and collector current $I_{C1}$ will increase

Thus base current $I_{B2}$ will increase as will the collector current of $I_{C2}$

Under assumption of operation in FA region get expression

$$ I_{B1} = I_G + \beta_1 \beta_2 I_{B1} $$

This is regenerative feedback (actually can show pole in RHP)
Very Approximate Analysis Showing RHP Pole

\[ V_G s C_B + I_{B1} = I_{C2} + I_G \]

\[ I_{C2} = \beta_1 \beta_2 I_{B1} \]

\[ I_{B1} R_{BE} = V_G \]

\[ V_G = I_G \frac{R_{BE}}{s R_{BE} C_B + 1 - \beta_1 \beta_2} \]

\[ p = \frac{\beta_1 \beta_2 - 1}{R_{BE} C_B} \]
Operation of the SCR

\[ V_{C1} \approx V_F - 0.6V \]

Under assumption of operation in FA region get expression

\[ I_{B1} = I_G + \beta_1 \beta_2 I_{B1} \]

What will happen with this is regenerative feedback?

If \( I_G \) is small (and thus \( \beta_1 \) and \( \beta_2 \) are small) \( I_F \) will be very small.

If \( I_G \) larger but less than \( \beta_1 \beta_2 I_{B1} \) it can be removed and current will continue to flow.

\( I_{C1} \) will continue to increase and drive \( Q_1 \) into SAT.

This will try to drive \( V_A \) towards 0.9V (but forced to be \( V_F \)!

The current in \( V_F \) will go towards \( \infty \).

The SCR will self-destruct because of excessive heating!

Too bad the circuit self-destructed because the small gate current was able to control a lot of current!
Operation of the SCR

Consider a modified application by adding a load (depicted as $R_L$)

All operation is as before, but now, after the triggering occurs, the voltage $V_F$ will drop to approximately 0.8 V and the voltage $V_{CC} - 0.8$ will appear across $R_L$.

If $V_{CC}$ is very large, the SCR has effectively served as a switch putting $V_{CC}$ across the load and after triggering occurs, $I_G$ can be removed!

But, how can we turn it off? Will discuss that later.
Operation of the SCR

SCR model

\[
\begin{aligned}
I_F &= f_1(V_F, V_G) \\
I_G &= f_2(V_G)
\end{aligned}
\]

As for MOSFET, Diode, and BJT, several models for SCR can be developed

The Ideal SCR Model

\[
\begin{aligned}
I_F &= f_{iI}(V_F, I_G) \\
I_G &= f_{2I}(V_G)
\end{aligned}
\] or \[
\begin{aligned}
I_F &= f_{iIA}(V_F, V_G) \\
I_G &= f_{2I}(V_G)
\end{aligned}
\]
Operation of the SCR

Consider the Ideal SCR Model

\[
\begin{align*}
I_F &= f_{1I}(V_F, I_G) \\
I_G &= f_{2I}(V_G)
\end{align*}
\]

$I_H$ is very small

$I_{G1}$ is small (but not too small)
Operation of the SCR

Operation with the Ideal SCR

Load Line:

\[ V_{CC} = I_F R_L + V_F \]

Analysis:

\[ V_{CC} = I_F R_L + V_F \]
\[ I_F = f_{II}(V_F, I_G) \]

The solution of these two equations is at the intersection of the load line and the device characteristics.

Note three intersection points:
- Two (upper and lower) are stable equilibrium points, one is not.

When operating at upper point, \( V_F = 0 \) so \( V_{CC} \) appears across \( R_L \) We say SCR is ON.

When operating at lower point, \( I_F \approx 0 \) so no signal across \( R_L \) We say SCR is OFF.

When \( I_G = 0 \), will stay in whatever state it was in.
Operation of the SCR

Operation with the Ideal SCR

\[ I_F = f_{1i} (V_F, I_G) \]

For notational convenience will drop subscript unless emphasis is needed

\[ I_F = f (V_F, I_G) \]
Operation of the SCR

Operation with the Ideal SCR

Now assume it was initially in the OFF state and then a gate current was applied.

\[
V_{CC} = I_F R_L + V_F
\]

\[
I_F = f \left( V_F, I_G \right)
\]

Now there is a single intersection point so a unique solution.

The SCR is now ON.

Removing the gate current will return to the previous solution (which has 3 intersection points) but it will remain in the ON state.
Operation of the SCR

Operation with the Ideal SCR

Turning SCR off when \( I_G = 0 \)

Reduce \( V_{CC} \) so that \( V_{CC}/R_L \) goes below \( I_H \)

This will provide a single intersection point

\( V_{CC} \) can then be increased again and SCR will stay off

Must not increase \( V_{CC} \) much above \( V_{BGF0} \) else will turn on
Operation of the SCR

Operation with the Ideal SCR

Turning SCR off when $I_G=0$
Operation of the SCR

Operation with the Ideal SCR

Often $V_{CC}$ is an AC signal (often 110V)

SCR will turn off whenever AC signal goes negative

\[ IF = 0 \]

\[ V_{CC} \]

\[ V_{R} \]

\[ I_H \]

\[ V_{BGF0} \]

\[ I_{F} \]

Load Line

\[ \frac{V_{CC}}{R_L} \]
Operation of the SCR

Operation with the Ideal SCR

Often $V_{CC}$ is an AC signal (often 110V)

SCR will turn off whenever AC signal goes negative
Operation of the SCR

Operation with the Ideal SCR

Turning SCR off when $I_G > 0$

Reduce $V_{CC}$ so that $V_{CC}/R_L$ goes below $I_H$

This will provide a single intersection point

But when $V_{CC}$ is then increased SCR will again turn on

Will not turn off if $I_G$ is very large
End of Lecture 29