Basic Concepts
Historical Background, Feature Sizes and Yield
Quiz 2

How many minimum-sized MOS transistors can be placed on a square die that is 1000µ on a side in a 65nm process? (Neglect any bonding pads needed to get the signals to the outside world. Assume factor of 10 overhead for spacing between transistors).
And the number is ....
And the number is ....
Quiz 2 How many minimum-sized MOS transistors can be placed on a square die that is 1000µ on a side in a 65nm process? (Neglect any bonding pads needed to get the signals to the outside world. Assume factor of 10 overhead for spacing between transistors.)

Solution:

\[ n_{\text{Tran}} \approx \frac{1}{10} \frac{A_{\text{die}}}{A_{\text{tran}}} \]

\[ n_{\text{Tran}} \approx \frac{1}{10} \frac{(1000\mu)^2}{(65\text{nm})^2} = 23.6 \text{ million} \]
Review from Last Time

• Sophisticated Integrated CAD Toolsets are extensively used in the industry to design integrated circuits
  – Minimize the chances of an error
  – Real asset to (and not a competitor of) the engineer
  – Critical to pay attention to what tools tell you
• Feature size good metric for characterizing capabilities of a process
  – State of the art at about 65nm
  – Pitch sometimes used instead of feature size
  – Drawn and actual features may differ
  – Bragging rights focus on actual rather than drawn features
• Yield often determined by statistically independent events

\[ Y = P^n \]

• Cost of Wafers in $800 to $3000 range depending on size and process

\[ C_{\text{per\ unit\ area}} \approx 2.5 \, \text{/cm}^2 \]
What is meant by “reliably”

Yield is acceptable if a very large number of these features are made

If $P$ is the probability that a feature is good

$n$ is the number of features on an IC

$Y$ is the yield

\[ Y = P^n \]

\[ P = e^{\frac{\log_e Y}{n}} \]
Example: How reliable must a feature be?

\[ n = 5 \times 10^3 \]
\[ Y = 0.9 \]

\[ P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5 \times 10^3}} = 0.999979 \]

But is \( n = 5000 \) large enough?

More realistically \( n = 5 \times 10^9 \)

\[ P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5 \times 10^9}} = 0.999999999979 \]

Extremely high reliability must be achieved in all processing steps to obtain acceptable yields in state of the art processes.
Feature Size

• Typically minimum length of a transistor
• Often minimum width or spacing of a metal interconnect (wire)
• Point of “bragging” by foundries
  – Drawn length and actual length differ
• Often specified in terms of pitch
  – Pitch approximately equal to twice minimum feature size
Feature Size Evolution

<table>
<thead>
<tr>
<th>Year</th>
<th>Size</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mid 70’s</td>
<td>25µ</td>
</tr>
<tr>
<td>2005</td>
<td>90nm</td>
</tr>
<tr>
<td>2010</td>
<td>20nm</td>
</tr>
<tr>
<td>2020</td>
<td>10nm</td>
</tr>
</tbody>
</table>

\[ 1\mu = 10^3 \text{ nm} = 10^{-6} \text{ m} = 10^4 \text{ Å} \]
MOS Transistor

Active

Poly
MOS Transistor

Drawn Length and Width Shown
MOS Transistor

Actual Drain and Source at Edges of Channel
MOS Transistor

Effective Width and Length Generally Smaller than Drawn Width and Length
Technology Nomenclature

- SSI  Small Scale Integration  1-100
- MSI  Medium Scale Integration  100-10^3
- LSI  Large Scale Integration  10^3-10^5
- VLSI  Very Large Scale Integration  10^5-10^6

Any design in a process capable of incorporating a large number of devices is generally termed a VLSI design.
Device and Die Costs

Consider the high-volume incremental costs of manufacturing integrated circuits

Example: Assume an 8” wafer in a 0.25µ process costs $800

Determine the number of minimum-sized transistors that can be fabricated on this wafer and the cost per transistor. Neglect spacing and interconnect.

Solution:

\[ n_{trans} \leq \frac{A_{wafer}}{A_{trans}} = \frac{\pi(4\text{in})^2}{(0.25\mu)^2} = 5.2E11 \]

\[ C_{trans} = \frac{C_{wafer}}{n_{trans}} = \frac{$800}{5.2E11} = $15.4E-9 \]

Note: the device count may be decreased by a factor of 10 or more if interconnect and spacing is included but even with this decrease, the cost per transistor is still very low!
Device and Die Costs

\[ C_{\text{per unit area}} \approx \$2.5 / cm^2 \]

Example: If the die area of the 741 op amp is 1.8 \(mm^2\), determine the cost of the silicon needed to fabricate this op amp

\[ C_{741} = \$2.5 / cm^2 \cdot (1.8 \text{mm}^2) \approx \$0.05 \]

Actual integrated op amp will be dramatically less if bonding pads are not needed
# Size of Atoms and Molecules in Semiconductor Processes

<table>
<thead>
<tr>
<th>Material</th>
<th>Average Atom Spacing</th>
<th>Lattice Constant</th>
<th>Breakdown Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon:</td>
<td>2.7 Å</td>
<td>5.4 Å</td>
<td>5 to 10 MV/cm = 5 to 10 mV/Å</td>
</tr>
<tr>
<td>$\text{SiO}_2$</td>
<td>3.5 Å</td>
<td></td>
<td>20 KV/cm</td>
</tr>
<tr>
<td>Air</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Physical size of atoms and molecules place fundamental limit on conventional scaling approaches.
Defects in a Wafer

- Dust particles and other undesirable processes cause defects
- Defects in manufacturing cause yield loss
Yield Issues and Models

- Defects in processing cause yield loss
- The probability of a defect causing a circuit failure increases with die area
- The circuit failures associated with these defects are termed **Hard Faults**
- This is the major factor limiting the size of die in integrated circuits
- Wafer scale integration has been a “gleam in the eye” of designers for 3 decades but the defect problem continues to limit the viability of such approaches
- Several different models have been proposed to model the hard faults
Yield Issues and Models

• Parametric variations in a process can also cause circuit failure or cause circuits to not meet desired performance specifications (this is of particular concern in analog and mixed-signal circuits)

• The circuits failures associated with these parametric variations are termed **Soft Faults**

• Increases in area, judicious layout and routing, and clever circuit design techniques can reduce the effects of soft faults
Hard Fault Model

\[ Y_H = e^{-Ad} \]

\( Y_H \) is the probability that the die does not have a hard fault
\( A \) is the die area
\( d \) is the defect density (typically 1cm\(^2\) < \( d \) < 2cm\(^2\))

Industry often closely guards the value of \( d \) for their process

Other models, which may be better, have the same general functional form
Soft Fault Model

Soft fault models often dependent upon design and application

Often the standard deviation of a parameter is dependent upon the reciprocal of the square root of the parameter sensitive area

\[ \sigma = \frac{\rho}{\sqrt{A_k}} \]

\( \rho \) is a constant dependent upon the architecture and the process

\( A_k \) is the area of the parameter sensitive area
Soft Fault Model

\[ P_{SOFT} = \int_{X_{MIN}}^{X_{MAX}} f(x) \, dx \]

\( P_{SOFT} \) is the soft fault yield  
\( f(x) \) is the probability density function of the parameter of interest  
\( X_{MIN} \) and \( X_{MAX} \) define the acceptable range of the parameter of interest

Some circuits may have several parameters that must meet performance requirements
Soft Fault Model

If there are \( k \) parameters that must meet parametric performance requirements and if the random variables characterizing these parameters are uncorrelated, then the soft yield is given by

\[
Y_S = \prod_{j=1}^{k} P_{SOFT_j}
\]
If both hard and soft faults affect the yield of a circuit, the overall yield is given by the expression

\[ Y = Y_H Y_S \]
The manufacturing costs per good die is given by

\[ C_{\text{Good}} = \frac{C_{\text{FabDie}}}{Y} \]

where \( C_{\text{FabDie}} \) is the manufacturing costs of a fab die and \( Y \) is the yield.

There are other costs that must ultimately be included such as testing costs, engineering costs, etc.
Example: Assume a die has no soft fault vulnerability, a die area of $1\text{cm}^2$ and a process has a defect density of $1.5\text{cm}^{-2}$

a) Determine the hard yield

b) Determine the manufacturing cost per good die if 8” wafers are used and if the cost of the wafers is $1200
Solution

a) \[ Y_H = e^{-Ad} \]
\[ Y = e^{-1 \text{cm}^2 \cdot 1.5 \text{cm}^2} = 0.22 \]

b) \[ C_{\text{Good}} = \frac{C_{\text{FabDie}}}{Y} \]

\[ C_{\text{FabDie}} = \frac{C_{\text{Wafer}}}{A_{\text{Wafer}}} A_{\text{Die}} \]

\[ C_{\text{FabDie}} = \frac{$1200}{\pi (4 \text{in})^2} \text{1cm}^2 = $3.82 \]

\[ C_{\text{Good}} = \frac{$3.82}{0.22} = $17.37 \]
Statistics are Real!

Statistics govern what really happens throughout much of the engineering field!

Statistics are your Friend !!!!

You might as well know what will happen since statistics characterize what WILL happen in many processes!
Statistics can be abused!

Many that are not knowledgeable incorrectly use statistics

Many use statistics to intentionally mislead the public

Some openly abuse statistics for financial gain or for manipulation purposes

Keep an open mind to separate “good” statistics from “abused” statistics
End of Lecture 3