EE 330
Lecture 3

Basic Concepts
Feature Sizes, Manufacturing Costs, and Yield
Review from Last Time

Analog Flow

VLSI Design Flow Summary

- System Description
- Circuit Design (Schematic)
- SPICE Simulation
- Layout/DRC...
- Parasitic Extraction
- Back annotated Schematic
- Post-Layout Simulation
- Fabrication
- LVS
- DRC Error Report
- LVS Error Report
- Simulation Results
Feature Size

Feature size is the minimum lateral feature size that can be **reliably** manufactured.

Often given as either feature size or pitch.

Minimum feature size often identical for different features.
What is meant by “reliably”

Yield is acceptable if circuit performs as designed even when a very large number of these features are made.

If $P$ is the probability that a feature is good

If $n$ is the number of uncorrelated features on an IC

$Y$ is the yield

$$Y = P^n$$

$$P = e^{\frac{\log_e Y}{n}}$$
Example: How reliable must a feature be?

\[ n = 5 \times 10^3 \]
\[ Y = 0.9 \]

\[ P = e^{\log_e Y} \sqrt[5 \times 10^3]{\log_e 0.9} \]

\[ P = e^{5 \times 10^3} \log e 0.9 \]

\[ P = 0.9999979 \]

But is \( n = 5000 \) large enough?

More realistically \( n = 5 \times 10^9 \)

\[ P = e^{\log_e Y} \sqrt[5 \times 10^9]{\log_e 0.9} \]

\[ P = e^{5 \times 10^9} \log e 0.9 \]

\[ P = 0.999999999979 \]

Extremely high reliability must be achieved in all processing steps to obtain acceptable yields in state of the art processes.
Feature Size

- Typically minimum length of a transistor
- Often minimum width or spacing of a metal interconnect (wire)
- Point of “bragging” by foundries
  - Drawn length and actual length differ
- Often specified in terms of pitch
  - Pitch is sum of feature size and spacing to same feature
  - Pitch approximately equal to twice minimum feature size
## Feature Size Evolution

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<th>Size</th>
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\[1\mu = 10^3 \text{ nm} = 10^{-6} \text{ m} = 10^4 \text{ Å}\]
MOS Transistor

Poly

Active
MOS Transistor

Source

Gate

Drain

Region of Interest (Channel)

Drawn Length and Width Shown
MOS Transistor

Actual Drain and Source at Edges of Channel
MOS Transistor

Effective Width and Length Generally Smaller than Drawn Width and Length
Device and Die Costs

Characterize the high-volume incremental costs of manufacturing integrated circuits.

Example: Assume manufacturing cost of an 8” wafer in a 0.25µ process is $800.

Determine the number of minimum-sized transistors that can be fabricated on this wafer and the cost per transistor. Neglect spacing and interconnect.

Solution:

\[ n_{\text{trans}} \approx \frac{A_{\text{wafer}}}{A_{\text{trans}}} = \frac{\pi (4in)^2}{(0.25\mu)^2} = 5.2E11 \]

(520 Billion!)

(Trillion, Tera \ldots 10^{12})

\[ C_{\text{trans}} = \frac{C_{\text{wafer}}}{n_{\text{trans}}} = \frac{$800}{5.2E11} = $15.4E-9 \]

Note: the device count may be decreased by a factor of 10 or more if Interconnect and spacing is included but even with this decrease, the cost per transistor is still very low!
Device and Die Costs

\[ C_{\text{per unit area}} \approx \$2.5/cm^2 \]

Example: If the die area of the 741 op amp is 1.8mm\(^2\), determine the cost of the silicon needed to fabricate this op amp

\[ C_{741} = \$2.5/cm^2 \cdot (1.8\,mm^2) \approx \$0.05 \]

Actual integrated op amp will be dramatically less if bonding pads are not needed
# Size of Atoms and Molecules in Semiconductor Processes

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<th>Material</th>
<th>Average Atom Spacing</th>
<th>Lattice Constant</th>
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<td>Silicon:</td>
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<td>S(_2)O(_2):</td>
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Physical size of atoms and molecules place fundamental limit on conventional scaling approaches.
Defects in a Wafer

- Dust particles and other undesirable processes cause defects
- Defects in manufacturing cause yield loss
Yield Issues and Models

- Defects in processing cause yield loss
- The probability of a defect causing a circuit failure increases with die area
- The circuit failures associated with these defects are termed **Hard Faults**
- This is the major factor limiting the size of die in integrated circuits
- Wafer scale integration has been a “gleam in the eye” of designers for 3 decades but the defect problem continues to limit the viability of such approaches
- Several different models have been proposed to model the hard faults
Yield Issues and Models

- Parametric variations in a process can also cause circuit failure or cause circuits to not meet desired performance specifications (this is of particular concern in analog and mixed-signal circuits)
- The circuits failures associated with these parametric variations are termed **Soft Faults**
- Increases in area, judicious layout and routing, and clever circuit design techniques can reduce the effects of soft faults
Hard Fault Model

\[ Y_H = e^{-Ad} \]

\( Y_H \) is the probability that the die does not have a hard fault
A is the die area
\( d \) is the defect density (typically \( 1 \text{cm}^{-2} < d < 2 \text{cm}^{-2} \))

Industry often closely guards the value of \( d \) for their process

Other models, which may be better, have the same general functional form
Soft Fault Model

Soft fault models often dependent upon design and application

Often the standard deviation of a parameter is dependent upon the reciprocal of the square root of the parameter sensitive area

\[ \sigma = \frac{\rho}{\sqrt{A_k}} \]

\( \rho \) is a constant dependent upon the architecture and the process

\( A_k \) is the area of the parameter sensitive area
Soft Fault Model

\[ P_{SOFT} = \int_{X_{MIN}}^{X_{MAX}} f(x) \, dx \]

- \( P_{SOFT} \) is the soft fault yield
- \( f(x) \) is the probability density function of the parameter of interest
- \( X_{MIN} \) and \( X_{MAX} \) define the acceptable range of the parameter of interest

Some circuits may have several parameters that must meet performance requirements.
Soft Fault Model

If there are \( k \) parameters that must meet parametric performance requirements and if the random variables characterizing these parameters are uncorrelated, then the soft yield is given by

\[
Y_S = \prod_{j=1}^{k} P_{SOFT_j}
\]
Overall Yield

If both hard and soft faults affect the yield of a circuit, the overall yield is given by the expression

\[ Y = Y_H Y_S \]
Cost Per Good Die

The manufacturing costs per good die is given by

\[ C_{\text{Good}} = \frac{C_{\text{FabDie}}}{Y} \]

where \( C_{\text{FabDie}} \) is the manufacturing costs of a fab die and \( Y \) is the yield.

There are other costs that must ultimately be included such as testing costs, engineering costs, etc.
Example: Assume a die has no soft fault vulnerability, a die area of 1cm$^2$ and a process has a defect density of 1.5cm$^{-2}$

a) Determine the hard yield

b) Determine the manufacturing cost per good die if 8” wafers are used and if the cost of the wafers is $1200
Solution

a) \[ Y_H = e^{-Ad} \]
\[ Y = e^{-1\text{cm}^2 \cdot 1.5\text{cm}^2} = 0.22 \]

b) \[ C_{\text{Good}} = \frac{C_{\text{FabDie}}}{Y} \]
\[ C_{\text{FabDie}} = \frac{C_{\text{Wafer}}}{A_{\text{Wafer}}} A_{\text{Die}} \]
\[ C_{\text{FabDie}} = \frac{$1200}{\pi (4\text{in})^2} \text{cm}^2 = $3.82 \]
\[ C_{\text{Good}} = \frac{$3.82}{0.22} = $17.37 \]
Do you like statistics?
Statistics are Real!

Statistics govern what really happens throughout much of the engineering field!

Statistics are your Friend !!!!

You might as well know what will happen since statistics characterize what WILL happen in many processes!
Assume $x$ is a random variable of interest

$f(x) = \text{Probability Density Function for } x$

$$\int_{-\infty}^{\infty} f(x) \, dx = 1$$

$F(x) = \text{Cumulative Density Function for } x$

$$F(X_1) = \int_{-\infty}^{X_1} f(x) \, dx$$

$$0 \leq F(x) \leq 1 \quad \frac{\partial F(x)}{\partial x} \geq 0$$
Statistics Review

\[ f(x) = \text{Probability Density Function for } x \]

\[ F(x) = \text{Cumulative Density Function for } x \]

\[ P\{x \leq x_1\} = \int_{x=-\infty}^{x_1} f(x) \, dx \]

\[ P\{x \leq X_1\} = F(X_1) \]
Statistics Review

\[ f(x) = \text{Probability Density Function for } x \]

\[ F(x) = \text{Cumulative Density Function for } x \]

\[ \Pr\{X_1 \leq x \leq X_2\} = \int_{X_1}^{X_2} f(x) \, dx \quad \text{or} \quad \Pr\{X_1 \leq x \leq X_2\} = F(X_2) - F(X_1) \]
Statistics Review

Theorem 1: If the random variable $x$ is normally distributed with mean $\mu$ and standard deviation $\sigma$, then $y = \frac{x - \mu}{\sigma}$ is also a random variable that is normally distributed with mean 0 and standard deviation of 1.

(Normal Distribution and Gaussian Distribution are the same)
The random part of many parameters of microelectronic circuits is often assumed to be Normally distributed and experimental observations confirm that this assumption provides close agreement between theoretical and experimental results.

The mapping \( y = \frac{x - \mu}{\sigma} \) is often used to simplify the statistical characterization of the random parameters in microelectronic circuits.
Background Information

Theorem 2: If $x$ is a Normal (Gaussian) random variable with mean $\mu$ and standard deviation $\sigma$, then the probability that $x$ is between $x_1$ and $x_2$ is given by

$$p = \int_{x_1}^{x_2} f(x) \, dx = \int_{x_{1n}}^{x_{2n}} f_{n}(x) \, dx$$

where

$$x_{1n} = \frac{x_1 - \mu}{\sigma} \quad \text{and} \quad x_{2n} = \frac{x_2 - \mu}{\sigma}$$

and where $f_{n}(x)$ is N(0,1) and $f(x)$ is N($\mu$, $\sigma^2$).
Background Information
Observation: The probability that the $N(0,1)$ random variable $x_n$ satisfies the relationship $x_{1n} < x_n < x_{2n}$ is also given by

$$p = F_n(x_{2n}) - F_n(x_{1n})$$

where $F_n(x)$ is the CDF of $x_n$.

Since the $N(0,1)$ distribution is symmetric around 0, $p$ can also be expressed as

$$p = F_n(x_{2n}) - (1 - F_n(-x_{1n}))$$
Observation: In many electronic circuits, the random variables of interest are 0 mean Gaussian and the probabilities of interest are characterized by a region defined by the magnitude of the random variable. In these cases,

\[ p = \int_{-x_{1n}}^{x_{1n}} f_n(x) \, dx = F_n(x_{1n}) - F_n(-x_{1n}) = 2F_n(x_{1n}) - 1 \]
### Tables of the CDF of the N(0,1) random variable are readily available. It is also available in Matlab, Excel, and a host of other sources.

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http://www.math.unb.ca/~knight/utility/NormTble.htm
Background Information

Tables of the CDF of the $N(0,1)$ random variable are readily available. It is also available in Matlab, Excel, and a host of other sources.
**Background Information**

**Example:** Determine the probability that the $N(0,1)$ random variable has magnitude less than 2.6

$$p = 2F_n (2.6) - 1$$

From the table of the CDF, $F_n(2.6) = 0.9953$ so $p = .9906$
Example: Determine the soft yield of an operational amplifier that has an offset voltage requirement of 5mV if the standard deviation of the offset voltage is 2.5mV and the mean is 0V.

\[
y = \frac{x-0}{2.5\text{mV}}
\]

\[
p = \int_{-2}^{2} f_N(x) \, dx = F_N(2) - F_N(-2) = 2F_N(2) - 1
\]

\[
p = 2F_N(2) - 1 = 2 \times .9772 - 1 = .9544
\]
Meeting the Real Six-Sigma Challenge

Introduced by Bill Smith of Motorola in 1984

2/3 of Fortune 500 Companies adopted/adopting 6-sigma concepts
Meeting the Real Six-Sigma Challenge

Six-Sigma or Else !!

YOU'RE FIRED!
Yield at the Six-Sigma level

(Assume a Gaussian distribution)

\[ Y_{6\text{sigma}} = 2F_N(6) - 1 \]

\[ Y_{6\text{sigma}} = 0.9999999980 \]

This is approximately 2 defects out of 1 billion parts
Yield at Various Sigma Levels

<table>
<thead>
<tr>
<th>No</th>
<th>Sigma</th>
<th>Yield</th>
<th>Defect Rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1</td>
<td>0.682689492</td>
<td>0.317311</td>
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<tr>
<td>2</td>
<td>2</td>
<td>0.954499736</td>
<td>0.0455</td>
</tr>
<tr>
<td>3</td>
<td>3</td>
<td>0.997300204</td>
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<td>4</td>
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<td>6.33E-05</td>
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<tr>
<td>5</td>
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<td>0.999999427</td>
<td>5.73E-07</td>
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<tr>
<td>6</td>
<td>6</td>
<td><strong>0.999999980</strong></td>
<td>1.97E-09</td>
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<tr>
<td>7</td>
<td>7</td>
<td>0.99999999974</td>
<td>2.56E-12</td>
</tr>
</tbody>
</table>

Six-sigma performance is approximately 2 defects in a billion!
It is assumed that the performance or yield will drop, for some reason, by 1.5 sigma after a process has been established.

Initial “six-sigma” solutions really expect only 4.5 sigma performance in steady-state production.

Assumption: Processes of interest are Gaussian (Normal)

4.5 sigma performance corresponds to 3.4 defects in a million

Observation: Any Normally distributed random variable can be mapped to a $N(0,1)$ random variable by subtracting the mean and dividing by the variance.
Meeting the Real Six-Sigma Challenge

Six-Sigma or Else !!

Highly Statistical Concept !
The Six-Sigma Challenge

Two-sided capability:

Long-term Capability
Tails are 6.8 parts in a million

Short-term Capability
Tail is 2 parts in a billion

Six Sigma Performance is Very Good !!!
Example: Determine the maximum die area if the circuit yield is to initially meet the “six sigma” challenge for hard yield defects (Assume a defect density of 1cm$^{-2}$ and only hard yield loss). Is it realistic to set six-sigma die yield expectations on the design and process engineers?

Solution:

The “six-sigma” challenge requires meeting a 6 standard deviation yield with a Normal (0,1) distribution

$$Y_{6\text{sigma}} = 2F_N(6) - 1$$
Solution cont:

\[ Y_H = e^{-Ad} \]

\[ A = \frac{-\ln(Y_H)}{d} \]

\[ A = \frac{-\ln(0.999999998)}{1\text{cm}^{-2}} = 2.0 \times 10^{-9} \text{cm}^2 = 2.5 \times 10^5 \text{(Å)}^2 \]

This is comparable to the area required to fabricate a single transistor in a state of the art 20nm process.
Is it realistic to set six-sigma die hard yield expectations on the design and process engineers?

The best technologies in the world have orders of magnitude too many defects to build any useful integrated circuits with die yields that meet six-sigma performance requirements!!
Meeting the Real Six-Sigma Challenge

Six-Sigma or Else !!
Meeting the Real Six-Sigma Challenge

Improving a yield by even one sigma often is VERY challenging !!

Six-Sigma or Else !!
Statistics can be abused!

Many that are not knowledgeable incorrectly use statistics

Many use statistics to intentionally mislead the public

Some openly abuse statistics for financial gain or for manipulation purposes

Keep an open mind to separate “good” statistics from “abused” statistics
Meeting the Real Six-Sigma Challenge

How has Motorola fared with the 6-sigma approach?

Motorola, Inc. (pronounced ) was an American multinational telecommunications company based in Schaumburg, Illinois, which was eventually divided into two independent public companies, Motorola Mobility and Motorola Solutions on January 4, 2011, after losing $4.3 billion from 2007 to 2009.
Meeting the Real Six-Sigma Challenge

How has Motorola fared with the 6-sigma approach?

• Sold military activities to General Dynamics 2000/2001
• Sold automotive products in 2006
• Spun of discrete components as ON semiconductor in 1999
• Spun of SPS as Freescale in 2003
• Sold Motorola Mobility to Google in 2011
• Motorola Solutions has 23,000 employees, down from over 150,000 in mid ‘90s
Not every important Motorola innovation during Bob's time led to a physical product. For example, in the early 1980s—a period when American companies were struggling to compete with superior products pouring out of Japan—Motorola developed a system for total quality management called Six Sigma. (A Six Sigma process is one in which 99.99966 percent of products are free from manufacturing defects.) A good chunk of the Fortune 500, including General Electric, IBM, and Boeing, wound up adopting it.

NOTES: *They did so in large part by conducting layoffs and selling businesses. Motorola Solutions will shed 4,500 more jobs this fall, when Zebra Technologies completes its purchase of the company’s enterprise division. Data for 2014 as of June 30.

SOURCES: Google; Motorola Solutions.
Meeting the Real Six-Sigma Challenge

Six-sigma capability has almost nothing to do with optimizing profits and, if taken seriously, will likely guarantee a financial fiasco in most manufacturing processes.
Meeting the real Six-Sigma Challenge

Six-Sigma or Else!!

Actually optimizing a process to six-sigma performance will almost always guarantee financial disaster!
Meeting the real Six-Sigma Challenge

Six-Sigma or Else!!
Meeting the real Six-Sigma Challenge

Six-Sigma or Else !!

The concept of improving reliability (really profitability) is good – its just the statistics that are abused!
Meeting the real Six-Sigma Challenge

Six-Sigma or Else!!

I got the message
The Perception

Six-Sigma or Else!!

Earnings Per Die

Profit

Loss

-∞

Yield Variance

0

4.5σ

6σ
The Reality

- Designing for 4.5\(\sigma\) or 6\(\sigma\) yield variance will almost always guarantee large losses
- Yield targets should be established to optimize earnings not yield variance
The Perception on Yield

Perception is often that goal should be to get yields as close to 100% as possible
• Return on improving yield when yield is above 95% is small
• Inflection point could be at 99% or higher for some designs but below 50% for others
• Cost/good die will ultimately go to $\infty$ as yield approaches 100%

Designers goal should be to optimize profit, not arbitrary yield target
End of Lecture 3