EE 330
Lecture 34

- High Gain Amplifiers
- Differential Amplifiers
- MOS Amplifier Architectures
- Amplifier Biasing
- Digital Circuit Design
Can we use more cascoding to further increase the gain?
The double cascode

\[ A_V \approx -\left[ \frac{g_{m1}}{g_{01}} \right] \beta^2 \]

\[ g_{0CC} \approx \frac{g_{01}}{\beta^2} \]

- Further gain enhancement
- Further output impedance increase
- Limited applications, particularly at lower voltages, because signal swings at outputs are small
Review from Last Time

The Cascode Amplifier (consider n-ch MOS version)

Same issues for biasing with current source as for BJT case

\[ A_{VCC} \approx \begin{bmatrix} \frac{g_{m1} g_{m2}}{g_{01} g_{02}} \end{bmatrix} \]

\[ g_{0CC} \approx \begin{bmatrix} \frac{g_{01} g_{02}}{g_{m2}} \end{bmatrix} \]
The Cascode Amplifier

- Operational amplifiers often built with basic cascode configuration
- Usually configured as a differential structure when building op amps
- Have high output impedance (but can be buffered)
- Terms “telescopic cascode”, “folded-cascode”, and “regulated cascode” often refer to op amps based upon the cascode configuration
Cascade Configurations

Two-stage Cascade

\[ A_{VCB} = ? \]

\[ A_{VCM} = ? \]
Cascade Configurations

Two-stage Cascade

\[
A_{VCB} \approx \begin{bmatrix}
\frac{-g_{m1}}{g_{01} + g_{p2}} & -g_{m2} \\
g_{02} & g_{p2}
\end{bmatrix} \approx \frac{g_{m1}g_{m2}}{g_{p2}g_{02}} = \beta \frac{g_{m1}}{g_{02}}
\]

\[
A_{VCM} = \begin{bmatrix}
\frac{-g_{m1}}{g_{01}} & -g_{m2} \\
g_{02} & g_{01}
\end{bmatrix} = \frac{g_{m1}g_{m2}}{g_{01}g_{02}}
\]

- Significant increase in gain
- Gain is noninverting
- Comparable to that obtained with the cascode
Cascade Configurations

Two-stage Cascade

\[ A_{VCB} \approx \begin{bmatrix} -g_{m1} \\ g_{01} + g_{03} + g_{\pi 2} \end{bmatrix} \begin{bmatrix} -g_{m2} \\ g_{02} + g_{04} \end{bmatrix} = \frac{g_{m1}g_{m2}}{2g_{\pi 2}g_{02}} = \beta \frac{g_{m1}}{2g_{02}} \]

\[ A_{VCM} = \begin{bmatrix} -g_{m1} \\ g_{01} + g_{03} \end{bmatrix} \begin{bmatrix} -g_{m2} \\ g_{02} + g_{04} \end{bmatrix} = \frac{g_{m1}g_{m2}}{4g_{01}g_{02}} \]

Note factor or 2 and 4 reduction in gain due to actual current source bias
Cascade Configurations

- Large gains can be obtained by cascading
- Gains are multiplicative (when loading is included)
- Large gains used to build “Op Amps” and feedback used to control gain value
- Some attention is needed for biasing but it is manageable
- Minor variant of the two-stage cascade often used to built Op Amps
- Compensation of two-stage cascade needed if feedback is applied to maintain stability
- Three or more stages are seldom cascaded because no really good way to compensate to maintain stability
Differential Amplifiers

Basic operational amplifier circuit
Differential Amplifiers

Assume left-right matching
i.e. circuit (except for excitations) is symmetric
Differential Amplifiers

Common Mode Excitation

\[ V_C = \frac{V_1 + V_2}{2} \]

\[ V_D = V_2 - V_1 \]

Difference Mode Excitation

\[ V_1 = V_C - \frac{V_D}{2} \]

\[ V_2 = V_C + \frac{V_D}{2} \]

Analysis of two circuits is generally much easier than analysis of original circuit.
Differential Amplifiers

Common Mode Excitation

\[ V_{OUT1} = V_{OUT2} \]

\[ V_C \]

\[ Q_1 \to Q_1 \]

\[ R_1 \]

\[ V_{DD} \]

\[ V_{SS} \]

\[ I_{TAIL} \]

\[ V_{OUTQ} = V_{DD} \cdot R_1 \cdot \frac{I_{TAIL}}{2} \]

\[ A_C = \frac{V_{OUTC}}{V_C} = 0 \]

(A\textsubscript{C} will not be quite 0 if the tail current source is nonideal)
Differential Amplifiers

Difference Mode Excitation

Difference Mode Half Circuit

Theorem: The small-signal voltage of a symmetric linear network excited differentially is always 0 at every node on the axis of symmetry
Differential Amplifiers

**Difference Mode Excitation**

**Difference Mode Half Circuit**

\[
A_D = \frac{V_{OUT2}}{V_D} = - \frac{g_m}{2} R_1
\]

Theorem: The small-signal voltage of a symmetric linear network excited differentially is always 0 at every node on the axis of symmetry
Amplifier biasing is that part of the design of a circuit that establishes the desired operating point (or Q-point).

Goal is to invariably minimize the impact the biasing circuit has on the small-signal performance of a circuit.

Usually at most 2 dc power supplies are available and these are often fixed in value by system requirements – this restriction is cost driven.

Discrete amplifiers invariably involve adding biasing resistors and use capacitor coupling and bypassing.

Integrated amplifiers often use current sources which can be used in very large numbers and are very inexpensive.
Amplifier Biasing

Example:

\[ A_V = -g_m R_L \]

Desired small-signal circuit
Common Emitter Amplifier

Actual small-signal circuit

\[ A_V = -g_m \frac{R_L}{R_{C1}} \]
Amplifier Biasing

Example:

Desired small-signal circuit
Common Emitter Amplifier

Biased small-signal circuit

Biasing components shown in blue
Amplifier Biasing

Example:

Desired small-signal circuit
Common Collector Amplifier

Biased circuit

Biasing components shown in blue
Amplifier Biasing

Example:

Desired small-signal circuit
Inverting Feedback Amplifier

Biased circuit shown in blue
Darlington Configuration

- Current gain is approximately $\beta^2$
- Two diode drop between $B_{eff}$ and $E_{eff}$
Other Basic Configurations

- Same basic structure as Darlington Pair
- Current gain is approximately $\beta_n \beta_n$
- Current gain will not be as large when $\beta_p < \beta_p$
- Only one diode drop between $B_{\text{eff}}$ and $E_{\text{eff}}$
Other Basic Configurations

Low offset buffers

- Actually a CC-CC or a CD-CD cascade
- Significant drop in offset between input and output
- Biasing with DC current sources
Other Basic Configurations

- Attenuation factor is quite accurate (Determined by geometry)
- Infinite input impedance
- $M_1$ in triode, $M_2$ in saturation
- Actually can be a channel-tapped structure
Design Strategies

• Draw on Past Experience
• Often leads to Circuit or Architecture that can be modified or extended
• Identify the degrees of freedom in the design and the number of constraints and then systematically explore the design space
• Simulation-guided computer simulation is not an effective way of exploring a multi-variable design space!
MOS Amplifiers

- 1-1 mapping between almost all bipolar amplifiers and MOS amplifiers
- Simply replace BJT with MOS devices and redo the biasing

Small-signal gains for MOS circuits in terms of small-signal model parameters identical if set $g_{\pi} = 0$ for BJT circuits
MOS-Bipolar Amplifier Mapping

Common Emitter

Common Collector

Common Base

Common Source

Common Drain

Common Gate
MOS-Bipolar Amplifier Mapping

Example: Common Emitter – Common Source Circuits

\[ AV = \frac{-g_m}{g_o + G} \]

\[ R_{IN} = g_{\pi}^{-1} \]

\[ g_{\pi} = 0 \]

\[ AV = \frac{-g_m}{g_o + G} \]

\[ R_{IN} = \infty \]
Digital Circuit Design

Most of the remainder of the course will be devoted to digital circuit design
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates

- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Hierarchical Digital Design Domains:

- Behavioral:
- Structural:
- Physical

Multiple Levels of Abstraction
Hierarchical Digital Design Domains:

Behavioral:

Structural:

Physical

Bottom Up Design

Top Down Design
Hierarchical Digital Design Domains:

- Behavioral:
  - Structural:
  - Physical

Multiple Sublevels in Each Major Level
All Design Steps may not Fit Naturally in this Description
Hierarchical Analog Design Domains:

- Behavioral:
- Structural:
- Physical

Bottom Up Design → Top Down Design
Hierarchical Digital Design Domains:

**Behavioral**: Describes what a system does or what it should do

**Structural**: Identifies constituent blocks and describes how these blocks are interconnected and how they interact

**Physical**: Describes the constituent blocks to both the transistor and polygon level and their physical placement and interconnection

Multiple representations often exist at any level or sublevel
Example: Two distinct representations at the physical level (polygon sublevel)
Example: Two distinct representations at physical level (schematic sublevel)

\[ \frac{W}{L} = 4 \]

- \[ W = 4\mu, \quad L = 1\mu \]
- \[ W = 8\mu, \quad L = 2\mu \]

- \[ W_1, L \]
- \[ W_2, L \]
- \[ W_1 + W_2, L \]
Example: Two distinct representations at the structural/behavioral level (gate sublevel)

\[ C = A \oplus B \]
End of Lecture 34