EE 330
Lecture 34

Guest Lecture

Why are there so many Op Amps?

by Jerry Doorenbos of Texas Instruments
Op Amp Technology Overview

Developed by Art Kay, Thomas Kuehl, and Tim Green
Precision Amplifiers Applications Engineering
Texas Instruments – Tucson
Bipolar vs. CMOS / JFET

• Transistor technologies
  – Bipolar, CMOS and JFET

• Vos and Ib and Drift
  – Laser Trim, Package Trim, and Zero Drift

• Noise
  – JFET, MOSFET, and Bipolar (1/f noise)

• Input Structures
  – Rail-to-Rail, Charge Pump
  – Chopper (Zero-Drift)
    • Chopper Noise Sources
  – Input crossover distortion
Bipolar, CMOS, JFET (Op Amp input device structures)

1) **Current Controlled Device**
2) “Current Controlled Current Source”
3) \( I_c = I_b \times hfe \)
4) \( I_b = 0A \) turns bipolar off
5) Base is op amp +/- input
6) Highest Op Amp input current

1) **Voltage Controlled Device**
2) “Voltage Controlled Resistor”
3) \( V_{gs} > 2V \) controls \( R_{ds\_on} \)
4) \( V_{gs}=0V \) turns MOSFET off
5) Gate is op amp +/- input
6) Very Low Op Amp input current

1) **Voltage Controlled Device**
2) “Voltage Controlled Resistor”
3) \( 0V < V_{gs} < -2V \) controls \( R_{ds\_on} \)
4) \( V_{gs} < -2V \) turns JFET off
5) Gate is op amp +/- input
6) Very Low Op Amp input current

**NPN Bipolar**

**N-Channel CMOS**

**N-Channel JFET**
Vos & Ib: Model and Hand Calculations

- Voltage offset adds a dc error to Vout
- The offset contributed is unique to each device

\[
R_{eq} = \frac{R_f \cdot R_1}{R_f + R_1}
\]

\[
G_n = \frac{R_f}{R_1} + 1
\]

\[
V_{o_vos} = V_{os} \cdot G_n
\]

\[
V_{o_{ib+}} = I_b \cdot R_s \cdot G_n
\]

\[
V_{o_{ib-}} = I_b \cdot R_{eq} \cdot G_n
\]

\[
V_{o_os_{-ib}} = V_{o_vos} + V_{o_{ib+}} + V_{o_{ib-}}
\]
What’s inside the Amplifier – Bipolar vs. CMOS

VOS and Drift Trimming

Trim these resistors for Vos & Vos drift for Bipolar

Trim these resistors for Vos & Vos drift for CMOS

Bipolar input op amp

CMOS input op amp
Bipolar and CMOS
Op amp examples

<table>
<thead>
<tr>
<th>Model</th>
<th>Technology</th>
<th>Rail-to-rail</th>
<th>Supply V+ to V-</th>
<th>Op Current typ</th>
<th>Offset typ</th>
<th>Offset drift typ</th>
<th>Bias Current typ</th>
<th>Voltage noise 1 kHz</th>
<th>GBW</th>
<th>Slew rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA211</td>
<td>Bipolar</td>
<td>RRO</td>
<td>4.5 - 36 V</td>
<td>3.6 mA</td>
<td>60 uV</td>
<td>0.35 uV/°C</td>
<td>60 nA</td>
<td>1.1 nV/√Hz</td>
<td>45 MHz</td>
<td>27 V/us</td>
</tr>
<tr>
<td>OPA350</td>
<td>CMOS</td>
<td>RRIO</td>
<td>2.7 - 5.5 V</td>
<td>5.2 mA</td>
<td>150 uV</td>
<td>4 uV/°C</td>
<td>0.5 pA</td>
<td>16 nV/√Hz</td>
<td>38 MHz</td>
<td>22 V/us</td>
</tr>
</tbody>
</table>

• OPA2x11 - Ultra low Noise, low power, precision op amp
  – Ideal for driving high-precision 16-bit ADCs or buffering the output of high-resolution digital-to-analog converters DACs

• OPAx350 High-Speed, Single-Supply, Rail-to-Rail I/O
  – High-performance ADC driver, very high $C_{\text{Load}}$ drive capability
Inherent Drift of Bipolar vs. CMOS

- Drift is proportional to offset
- When Vos trimmed to zero, drift is near zero.
- Simple one step trim: just trim offset

- Frequently more curvature than bipolar
- When Vos trimmed to zero, drift remains.
- More complex two part trim: drift first, then offset
- Offset and drift trims interact, difficult to optimize both
Laser Trim – What does it look like?

- Bipolar, CMOS, JFET can be used
  - Only way to trim bipolar
- Trimmed in wafer form before package
- Laser makes narrow cuts in resistor
- Increases resistance continuously
- Circuit can be active, but laser may disturb circuit function—requires cutting in bursts (long test time)
- Generally each trim has a pair of resistors for bidirectional trim
Bipolar vs. CMOS
Op amps that utilize thin-film resistor laser trimming for improved offset and drift

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<th>Offset drift typ</th>
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<th>Voltage noise 1 kHz</th>
<th>GBW</th>
<th>Slew rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA1612</td>
<td>Bipolar</td>
<td>Out</td>
<td>4.5 – 36 V</td>
<td>3.6 mA</td>
<td>100 uV</td>
<td>1 uV/°C</td>
<td>60 nA</td>
<td>1.1 nV/√Hz</td>
<td>40 MHz</td>
<td>27 V/us</td>
</tr>
<tr>
<td>OPA320S</td>
<td>LV CMOS</td>
<td>RRIO</td>
<td>1.8 – 5.5 V</td>
<td>1.5 mA</td>
<td>40 uV</td>
<td>1.5 uV/°C</td>
<td>0.2 pA</td>
<td>8.5 nV/√Hz</td>
<td>20 MHz</td>
<td>10 V/us</td>
</tr>
</tbody>
</table>

- OPA1612 - SoundPlus™ High-Performance, Bipolar-Input Audio Op Amp
  - Achieves very low noise density with an ultralow distortion of 0.000015% at 1 kHz.
  - Rail-to-rail output swing to within 600 mV with a 2-kΩ load

- OPA320S - 20-MHz, Low-Noise, RRI/O, Low operating current, with shutdown
  - A combination of very low noise, high gain-bandwidth, and fast slew make it ideal for signal conditioning and sensor amplification requiring high gain
Package level electronic trim, e-trim™

- CMOS op amps only due to digital circuitry requirements
- Standard pinout
  - Trim data is entered through output current load
- Blow and set internal fuses
- Disable trim mechanism after the trim is completed
  - No customer access to trim function
- Programmed fuses are read at each power-on
# e-trim™ OpAmps: OPA376 vs OPA192

## Comparison Table

<table>
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<th>Offset drift typ</th>
<th>Bias Current typ</th>
<th>Voltage noise 1 kHz</th>
<th>GBW</th>
<th>Slew rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA376</td>
<td>LV CMOS</td>
<td>RRIO</td>
<td>2.2 – 5.5 V</td>
<td>760 uA</td>
<td>5 uV</td>
<td>0.26 uV/°C</td>
<td>0.2 pA</td>
<td>7.5 nV/√Hz</td>
<td>5.5 MHz</td>
<td>2 V/us</td>
</tr>
<tr>
<td>OPA192</td>
<td>HV CMOS</td>
<td>RRIO</td>
<td>8 – 36 V</td>
<td>1 mA</td>
<td>5 uV</td>
<td>0.1 uV/°C</td>
<td>5 pA</td>
<td>5.5 nV/√Hz</td>
<td>10 MHz</td>
<td>20 V/us</td>
</tr>
</tbody>
</table>

- **OPA376** – Precision, Low-noise, Low offset, Low quiescent current
  - Well-suited for driving SAR ADCs as well as 24-bit and higher resolution converters

- **OPA192** - Precision, 36 V, Low offset, Fast slewing
  - differential input-voltage range to the supply rail
  - high output current (±65 mA)
What’s inside the Amplifier – Bipolar vs. CMOS

Understanding $I_B$

Bipolar input op amp

CMOS input op amp

$I_b$ from diode leakage $I_b \approx \pm 1\text{pA}$

$I_b$ from base current $\approx 100\text{nA}$

Bipolar input does have ESD cells, but $I_b \gg I_{\text{leak}}$
Bipolar - Bias Current Cancellation

**Bipolar Ib**

<table>
<thead>
<tr>
<th>Typical</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>w/o Ib cancellation</td>
<td>100nA</td>
</tr>
<tr>
<td>With Ib cancellation</td>
<td>1nA</td>
</tr>
</tbody>
</table>

![Bias Current Cancellation Diagram]

- **Vcc**
- **IS**
- **Q1**
- **Q2**
- **R1**
- **R2**
- **Vin1**
- **Vin2**
- **Ib1**
- **Ib2**
- **Ib Cancel Circuit**
- **Σ**
## Bipolar - Bias Current Cancellation
### Cancellation vs non-cancellation

<table>
<thead>
<tr>
<th>Model</th>
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<th>Rail-to-rail</th>
<th>Supply V+ to V-</th>
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<th>Offset drift typ</th>
<th>Bias Current typ</th>
<th>Voltage noise 1 kHz</th>
<th>GBW</th>
<th>Slew rate</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>OPA209</strong></td>
<td>Bipolar with Ib cancel</td>
<td>RRO</td>
<td>4.5 - 36 V</td>
<td>2.2 mA</td>
<td>35 uV</td>
<td>0.05 uV/°C</td>
<td>1 nA typ 4.5 nA max</td>
<td>2.2 nV/√Hz</td>
<td>18 MHz</td>
<td>6.4 V/us</td>
</tr>
<tr>
<td><strong>OPA211</strong></td>
<td>Bipolar w/o Ib cancel</td>
<td>RRO</td>
<td>4.5 - 36 V</td>
<td>3.6 mA</td>
<td>60 uV</td>
<td>0.35 uV/°C</td>
<td>60 nA typ 175 nA max</td>
<td>1.1 nV/√Hz</td>
<td>45 MHz</td>
<td>27 V/us</td>
</tr>
</tbody>
</table>

- **OPA209** – 36 V, low power, noise, offset, drift and input bias current
  - Suitable for fast, high-precision applications. Has fast settling time to 16-bit accuracy

- **OPA2x11** - Ultra low Noise, low power, precision op amp
  - Ideal for driving high-precision 16-bit ADCs, or buffering the output of high-resolution DACs
Bipolar vs. CMOS bias current drift (Ib vs Temp)

Bipolar amplifier:
In this case you see a dramatic increase in bias current at 75 °C.

CMOS amplifier:
In this case you see a dramatic increase in bias current at 25 °C. Note the logarithmic vertical bias current scale. Ib about doubles every 10 °C.
Current Noise performance

CMOS: $I_{n_{350}} = 4 \text{ fA}/\sqrt{\text{Hz}}$
JFET: $I_{n_{827}} = 2.2 \text{ fA}/\sqrt{\text{Hz}}$
Bipolar: $I_{n_{277}} = 200 \text{ fA}/\sqrt{\text{Hz}}$

Note: CMOS current noise has minimal 1/f, but it may be significant in bipolar
JFET, Bipolar, and CMOS Noise

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<th>Offset drift typ</th>
<th>Bias Current typ</th>
<th>Voltage noise 1 kHz</th>
<th>GBW</th>
<th>Slew rate</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA827</td>
<td>JFET + Bipolar</td>
<td>No</td>
<td>8 – 36 V</td>
<td>4.8 mA</td>
<td>75 uV</td>
<td>0.1 uV/°C</td>
<td>3 pA</td>
<td>4 nV/√Hz</td>
<td>22 MHz</td>
<td>28 V/us</td>
</tr>
<tr>
<td>OPA227</td>
<td>Bipolar</td>
<td>No</td>
<td>10 – 36 V</td>
<td>3.7 mA</td>
<td>10 uV</td>
<td>0.3 uV/°C</td>
<td>2.5 nA</td>
<td>3 nV/√Hz</td>
<td>8 MHz</td>
<td>2.3 V/us</td>
</tr>
<tr>
<td>OPA350</td>
<td>CMOS</td>
<td>RRIO</td>
<td>2.7 – 5.5 V</td>
<td>5.2 mA</td>
<td>150 uV</td>
<td>4 uV/°C</td>
<td>0.5 pA</td>
<td>16 nV/√Hz</td>
<td>38 MHz</td>
<td>22 V/us</td>
</tr>
</tbody>
</table>

- OPA827 - Low-Noise, High-Precision, JFET-Input
  - Precision 16-bit to 18-bit mixed signal systems, transimpedance amplifiers
- OPA227 - High Precision, Low Noise
  - Ideal for applications requiring both AC and precision DC performance
- OPAX350 High-Speed, Single-Supply, Rail-to-Rail I/O
  - High-performance ADC driver, very high $C_{\text{Load}}$ drive capability
OPA703 Complementary CMOS – Rail-to-Rail

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITION</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT VOLTAGE RANGE</td>
<td>$V_{CM}$</td>
<td>$V_s = \pm 5V, (V-) - 0.3V &lt; V_{CM} &lt; (V+) + 0.3V$</td>
<td>(V-) - 0.3</td>
<td>70</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>CMRR</td>
<td>$V_s = \pm 5V, (V-) &lt; V_{CM} &lt; (V+)$</td>
<td>68</td>
<td>90</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = \pm 5V, (V-) - 0.3V &lt; V_{CM} &lt; (V+) - 2V$</td>
<td>80</td>
<td>96</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_s = \pm 5V, (V-) &lt; V_{CM} &lt; (V+) - 2V$</td>
<td>74</td>
<td>dB</td>
<td></td>
</tr>
</tbody>
</table>

Diagram showing the circuitry of the OPA703 with symbols for $V_{IN+}$, $V_{IN-}$, $V_s$, $Q_1$, $Q_2$, $Q_3$, and $Q_4$.

Graph illustrating the input offset voltage in microvolts ($\mu V$) vs. common mode voltage (V).
Complementary CMOS – Rail-to-Rail
A abrupt offset change at input P-ch/ N-ch switchover point

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<tr>
<th>Model</th>
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<th>Supply V+ to V-</th>
<th>Op Current typ</th>
<th>Offset typ</th>
<th>Offset drift typ</th>
<th>Bias Current typ</th>
<th>CMRR rail-to-rail input</th>
<th>PSRR</th>
<th>Open-loop Gain</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA703</td>
<td>12 V CMOS</td>
<td>RRIO</td>
<td>4 - 12 V</td>
<td>160 uA</td>
<td>35 uV</td>
<td>4 uV/°C</td>
<td>1 pA</td>
<td>90 dB (V+)-0.3 V</td>
<td>20 uV/V</td>
<td>110 dB RL = 20 k</td>
</tr>
<tr>
<td>OPA314</td>
<td>LV CMOS</td>
<td>RRIO</td>
<td>1.8 – 5.5 V</td>
<td>150 uA</td>
<td>60 uV</td>
<td>1 uV/°C</td>
<td>0.4 pA</td>
<td>96 dB (V+)-1.3 V</td>
<td>25 uV/V</td>
<td>115 dB RL = 2 k</td>
</tr>
</tbody>
</table>

- The CMRR is often specified
  - Over an optimal range having higher performance
  - The full rail-to-rail input range having somewhat reduced performance

OPA703  0 to +5 V input, $V_S \pm 5$ V  
OPA314  ±2.75 V input, $V_S \pm 2.75$ V
Input Crossover Distortion

Vout vs. Time

![Graph showing Vout vs. Time](image)

Vout vs. Time (Zoomed In)

![Graph showing Zoomed In Vout vs. Time](image)

Input Offset Voltage

![Graph showing Input Offset Voltage](image)

Common Mode Voltage

![Graph showing Common Mode Voltage](image)

Input Offset Voltage (mV)

![Graph showing Input Offset Voltage (Zoomed In)](image)
OPA365 MOSFET Charge Pump – Rail-to-Rail

- Uses charge pump to raise $V_{+}$ rail and overcome $V_{sat} + V_{gs}$ of input PMOS FETs
- Charge pump switches at 10 MHz which is within op amp 50 MHz GBW
- Pump design is patented and has very low ripple
- Charge pump noise is small relative to broadband noise

$V_{OUT} = +V_{S} + 1.8V$
MOSFET Charge Pump – Rail-to-Rail
Eliminates input stage crossover distortion

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<th>Offset typ</th>
<th>Offset drift typ</th>
<th>Bias Current typ</th>
<th>CMRR rail-to-rail input</th>
<th>PSRR</th>
<th>Open-loop Gain ( R_L = 10 , \text{k}\Omega)</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA365</td>
<td>LV CMOS</td>
<td>RRIO</td>
<td>2.2 – 5.5 V</td>
<td>4.6 mA</td>
<td>100 uV</td>
<td>1 uV/°C</td>
<td>0.2 pA</td>
<td>120 dB</td>
<td>10 uV/V</td>
<td>120 dB</td>
</tr>
<tr>
<td>OPA322</td>
<td>LV CMOS</td>
<td>RRIO</td>
<td>1.8 – 5.5 V</td>
<td>1.5 mA</td>
<td>500 uV</td>
<td>1.5 uV/°C</td>
<td>0.2 pA</td>
<td>100 dB</td>
<td>10 uV/V</td>
<td>130 dB</td>
</tr>
</tbody>
</table>

- OPA365 – RRIO, Wide 50 MHz bandwidth, Low distortion, High CMRR
  - Features high performance that is optimized for low voltage, single-supply applications
- OPA322 – RRIO, Wide 20 MHz bandwidth, Low current
  - Features low distortion, 0.0005% THD+N and low noise, 8.5 nV/√Hz at 1 kHz
- Excellent CMRR without the input crossover of traditional complementary P-N MOSFET input stages. Low offset and drift, high CMRR, PSRR, and AOL performances
Chopper and Zero Drift MOSFET – Rail-to-Rail

“Chopper” and “Zero-Drift” CMOS Op Amps use complementary input P-ch/ N-ch concept with Digital Calibration for Offset Correction

\[ V_{IN^-} \]

\[ V_{IN^+} \]

\[ -V_{SUPPLY} \]
Comparing Common Architectures vs. Chopper

<table>
<thead>
<tr>
<th>CMOS Vos/drift</th>
<th>Typ Vos (uV)</th>
<th>Typ Drift (uV/C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Uncorrected</td>
<td>1000</td>
<td>5</td>
</tr>
<tr>
<td>Zero Drift (chopper)</td>
<td>10</td>
<td>0.05</td>
</tr>
<tr>
<td>Package Trim</td>
<td>10</td>
<td>0.5</td>
</tr>
</tbody>
</table>
## Chopper Op Amps
Chopper techniques provide low offset voltage, near zero-drift over time and temperature

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<th>Offset drift typ</th>
<th>Bias Current typ</th>
<th>CMRR rail-to-rail input</th>
<th>PSRR</th>
<th>Open-loop Gain $R_L = 10 , \text{k}\Omega$</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPA333</td>
<td>LV CMOS</td>
<td>RRIO</td>
<td>1.8 – 5.5 V</td>
<td>17 uA</td>
<td>2 uV</td>
<td>0.02 uV/°C</td>
<td>70 pA</td>
<td>130 dB</td>
<td>1 uV/V</td>
<td>130 dB</td>
</tr>
<tr>
<td>OPA188</td>
<td>HV CMOS</td>
<td>RRO</td>
<td>4- 36 V</td>
<td>425 uA</td>
<td>6 uV</td>
<td>0.03 uV/°C</td>
<td>160 pA</td>
<td>134 dB</td>
<td>0.075 uV/V</td>
<td>134 dB</td>
</tr>
</tbody>
</table>

- OPA333 - 1.8 V, Precision, microPower, Rail-to-Rail Input and Output
- OPA2188 – 36 V, Precision, Low-Noise, Rail-to-Rail Output

They provide:
- Excellent CMRR without the crossover of traditional complementary P-N MOSFET input stages
- Very low offset and drift, high CMRR, PSRR, and AOL performances
## Summary CMOS vs. Bipolar vs. JFET

<table>
<thead>
<tr>
<th>Parameter</th>
<th>CMOS</th>
<th>Bipolar</th>
<th>JFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vos</td>
<td>✗</td>
<td>✓</td>
<td>✗</td>
</tr>
<tr>
<td></td>
<td>Generally higher than bipolar. Complex trim. Inherent ≈ 5mV, Trimmed ≈ 500uV</td>
<td>Generally lower than JFET and CMOS. Laser Trim Only. Inherent ≈ 200uV, Trimmed ≈ 20uV</td>
<td>Generally higher than bipolar. Complex laser trim. Inherent ≈ 1mV, Trimmed ≈ 100uV</td>
</tr>
<tr>
<td></td>
<td>Can use zero drift tech, or and package-level e-trim.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Vos Drift</td>
<td>✗</td>
<td>✓</td>
<td>✗</td>
</tr>
<tr>
<td>Ib</td>
<td>✓</td>
<td>✗</td>
<td>✓</td>
</tr>
<tr>
<td></td>
<td>Low compared with bipolar</td>
<td>Much higher than CMOS and JFET. Can use bias current cancellation. Inherent ≈ 100nA, Canceled ≈ 1nA</td>
<td>Low compared with bipolar</td>
</tr>
<tr>
<td></td>
<td>Ib ≈ 1pA @ 25C</td>
<td></td>
<td>Ib ≈ 1pA @ 25C</td>
</tr>
<tr>
<td>Ib Drift</td>
<td>✗</td>
<td>✓</td>
<td>✗</td>
</tr>
<tr>
<td></td>
<td>Doubles every 10C, diode leakage</td>
<td>Small compared to room temp</td>
<td>Doubles every 10C, diode leakage</td>
</tr>
<tr>
<td></td>
<td>IB room ≈ 1nA, T = 25C</td>
<td>IB room ≈ 1nA, T = 25C</td>
<td>IB room ≈ 1nA, T = 25C</td>
</tr>
<tr>
<td></td>
<td>IB hot ≈ 1000pA, T = 125C</td>
<td>IB hot ≈ 3nA, T = 125C</td>
<td>IB hot ≈ 1000pA, T = 125C</td>
</tr>
<tr>
<td>Ibos</td>
<td>✗</td>
<td>✓</td>
<td>✗</td>
</tr>
<tr>
<td></td>
<td>Large offset current that is comparable to Ib. Don’t use resistor to cancel effects. Ib ≈ ±1pA, Ibos = ±1pA</td>
<td>When bias current cancellation is not used Ibos is low relative to Ib. Resistor can help cancel effects. Ib = 100nA, Ibos = ±1nA</td>
<td>Large offset current that is comparable to Ib. Don’t use resistor to cancel effects. Ib ≈ ±1pA, Ibos = ±1pA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>When bias current cancellation is used Ibos is comparable to Ib. Don’t use resistor to cancel effects. Ib = ±1nA, Ibos = ±1nA</td>
<td></td>
</tr>
</tbody>
</table>

**Notes:**
- CMOS: Complementary Metal-Oxide-Semiconductor
- Bipolar: Bipolar Transistor
- JFET: Junction Field-Effect Transistor
<table>
<thead>
<tr>
<th>Parameter</th>
<th>CMOS</th>
<th>Bipolar</th>
<th>JFET</th>
</tr>
</thead>
<tbody>
<tr>
<td>Broadband Noise</td>
<td>☒ Generally higher than bipolar. Noise decreases to the square root of Id.</td>
<td>☑ Generally lower than JFET and CMOS. Noise decreases directly with Id.</td>
<td>☒ Slightly higher than Bipolar</td>
</tr>
<tr>
<td>1/f Noise</td>
<td>☒ Generally worse than bipolar. Noise Corner &gt; 1kHz</td>
<td>☑ Generally better than CMOS. Noise Corner &lt; 10Hz</td>
<td>☑ Generally better than CMOS, but not as good as bipolar. Noise Corner &lt; 100Hz</td>
</tr>
<tr>
<td>Back-to-Back Diodes</td>
<td>☑ May or may not be required. Check Data Sheet!</td>
<td>☒ Generally required</td>
<td>☑ Not required. Check Data Sheet</td>
</tr>
<tr>
<td>Integrated Digital?</td>
<td>☑ Yes. i.e. Chopper, package trim</td>
<td>☒ No</td>
<td>☒ No</td>
</tr>
<tr>
<td>Rail to Rail Input</td>
<td>☑ Yes</td>
<td>☒ No</td>
<td>☒ Not common. Difficult</td>
</tr>
<tr>
<td>Rail to Rail Output</td>
<td>Very close to the rail. 10mV</td>
<td>Close to the rail. 200mV</td>
<td>Same as bipolar</td>
</tr>
<tr>
<td>Output vs. Load</td>
<td>☒ Falls off quickly with load. Ron of output transistor.</td>
<td>☑ Relatively flat until you reach current limit. Vsat not related to Ron as with CMOS.</td>
<td>Same as bipolar</td>
</tr>
</tbody>
</table>
How do I “Pick An Op Amp?”
Op Amp Selection – 1st Criteria
“Voltage, Current, and Speed”

- Bandwidth
- Supply Voltage
- Voltage
- Speed
- Current
- Iq
Op Amp Selection – 2nd Criteria

Current:
1) **Supply Current (1st)**
2) Output Current
3) Input Bias Current
4) Input Current Noise

Voltage:
1) **Supply (1st)**
2) Input Offset Voltage
3) Input Noise Voltage
4) Common Mode Input
5) Output Swing

Speed:
1) **Bandwidth (1st)**
2) Slew Rate
3) Output Impedance

Other:
1) Package
2) Single, Dual, Quad?
3) Price
Thank you