Digital Circuits

Characterization of CMOS Inverter
Static CMOS Logic Gates
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
  - Characterization of CMOS Inverter
- Static CMOS Logic Gates
  - Ratio Logic
- Propagation Delay
  - Simple analytical models
  - Elmore Delay
- Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Review from last time:

The basic logic gates

The characteristics of any gate logic family can be expressed rather simply in terms of the characteristics of the basic inverter in that logic family.
Review from last time:

The basic logic gates

It suffices to characterize the inverter of a logic family and then express the performance of other gates in that family in terms of the performance of the inverter.

What characteristics are required and desirable for an inverter to form the basis for a useful logic family?
Desirable and/or Required Logic Family Characteristics

1. High and low logic levels must be uniquely distinguishable (even in a long cascade)
2. Capable of driving many loads (good fanout)
3. Fast transition times (but in some cases, not too fast)
4. Good noise margins (low error probabilities)
5. Small die area
6. Low power consumption
7. Economical process requirements
Desirable and/or Required Logic Family Characteristics

8. Minimal noise injection to substrate  
9. Low leakage currents  
10. No oscillations during transitions  
11. Compatible with synthesis tools  
12. Characteristics do not degrade too much with temperature  
13. Characteristics do not vary too much with process variations

Are some of these more important than others?

Yes! – must have well-defined logic levels for circuits to even function as logic
Review from last time:

The two-inverter loop

\[ \text{Standard 6-transistor SRAM Cell} \]
When $V_{\text{OUT}} = V_{\text{IN}}$ for the inverter, $V'_{\text{OUT}}$ is also equal to $V_{\text{IN}}$. Thus the intersection point for $V_{\text{OUT}} = V_{\text{IN}}$ in the inverter transfer characteristics (ITC) is also an intersection point for $V'_{\text{OUT}} = V_{\text{IN}}$ in the inverter-pair transfer characteristics (IPTC).
The inverter-pair transfer characteristics must have three unique intersection points with the $V'_{\text{OUT}} = V_{\text{IN}}$ line.

The two extreme intersection points of the inverter-pair transfer characteristics with the $V'_{\text{OUT}} = V_{\text{IN}}$ line are $V_H$ and $V_L$.

Can we legislate $V_H$ and $V_L$ for a logic family?
Transfer characteristics of the static CMOS inverter

Review from last time:
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 1  $M_1$ triode, $M_2$ cutoff

\[
I_{D1} = \mu_n C_{oxn} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}
\]

$\quad I_{D2} = 0$

Equating $I_{D1}$ and $-I_{D2}$ we obtain:

\[
0 = \mu_n C_{oxn} \frac{W_1}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}
\]

It can be shown that setting the first product term to 0 will not verify, thus

\[
V_{OUT} = 0
\]

valid for:

\[
V_{GS1} \geq V_{Tn} \quad V_{DS1} < V_{GS1} - V_{Tn} \quad V_{GS2} \geq V_{Tp}
\]

thus, valid for:

\[
V_{IN} \geq V_{Tn} \quad V_{OUT} < V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \geq V_{Tp}
\]
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 1  \( M_1 \) triode, \( M_2 \) cutoff

\[ V_{\text{out}} = 0 \]
Transfer characteristics of the static CMOS inverter (Neglect $\lambda$ effects)

Case 1  \( M_1 \) triode, \( M_2 \) cutoff

\[ V_{\text{out}} = 0 \]
Review from last time:

Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Partial solution:
Regions of Operation for Devices in CMOS inverter.
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 2  M₁ triode, M₂ sat
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 2 $M_1$ triode, $M_2$ sat

$$I_{D1} = \mu_n C_{Ox} \frac{W}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

$$I_{D2} = -\frac{\mu_p C_{Oxp}}{2} \frac{W}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} \right)^2$$

Equating $I_{D1}$ and $-I_{D2}$ we obtain:

$$\frac{\mu_p C_{Oxp}}{2} \frac{W}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} \right)^2 = \mu_n C_{Ox} \frac{W}{L_1} \left( V_{IN} - V_{Tn} - \frac{V_{OUT}}{2} \right) V_{OUT}$$

valid for:

$$V_{GS1} \geq V_{Tn} \quad V_{DS1} < V_{GS1} - V_{Tn} \quad V_{GS2} \leq V_{Tp} \quad V_{DS2} \leq V_{GS2} - V_{T2}$$

thus, valid for:

$$V_{IN} \geq V_{Tn} \quad V_{OUT} < V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \leq V_{Tp} \quad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 2 $M_1$ triode, $M_2$ sat

$V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp}$

$V_{IN} \geq V_{Tn}$

$V_{OUT} < V_{IN} - V_{Tn}$

$V_{IN} - V_{DD} \leq V_{Tp}$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 2 \hspace{2mm} M_1 \text{ triode, } M_2 \text{ sat}

\begin{align*}
V_{\text{OUT}} - V_{\text{DD}} & \leq V_{\text{IN}} - V_{\text{DD}} - V_{\text{TP}} \\
V_{\text{IN}} & \geq V_{\text{Tn}} \\
V_{\text{OUT}} & < V_{\text{IN}} - V_{\text{Tn}} \\
V_{\text{IN}} - V_{\text{DD}} & \leq V_{\text{TP}}
\end{align*}
Transfer characteristics of the static CMOS inverter

Partial solution:
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3 $M_1$ sat, $M_2$ sat
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 3 $M_1$ sat, $M_2$ sat

$$I_{D1} = \frac{nC_{Ox}}{2} \frac{W_1}{L_1} (V_{IN} - V_{Tn})^2$$

$$I_{D2} = \frac{pC_{Oxp}}{2} \frac{W_2}{L_2} (V_{IN} - V_{DD} - V_{Tp})^2$$

Equating $I_{D1}$ and $-I_{D2}$ we obtain:

$$\frac{pC_{Oxp}}{2} \frac{W_2}{L_2} (V_{IN} - V_{DD} - V_{Tp})^2 = \frac{nC_{Oxn}}{2} \frac{W_1}{L_1} (V_{IN} - V_{Tn})^2$$

Which can be rewritten as:

$$\sqrt{\frac{pC_{Oxp}}{2} \frac{W_2}{L_2}} (V_{DD} + V_{Tp} - V_{IN}) = \sqrt{\frac{nC_{Oxn}}{2} \frac{W_1}{L_1}} (V_{IN} - V_{Tn})$$

Which can be simplified to:

$$V_{IN} = \frac{(V_{Tn})}{\sqrt{\frac{nC_{Oxn}}{2} \frac{W_1}{L_1}}} + (V_{DD} + V_{Tp}) \sqrt{\frac{pC_{Oxp}}{2} \frac{W_2}{L_2}}$$

This is a vertical line
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 3  \(M_1\) sat, \(M_2\) sat

\[
V_{IN} = \frac{(V_{Tn}) \sqrt{\frac{\mu_n C_{Ox_n} W_1}{2 L_1}} + (V_{DD} + V_{T_D}) \sqrt{\frac{\mu_p C_{Ox_p} W_2}{2 L_2}}}{\sqrt{\frac{\mu_n C_{Ox_n}}{2 L_1}} + \sqrt{\frac{\mu_p C_{Ox_p}}{2 L_2}}}
\]

Since \(C_{Ox_n} \approx C_{Ox_p} = C_{ox}\) this can be simplified to:

\[
V_{IN} = \frac{(V_{Tn}) \sqrt{\frac{W_1}{L_1}} + (V_{DD} + V_{T_D}) \sqrt{\frac{\mu_p W_2}{\mu_n L_2}}}{\sqrt{\frac{W_1}{L_1}} + \sqrt{\frac{\mu_p W_2}{\mu_n L_2}}}
\]

valid for:

\[
V_{GS1} \geq V_{Tn} \quad V_{DS1} \geq V_{GS1} - V_{Tn} \quad V_{GS2} \leq V_{T_D} \quad V_{DS2} \leq V_{GS2} - V_{T_2}
\]

thus, valid for:

\[
V_{IN} \geq V_{Tn} \quad V_{OUT} \geq V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \leq V_{T_D} \quad V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{T_D}
\]
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 3  $M_1$ sat, $M_2$ sat

\[ V_{OUT} - V_{DD} \leq V_{IN} - V_{DD} - V_{Tp} \]
\[ V_{IN} \geq V_{Tn} \]
\[ V_{OUT} \geq V_{IN} - V_{Tn} \]
\[ V_{IN} - V_{DD} \leq V_{Tp} \]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Partial solution:
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 3 \( M_1 \text{ sat}, M_2 \text{ sat} \)

\[
V_{\text{OUT}} - V_{\text{DD}} \leq V_{\text{IN}} - V_{\text{DD}} - V_{\text{TP}} \\
V_{\text{IN}} \geq V_{\text{Tn}} \\
V_{\text{OUT}} \geq V_{\text{IN}} - V_{\text{Tn}} \\
V_{\text{IN}} - V_{\text{DD}} \leq V_{\text{TP}}
\]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 4 $M_1$ sat, $M_2$ triode
Transfer characteristics of the static CMOS inverter

(Neglect λ effects)

Case 4  \( M_1 \) sat, \( M_2 \) triode

\[
I_{D1} = \frac{\mu_n C_{Ox_n} W_1}{2} \left( V_{IN} - V_{Tn} \right)^2
\]

\[
I_{D2} = -\mu_p C_{Ox_p} \frac{W_2}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT} - V_{DD}}{2} \right) \cdot (V_{OUT} - V_{DD})
\]

Equating \( I_{D1} \) and \( -I_{D2} \) we obtain:

\[
\frac{\mu_n C_{Ox_n} W_1}{2} \left( V_{IN} - V_{Tn} \right)^2 = \mu_p C_{Ox_p} \frac{W_2}{L_2} \left( V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT} - V_{DD}}{2} \right) \cdot (V_{OUT} - V_{DD})
\]

valid for:

\[
V_{GS1} \geq V_{Tn} \quad V_{DS1} \geq V_{GS1} - V_{Tn} \quad V_{GS2} \leq V_{Tp} \quad V_{DS2} > V_{GS2} - V_{T2}
\]

thus, valid for:

\[
V_{IN} \geq V_{Tn} \quad V_{OUT} \geq V_{IN} - V_{Tn} \quad V_{IN} - V_{DD} \leq V_{Tp} \quad V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{Tp}
\]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 4  $M_1$ sat, $M_2$ triode

\[ V_{\text{OUT}} - V_{\text{DD}} > V_{\text{IN}} - V_{\text{DD}} - V_{T_p}, \]
\[ V_{\text{IN}} \geq V_{T_n}, \]
\[ V_{\text{OUT}} \geq V_{\text{IN}} - V_{T_n}, \]
\[ V_{\text{IN}} - V_{\text{DD}} \leq V_{T_p}. \]
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 4 \( M_1 \) sat, \( M_2 \) triode

\[
\begin{align*}
V_{\text{OUT}} & \geq V_{\text{IN}} - V_{\text{TP}} - V_{\text{DD}} \\
V_{\text{IN}} & \geq V_{Tn} \\
V_{\text{OUT}} & \geq V_{\text{IN}} - V_{Tn} \\
V_{\text{IN}} - V_{\text{DD}} & \leq V_{\text{TP}}
\end{align*}
\]
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Partial solution:
Transfer characteristics of the static CMOS inverter
(Neglect λ effects)

Case 4  $M_1$ cutoff, $M_2$ triode
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 5  $M_1$ cutoff, $M_2$ triode

$I_{d1} = 0$

$I_{d2} = -\mu_p C_{ox} \frac{W^2}{L^2} \left( V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT} - V_{DD}}{2} \right) \bullet (V_{OUT} - V_{DD})$

Equating $I_{d1}$ and $-I_{d2}$ we obtain:

$$\mu_p C_{ox} \frac{W^2}{L^2} \left( V_{IN} - V_{DD} - V_{Tp} - \frac{V_{OUT} - V_{DD}}{2} \right) \bullet (V_{OUT} - V_{DD}) = 0$$

valid for:

$$V_{GS1} < V_{Tn}$$
$$V_{GS2} \leq V_{Tp}$$
$$V_{DS2} > V_{GS2} - V_{T2}$$

thus, valid for:

$$V_{IN} < V_{Tn}$$
$$V_{IN} - V_{DD} \leq V_{Tp}$$
$$V_{OUT} - V_{DD} > V_{IN} - V_{DD} - V_{Tp}$$
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

Case 5  $M_1$ cutoff, $M_2$ triode
Transfer characteristics of the static CMOS inverter
(Neglect \( \lambda \) effects)

Case 5 \( M_1 \) cutoff, \( M_2 \) triode

\[
\begin{align*}
V_{\text{IN}} - V_{\text{DD}} &> V_{\text{IN}} - V_{\text{DD}} - V_{\text{Tp}} \\
V_{\text{IN}} < V_{\text{Tn}} \\
V_{\text{IN}} - V_{\text{DD}} &\leq V_{\text{Tp}}
\end{align*}
\]
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)
Transfer characteristics of the static CMOS inverter
(Neglect $\lambda$ effects)

From Case 3 analysis:

$$V_{IN} = \frac{(V_{Tn} + (V_{DD} + V_{Tp}) \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}})}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}$$
Inverter Transfer Characteristics of Inverter Pair

\[ V_{\text{IN}} \rightarrow V'_{\text{OUT}} \]
Sizing of the Basic CMOS Inverter

How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?
How should $M_1$ and $M_2$ be sized?

How many degrees of freedom are there in the design of the inverter?

\[ \{ W_1, W_2, L_1, L_2 \} \quad \text{4 degrees of freedom} \]

But in basic device model and in most performance metrics, $W_1/L_1$ and $W_2/L_2$ appear as ratios

\[ \{ W_1/L_1, W_2/L_2 \} \quad \text{effectively 2 degrees of freedom} \]
How should $M_1$ and $M_2$ be sized?

\{ W_1, W_2, L_1, L_2 \} \quad 4 \text{ degrees of freedom} \quad \text{Usually pick } L_1 = L_2 = L_{\text{min}}

\{ W_1/L_1, W_2/L_2 \} \quad \text{effectively 2 degrees of freedom}

How are $W_1$ and $W_2$ chosen?

Depends upon what performance parameters are most important for a given application!
How should $M_1$ and $M_2$ be sized?

Usually pick $L_1 = L_2 = L_{\text{min}}$

\[
\{ \frac{W_1}{L_1}, \frac{W_2}{L_2} \} \quad \text{2 remaining degrees of freedom}
\]

One popular sizing strategy:
1. Pick $W_1 = W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{\text{DD}}/2$
How should $M_1$ and $M_2$ be sized? 

pick $L_1=L_2=L_{\text{min}}$

One popular sizing strategy:
1. Pick $W_1=W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{DD}/2$

Observe Case 3 provides expression for $V_{\text{TRIP}}$

Thus, at the trip point,

$$V_{\text{OUT}} = V_{\text{IN}} = V_{\text{TRIP}} = \frac{(V_{\text{Tn}}) + (V_{\text{DD}} + V_{\text{Tp}}) \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}{1 + \sqrt{\frac{\mu_p W_2 L_1}{\mu_n W_1 L_2}}}$$
How should $M_1$ and $M_2$ be sized?

pick $L_1 = L_2 = L_{\text{min}}$

One popular sizing strategy:
1. Pick $W_1 = W_{\text{MIN}}$ to minimize area of $M_1$
2. Pick $W_2$ to set trip-point at $V_{\text{DD}/2}$

Typically $V_{Tn} = 0.2V_{\text{DD}}$, $|V_{Tp}| = 0.2V_{\text{DD}}$

$$V_{\text{TRIP}} = \frac{(V_{Tn}) + (V_{\text{dd}} + V_{Tp}) \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} L_1}}{1 + \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1} L_1}}$$

$\therefore \quad \frac{V_{\text{dd}}}{2} = \frac{(0.2V_{\text{dd}}) + (V_{\text{dd}} - 0.2V_{\text{dd}}) \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1}}}{1 + \sqrt{\frac{\mu_p}{\mu_n} \frac{W_2}{W_1}}}$

Solving this equation for $W_2$, obtain

$$W_2 = W_1 \left( \frac{\mu_n}{\mu_p} \right)$$

Other sizing strategies are used as well and will be discussed later!
Extension of Basic CMOS Inverter to Multiple-Input Gates

Performs as a 2-input NOR Gate

Can be easily extended to an n-input NOR Gate

Truth Table

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Extension of Basic CMOS Inverter to Multiple-Input Gates

Performs as a 2-input NAND Gate

Can be easily extended to an n-input NAND Gate

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Static CMOS Logic Family

Observe PUN is p-channel, PDN is n-channel

Pull-up Network PUN
Pull-down Network PDN
Static CMOS Logic Family

n-channel PDN and p-channel PUN
General Logic Family

p-channel PUN
n-channel PDN

Arbitrary PUN and PDN
Other CMOS Logic Families

- Enhancement Load NMOS
- Enhancement Load Pseudo-NMOS
- Depletion Load NMOS
Other CMOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when \( V_{OUT} \) is low
- Very economical process
- Termed “ratio logic”
- Compact layout (no wells !)
Other CMOS Logic Families

- Multiple-input gates require single transistor for each additional input
- Still useful if many inputs are required (static power does not increase with k)
Other CMOS Logic Families

- High and low swings are reduced
- Response time is slow on LH output transitions
- Static Power Dissipation Large when $V_{OUT}$ is low
- Termed “ratio” logic
Other CMOS Logic Families

$V_{IN}$
$V_{OUT}$
$V_{DD}$
$M_2$
$M_1$

- $V_{TD}<0$
- Low swing is reduced
- Static Power Dissipation Large when $V_{OUT}$ is low
- Very economical process
- Termed “ratio” logic
- Compact layout (no wells!)
- Dominant MOS logic until about 1985
- Depletion device not available in most processes today
Other CMOS Logic Families

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation
- Shallow slope at $V_{TRIP}$
Other CMOS Logic Families

- Reduced $V_H - V_L$
- Device sizing critical for even basic operation
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Other CMOS Logic Families

- Reduced $V_H - V_L$
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