EE 330
Lecture 36

High-Gain Amplifiers
Digital Circuit Design

• Hierarchical Design
• Synthesis
• Basic Gate Operation
High-gain amplifier

\[ A_V = -\frac{g_m}{g_0} \]

\[ A_V = \frac{-I_{CQ}}{V_tI_{CQ}/V_{AF}} = -\frac{V_{AF}}{V_t} \]

\[ A_V = -\frac{V_{AF}}{V_t} \approx \frac{200V}{25\text{mV}} = -8000 \]

This gain is very large!
Current Sources/Mirrors

Review from Last Time

- Multiple Outputs Possible
- Can be built at sourcing or sinking currents
- Also useful as a current amplifier
- MOS counterparts work very well and are not plagued by base current
Review from Last Time

High-gain amplifier

\[ A_V \approx -8000 \]

How can we build the ideal current source?

What is the small-signal model of an actual current source?
Review from Last Time

Basic Current Sources and Sinks

Basic Bipolar Current Sinks

Basic Bipolar Current Sources

Very practical methods for biasing the BJTs can be used
Current Mirrors often used for generating sourcing and sinking currents
Basic Current Sources and Sinks

Small-signal Model of BJT Current Sinks and Sources

Small-signal model of all other BJT Sinks and Sources are the same
Nonideal current source decreased the gain by a factor of 2

But the voltage gain is still quite large

Can the gain be made even larger?
High-gain amplifier

Can the gain be made even larger?

The Cascode Configuration

Discuss
The Cascode Amplifier (consider npn BJT version)

- Actually a cascade of a CE stage followed by a CB stage but usually viewed as a “single-stage” structure
- Cascode structure is widely used
The Cascode Amplifier (consider npn BJT version)
The Cascode Amplifier (consider npn BJT version)

Instead of just determining the voltage gain, we will obtain the two-port model for the cascode amplifier.
Review of Two-Port Networks

Two alternative two-port networks

Two Port (Thevenin)

\[ V_1 = R_{in} I_1 + A_{VR} V_2 \]

\[ V_2 = R_{OUT} I_2 + A_V V_1 \]

Two Port (Norton)

\[ I_1 = g_{11} V_1 + g_{21} V_2 \]

\[ I_2 = g_{21} V_1 + g_{22} V_2 \]
Review of Two-Port Networks

Relationship between Thevenin and Norton two-port parameters

\[ V_1 = R_{in} I_1 + A_{VR} V_2 \]
\[ V_2 = R_{OUT} I_2 + A_V V_1 \]

\[ R_{IN} = \frac{1}{g_{11}} \quad R_{OUT} = \frac{1}{g_{22}} \quad A_{VR} = -\frac{g_{12}}{g_{22}} \quad A_{VR} = -\frac{g_{21}}{g_{11}} \]

\[ I_1 = g_{11} V_1 + g_{21} V_2 \]
\[ I_2 = g_{21} V_1 + g_{22} V_2 \]
Review of Two-Port Networks

Two representations of same two-port model

\[ I_1 = g_{11} V_1 + g_{21} V_2 \]
\[ I_2 = g_{21} V_1 + g_{22} V_2 \]

\[ I_1 = g_{\pi} V_1 + g_{mr} V_2 \]
\[ I_2 = g_m V_1 + g_0 V_2 \]
Often useful two-port networks comprised of transistors are unilateral.
Review of Two-Port Networks

Alternate representation of unilateral two-port networks

Unilateral Two Port

\[ I_1 = g_\pi V_1 \]
\[ I_2 = g_m V_1 + g_0 V_2 \]

\[ V_1 = R_{in} I_1 \]
\[ V_2 = R_{OUT} I_2 + A_V V_1 \]
Review of Two-Port Networks

Several methods can be used to determine two-port parameters

1. Open-short termination method
2. I/O equation formulation

\[ I_1 = g_{11} V_1 + g_{21} V_2 \]
\[ I_2 = g_{21} V_1 + g_{22} V_2 \]
Review of Two-Port Networks

Open-short termination method (Norton)

\[ I_1 = g_{11} V_1 + g_{21} V_2 \]

\[ I_2 = g_{21} V_1 + g_{22} V_2 \]

\[ V_1 = 0 \quad g_{22} \]

\[ V_2 = 0 \]

\[ g_{11} = \frac{I_1}{V_1} \bigg|_{V_2=0} \]

\[ g_{21} = \frac{I_2}{V_1} \bigg|_{V_2=0} \]
Review of Two-Port Networks

Open-short termination method (Norton)

Arbitrary Linear Network

\[ I_1 = g_{11} V_1 + g_{21} V_2 \]
\[ I_2 = g_{21} V_1 + g_{22} V_2 \]

Arbitrary Linear Network

\[ g_{21} = \frac{I_1}{V_2 \mid V_1 = 0} \]
\[ g_{22} = \frac{I_2}{V_2 \mid V_1 = 0} \]
Review of Two-Port Networks

Open-short termination method (Thevenin)

Arbitrary Linear Network

\[ V_1 = R_{\text{in}} I_1 + A_{\text{VR}} V_2 \]

\[ V_2 = R_{\text{OUT}} I_2 + A_{\text{V}} V_1 \]

\[ R_{\text{IN}} = \frac{V_1}{I_1} \bigg|_{V_2=0} \]
Review of Two-Port Networks

Open-short termination method (Thevenin)

\[
V_1 = R_{in}I_1 + A_{VR}V_2 \\
V_2 = R_{OUT}I_2 + A_VV_1
\]

\[
A_V = \frac{V_2}{V_1}_{|I_2=0}
\]
Review of Two-Port Networks

Open-short termination method (Thevenin)

\[ V_1 = R_{\text{in}} I_1 + A_{VR} V_2 \]
\[ V_2 = R_{\text{OUT}} I_2 + A_V V_1 \]

\[ R_{\text{OUT}} = \left. \frac{V_2}{I_2} \right|_{V_1=0} \]
Review of Two-Port Networks

Open-short termination method (Thevenin)

\[ V_1 = R_{\text{in}} I_1 + A_{\text{VR}} V_2 \]
\[ V_2 = R_{\text{OUT}} I_2 + A_{V} V_1 \]

\[ A_{\text{VR}} = \left. \frac{V_1}{V_2} \right|_{I_1=0} \]
Review of Two-Port Networks

Open-short termination method summary (Thevenin)

\[ V_1 = R_{\text{in}} I_1 + A_{VR} V_2 \]
\[ V_2 = R_{\text{OUT}} I_2 + A_V V_1 \]

\[ R_{\text{IN}} = \left. \frac{V_1}{I_1} \right|_{V_2=0} \]
\[ A_{VR} = \left. \frac{V_1}{V_2} \right|_{I_1=0} \]
\[ R_{\text{OUT}} = \left. \frac{V_2}{I_2} \right|_{V_1=0} \]
\[ A_V = \left. \frac{V_2}{V_1} \right|_{I_2=0} \]

For many practical transistor-level two-ports the network is unilateral so \( A_{VR}=0 \)
Review of Two-Port Networks

Several methods can be used to determine two-port parameters

1. Open-short termination method
2. I/O equation formulation

![Two Port (Norton)](image)

\[ I_1 = g_{11} V_1 + g_{12} V_2 \]
\[ I_2 = g_{21} V_1 + g_{22} V_2 \]

1. Write set of equations relating \( I_1, V_1, I_2, V_2 \), and internal node voltages/currents

\[ f_1(I_1, I_2, V_1, V_2, V_{1\text{int}}, V_{2\text{int}}, \ldots I_{1\text{int}}, I_{2\text{int}}, \ldots) = 0 \]
\[ f_2(I_1, I_2, V_1, V_2, V_{1\text{int}}, V_{2\text{int}}, \ldots I_{1\text{int}}, I_{2\text{int}}, \ldots) = 0 \]

... 
\[ f_k(I_1, I_2, V_1, V_2, V_{1\text{int}}, V_{2\text{int}}, \ldots I_{1\text{int}}, I_{2\text{int}}, \ldots) = 0 \]

2. Eliminate all variables except \( I_1, V_1, I_2, V_2 \), to obtain two linear equations in linear form

3. Read off \( g_{11}, g_{12}, g_{21} \) and \( g_{22} \) from these two equations (or \( R_{IN}, R_{OUT}, A_V, A_{VR} \))
The Cascode Amplifier (consider npn BJT version)

From the two-port model of the cascode, the $A_{VCC}$ in the model is simply the voltage gain of the cascode amplifier and $g_{0CC}$ is the output conductance of the cascode amplifier. Instead of just determining the voltage gain, we will obtain the two-port (Thevenin) model for the cascode amplifier.
The Cascode Amplifier (consider npn BJT version)
### Cascode Configuration

Two-port model of cascode amplifier

\[
\begin{aligned}
\left\{
\begin{array}{l}
(V_X + V_2)g_{02} + V_2g_{m2} = I_X \\
V_1 g_{m1} - V_2 (g_{01} + g_{\pi2}) = I_X
\end{array}
\right.
\end{aligned}
\]

Observing \( V_1 = V_{IN} \) and eliminating \( V_2 \) between these two equations, we obtain

\[
V_X = -\left[ \frac{g_{m1}(g_{02}+g_{m2})}{g_{02}(g_{\pi2}+g_{01})} \right] V_{IN} + \left[ \frac{g_{01}+g_{02}+g_{\pi2}+g_{m2}}{g_{02}(g_{01}+g_{\pi2})} \right] I_X
\]

and

\[
V_{IN} = \frac{1}{g_{\pi1}} I_1
\]
Cascode Configuration

Two-port model of cascode amplifier

\[
V_X = -\left[\frac{g_{m1}(g_{02}+g_{m2})}{g_{02}(g_{\pi2}+g_{01})}\right] V_1 + \left[\frac{g_{01}+g_{02}+g_{\pi2}+g_{m2}}{g_{02}(g_{01}+g_{\pi2})}\right] I_X
\]

\[
V_{IN} = \frac{1}{g_{\pi1}} I_1
\]

It thus follows for the npn bipolar structure that:

\[
A_{VCC} = -\left[\frac{g_{m1}(g_{02}+g_{m2})}{g_{02}(g_{\pi2}+g_{01})}\right] \approx -\left[\frac{g_{m1}g_{m2}}{g_{02}g_{\pi2}}\right]
\]

\[
g_{0CC} = \left[\frac{g_{02}(g_{01}+g_{\pi2})}{g_{01}+g_{02}+g_{\pi2}+g_{m2}}\right] \approx \left[\frac{g_{02}g_{\pi2}}{g_{m2}}\right]
\]

\[
g_{\pi CC} = g_{\pi1}
\]
Cascode Configuration

- Voltage gain is a factor of $\beta$ larger than that of the CE amplifier with current source load
- Output impedance is a factor of $\beta$ larger than that of the CE amplifier

**Expressions**

\[
A_{VCC} \approx - \left[ \frac{g_{m1}g_{m2}}{g_{02}g_{\pi2}} \right]
\]

\[
g_{0CC} \approx \left[ \frac{g_{02}g_{\pi2}}{g_{m2}} \right]
\]

\[
g_{\pi CC} = g_{\pi1}
\]

\[
A_{VCC} \approx - \left[ \frac{g_{m1}}{g_{02}} \right] \approx - \left[ \frac{g_{m1}}{g_{01}} \right] \beta
\]

\[
g_{0CC} \approx \frac{g_{01}}{\beta}
\]
Cascode Configuration

What happens to the gain if a transistor-level current source is used for $I_B$?

This gain is very large!

$$A_{VCC} \approx -\left[ \frac{g_{m1}}{g_{02}} \beta \right] \approx -\beta \left[ \frac{g_{m1}}{g_{01}} \right]$$

$$g_{0CC} \approx \frac{g_{02}}{\beta}$$

$V_{IN}$

$V_{CC}$

$V_{OUT}$

$V_{SS}$

$V_{XX}$

$Q_1$

$Q_2$

$I_B$
Cascode Configuration

\[ V_{XX} \quad Q_1 \quad V_{OUT} \quad V_{CC} \]

\[ V_{IN} \quad \pm \]

\[ V_{SS} \]

\[ I_B \]

\[ v_{OUT} \]

\[ V_{YY} \quad Q_3 \]

\[ v_{OUT} \]

\[ v_{IN} \quad \pm \]

\[ v_{OUT} \]
Cascode Configuration

$V_{XX}$
$Q_2$
$Q_3$
$V_{YY}$
$V_{CC}$

$V_{IN}$

$V_{OUT}$
High-gain amplifier comparisons

\[ AV = AVCC \left[ \frac{g_{0CC}}{g_{03} + g_{0CC}} \right] \]

But \[ g_{0CC} \sim g_{03}/\beta \]

\[ AV \approx AVCC \left[ \frac{g_{0CC}}{g_{03}} \right] \approx \frac{AVCC}{\beta} \]

This is a dramatic reduction in gain compared to what the ideal current source biasing provided.
Cascode Configuration

\[ A_V \approx A_{VCC} \left[ \frac{g_{0CC}}{g_{03}} \right] \approx \frac{A_{VCC}}{\beta} \]

But recall

\[ A_{VCC} \approx -\left[ \frac{g_{m1}}{g_{01}} \right] \beta \]

Thus

\[ A_V \approx -\left[ \frac{g_{m1}}{g_{01}} \right] \]

- This is still a factor of 2 better than that of the CE amplifier with transistor current source
- It only requires one additional transistor
- But it's not nearly as good as the gain the cascode circuit seemed to provide
Cascode Configuration Comparisons

Can we design a better current source?
In particular, one with a higher output impedance?
Better current sources

Need a higher output impedance than $g_0$.

The output impedance of the cascode circuit itself was very large!

Can a current source be built with the cascode circuit?

\[ g_{0CC} \approx \frac{g_{01}}{\beta} \]
Cascode current sources

\[ Q_1 \quad V_{XX} \quad V_{YY} \quad V_{SS} \]

\[ Q_2 \quad \]

\[ V_{SS} \]

\[ M_1 \quad V_{XX} \quad V_{YY} \quad V_{SS} \]

\[ M_2 \quad \]

\[ V_{SS} \]

\[ M_1 \quad V_{XX} \quad V_{YY} \quad V_{DD} \]

\[ M_2 \quad \]

\[ V_{DD} \]
Cascode current sources

All have the same small-signal model

$$g_{0CC} = \frac{g_{02} (g_{01} + g_{\pi2})}{g_{01} + g_{02} + g_{\pi2} + g_{m2}}$$
Cascode current sources

For the BJT cascode current sources

\[
g_{0CC} = \left[ \frac{g_{02} \left( g_{01} + g_{\pi 2} \right)}{g_{01} + g_{02} + g_{\pi 2} + g_{m2}} \right] \approx \left[ \frac{g_{02} g_{\pi 2}}{g_{m2}} \right] = \frac{g_{01}}{\beta}
\]
Cascode Configuration
This gain is very large and is a factor of 2 below that obtained with an ideal current source biasing.

Although the factor of 2 is not desired, the performance of this circuit is still very good.

This factor of 2 gain reduction is that same as was observed for the CE amplifier when a transistor-level current source was used.
Can we use more cascoding to further increase the gain?
Cascode Configuration

The double cascode

![Cascode Circuit Diagram]

- Further gain enhancement
- Further output impedance increase
- Limited applications, particularly at lower voltages, because signal swings at outputs are small

\[ A_V \approx - \left[ \frac{g_{m1}}{g_{01}} \right] \beta^2 \]

\[ g_{0CC} \approx \frac{g_{01}}{\beta^2} \]
The Cascode Amplifier (consider n-ch MOS version)

- Same functional form for gain and output conductance except $g_\pi = 0$
- Simplifications functionally different!

\[
A_{VCC} = - \left[ \frac{g_{m1}(g_{02}+g_{m2})}{g_{02}(g_\pi+g_{01})} \right] \approx - \left[ \frac{g_{m1}g_{m2}}{g_{01}g_{02}} \right]
\]

\[
g_{0CC} = \left[ \frac{g_{02}(g_{01}+g_\pi)}{g_{01}+g_{02}+g_\pi+g_{m2}} \right] \approx \left[ \frac{g_{01}g_{02}}{g_{m2}} \right]
\]
The Cascode Amplifier (consider n-ch MOS version)

Same issues for biasing with current source as for BJT case

With cascode current source, gain only drops by a factor of 2
The Cascode Amplifier (consider n-ch MOS version)

\[ A_{VCC} \approx -\frac{g_{m1}g_{m2}}{g_{01}g_{02}} \]

\[ A_{VCC} \approx -\frac{g_{m1}}{g_{01}} \]

\[ A_{VCC} \approx -\frac{1}{2} \left[ \frac{g_{m1}g_{m2}}{g_{01}g_{02}} \right] \]
The Cascode Amplifier

- Operational amplifiers often built with basic cascode configuration
- Usually configured as a differential structure when building op amps
- Have high output impedance (but can be buffered)
- Terms “telescopic cascode”, “folded-cascode”, and “regulated cascode” often refer to op amps based upon the cascode configuration

Telescopic Cascode Op Amp
(CMFB feedback biasing not shown)
Cascade Configurations

Two-stage Cascade

\[ A_{VCB} = ? \]

\[ A_{VCM} = ? \]
Cascade Configurations

Two-stage Cascade

\[ A_{VCB} \approx \begin{bmatrix} -g_{m1} \\ g_{01} + g_{\pi2} \end{bmatrix} \begin{bmatrix} -g_{m2} \\ g_{02} \end{bmatrix} \approx \frac{g_{m1}g_{m2}}{g_{\pi2}g_{02}} = \beta \frac{g_{m1}}{g_{02}} \]

\[ A_{VCM} = \begin{bmatrix} -g_{m1} \\ g_{01} \end{bmatrix} \begin{bmatrix} -g_{m2} \\ g_{02} \end{bmatrix} = \frac{g_{m1}g_{m2}}{g_{01}g_{02}} \]

- Significant increase in gain
- Gain is noninverting
- Comparable to that obtained with the cascode
Cascade Configurations

Two-stage Cascade

\[ A_{VCB} \approx \left[ \frac{-g_{m1}}{g_{01} + g_{03} + g_{\pi2}} \right] \left[ \frac{-g_{m2}}{g_{02} + g_{04}} \right] \approx \frac{g_{m1}g_{m2}}{2g_{\pi2}g_{02}} = \beta \frac{g_{m1}}{2g_{02}} \]

\[ A_{VCM} = \left[ \frac{-g_{m1}}{g_{01} + g_{03}} \right] \left[ \frac{-g_{m2}}{g_{02} + g_{04}} \right] = \frac{g_{m1}g_{m2}}{4g_{01}g_{02}} \]

Note factor or 2 and 4 reduction in gain due to actual current source bias.
Cascade Configurations

Two-stage Cascade

- Large gains can be obtained by cascading
- Gains are multiplicative (when loading is included)
- Large gains used to build “Op Amps” and feedback used to control gain value
- Some attention is needed for biasing but it is manageable
- Minor variant of the two-stage cascade often used to build Op Amps

Three-stage Cascade

- Compensation of two-stage cascade needed if feedback is applied to maintain stability
- Three or more stages are seldom cascaded because no really good way to compensate to maintain stability
Differential Amplifiers

Basic operational amplifier circuit
Differential Amplifiers

Assume left-right matching
i.e. circuit (except for excitations) is symmetric
Differential Amplifiers

Common Mode Excitation

\[ V_C = \frac{V_1 + V_2}{2} \]

\[ V_D = V_2 - V_1 \]

Difference Mode Excitation

\[ V_1 = V_C - \frac{V_D}{2} \]

\[ V_2 = V_C + \frac{V_D}{2} \]

Analysis of two circuits is generally much easier than analysis of original circuit.
Differential Amplifiers

Common Mode Excitation

\[ V_{OUT} = V_{DD} - R_1 \frac{I_{TAIL}}{2} \]

\[ A_C = \frac{V_{OUTC}}{V_C} = 0 \]

(A_C will not be quite 0 if the tail current source is nonideal)
Differential Amplifiers

Difference Mode Excitation

Theorem: The small-signal voltage of a symmetric linear network excited differentially is always 0 at every node on the axis of symmetry
Differential Amplifiers

Difference Mode Excitation

Theorem: The small-signal voltage of a symmetric linear network excited differentially is always 0 at every node on the axis of symmetry

\[ A_D = \frac{V_{OUT2}}{V_D} = -\frac{g_{m1} R_1}{2} \]
Amplifier Biasing

Amplifier biasing is that part of the design of a circuit that establishes the desired operating point (or Q-point)

Goal is to invariably minimize the impact the biasing circuit has on the small-signal performance of a circuit

Usually at most 2 dc power supplies are available and these are often fixed in value by system requirements – this restriction is cost driven

Discrete amplifiers invariably involve adding biasing resistors and use capacitor coupling and bypassing

Integrated amplifiers often use current sources which can be used in very large numbers and are very inexpensive
Amplifier Biasing

Example:

\[ A_V = -g_m R_L \]

Desired small-signal circuit
Common Emitter Amplifier

Actual small-signal circuit
\[ A_V = -g_m \left( R_L \parallel R_{C1} \right) \]
Amplifier Biasing

Example:

Desired small-signal circuit
Common Emitter Amplifier

Biased small-signal circuit
Amplifier Biasing

Example:

Desired small-signal circuit
Common Collector Amplifier

Biased circuit

Biasing components shown in blue
Amplifier Biasing

Example:

Desired small-signal circuit
Inverting Feedback Amplifier

Biased circuit
Other Basic Configurations

Darlington Configuration

- Current gain is approximately $\beta^2$
- Two diode drop between $B_{\text{eff}}$ and $E_{\text{eff}}$
Other Basic Configurations

**Sziklai Pair**

- Same basic structure as Darlington Pair
- Current gain is approximately $\beta_n \beta_n$
- Current gain will not be as large when $\beta_p < \beta_p$
- Only one diode drop between $B_{eff}$ and $E_{eff}$
Other Basic Configurations

Low offset buffers

- Actually a CC-CC or a CD-CD cascade
- Significant drop in offset between input and output
- Biasing with DC current sources
Other Basic Configurations

Voltage Attenuator

- Attenuation factor is quite accurate (Determined by geometry)
- Infinite input impedance
- $M_1$ in triode, $M_2$ in saturation
- Actually can be a channel-tapped structure
Design Strategies

• Draw on Past Experience
• Often leads to Circuit or Architecture that can be modified or extended
• Identify the degrees of freedom in the design and the number of constraints and then systematically explore the design space
• Simulation-guided computer simulation is not an effective way of exploring a multi-variable design space!
MOS Amplifiers

- 1-1 mapping between almost all bipolar amplifiers and MOS amplifiers
- Simply replace BJT with MOS devices and redo the biasing

- Small-signal gains for MOS circuits in terms of small-signal model parameters identical if set $g_{m} = 0$ for BJT circuits
MOS-Bipolar Amplifier Mapping

Common Emitter

Common Collector

Common Base

Common Source

Common Drain

Common Gate
MOS-Bipolar Amplifier Mapping

Example: Common Emitter – Common Source Circuits

\[ A_V = -\frac{g_m}{g_o + G} \]
\[ R_{IN} = \frac{1}{g_\pi} \]
\[ g_\pi = 0 \]

\[ A_V = -\frac{g_m}{g_o + G} \]
\[ R_{IN} = \infty \]
Digital Circuit Design

Most of the remainder of the course will be devoted to digital circuit design
Digital Circuit Design

• Hierarchical Design
• Basic Logic Gates
• Properties of Logic Families
• Characterization of CMOS Inverter
• Static CMOS Logic Gates
  – Ratio Logic
• Propagation Delay
  – Simple analytical models
  – Elmore Delay
• Sizing of Gates

• Propagation Delay with Multiple Levels of Logic
• Optimal driving of Large Capacitive Loads
• Power Dissipation in Logic Circuits
• Other Logic Styles
• Array Logic
• Ring Oscillators
Hierarchical Digital Design Domains:

- Behavioral:
- Structural:
- Physical

Multiple Levels of Abstraction
Hierarchical Digital Design Domains:

- Behavioral:
- Structural:
- Physical

Bottom Up Design

Top Down Design
Hierarchical Digital Design Domains:

- Behavioral:
- Structural:
- Physical

Multiple Sublevels in Each Major Level
All Design Steps may not Fit Naturally in this Description
Hierarchical Analog Design Domains:

- Behavioral:
- Structural:
- Physical

Methods:
- Bottom Up Design
- Top Down Design
Hierarchical Digital Design Domains:

**Behavioral**: Describes what a system does or what it should do

**Structural**: Identifies constituent blocks and describes how these blocks are interconnected and how they interact

**Physical**: Describes the constituent blocks to both the transistor and polygon level and their physical placement and interconnection

Multiple representations often exist at any level or sublevel
Example: Two distinct representations at the physical level (polygon sublevel)
Example: Two distinct representations at physical level (schematic sublevel)

\[ \frac{W}{L} = 4 \]

\[ \begin{align*}
W &= 4\mu \\
L &= 1\mu \\
\end{align*} \]

\[ \begin{align*}
W &= 8\mu \\
L &= 2\mu \\
\end{align*} \]
Example: Two distinct representations at the structural/behavioral level (gate sublevel)

\[ C = A \oplus B \]
In each domain, multiple levels of abstraction are generally used.

Consider Physical Domain

- Consider lowest level to highest
  0 - placement of diffusions, thin oxide regions, field oxide, ect. on a substrate.
  1 - polygons identify all mask information (not unique)
  2 - transistors (not unique)
  3 - gate level (not unique)
  4 - cell level

Adders, Flip Flop, MUTs,…
Structural Level:

- DSP
- Blocks (Adders, Memory, Registers, etc.)
- Gates
- Transistor

Information Type

HDL
Netlists
Behavior Level (top down):

- Application
- Programs
- Subroutines
- Boolean Expressions
Digital Circuit Design

- Hierarchical Design
- Basic Logic Gates
- Properties of Logic Families
- Characterization of CMOS Inverter
  - Static CMOS Logic Gates
    - Ratio Logic
  - Propagation Delay
    - Simple analytical models
    - Elmore Delay
  - Sizing of Gates
- Propagation Delay with Multiple Levels of Logic
- Optimal driving of Large Capacitive Loads
- Power Dissipation in Logic Circuits
- Other Logic Styles
- Array Logic
- Ring Oscillators
Representaion of Digital Systems
Standard Approach to Digital Circuit Design

1. Behavioral Description
   
   – Technology independent

2. RTL Description  (Register Transfer Level)
   
   (must verify (1) ⇔ (2))

3. RTL Compiler

   Registers and Combinational Logic Functions

4. Logic Optimizer

5. Logic Synthesis

   Generally use a standard call library for synthesis
Representation of Digital Systems
Standard Approach to Digital Circuit Design

1. Behavioral Description
   - Technology independent
2. RTL Description
   (must verify $1 \Leftrightarrow 2$)
3. RTL Compiler
   Registers and Combinational Logic Functions
4. Logic Optimizer

5. Logic Synthesis
   Generally use a standard call library for synthesis
6. Place and Route

(physically locates all gates and registers and interconnects them)

7. Layout Extraction
   • DRC
   • Back Annotation

8. Post Layout simulation

   May necessitate a return to a higher level in the design flow

Logic synthesis, though extensively used, often is not as efficient nor as optimal for implementing some important blocks or some important functions

These applications generally involve transistor level logic circuit design that may combine one or more different logic design styles
Logic Optimization

What is optimized (or minimized)?

- Number of Gates
- Number or Levels of Logic
- Speed
- Delay
- Power Dissipation
- Area
- Cost
- Peak Current

Depends Upon What User Is Interested In
Standard Cell Library

• Set of primitive building blocks that have been pre-characterized for dc and high frequency performance
• Generally includes basic multiple-input gates and flip flops
• P-cells often included
• Can include higher-level blocks
  – Adders, multipliers, shift registers, counters,…
• Cell library often augmented by specific needs of a group or customer
Logic Circuit Block Design

Many different logic design styles

• Static Logic Gates
• Complex Logic Gates
• Pseudo NMOS
• Pass Transistor Logic
• Dynamic Logic Gates
  • Domino Logic
  • Zipper Logic
  • Output Prediction Logic

Various logic design styles often combined in the implementation of one logic block